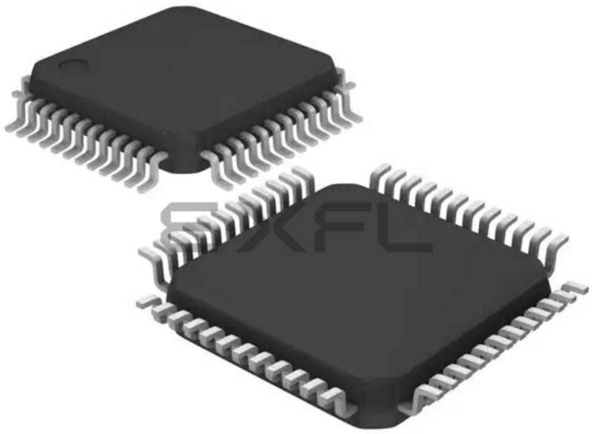

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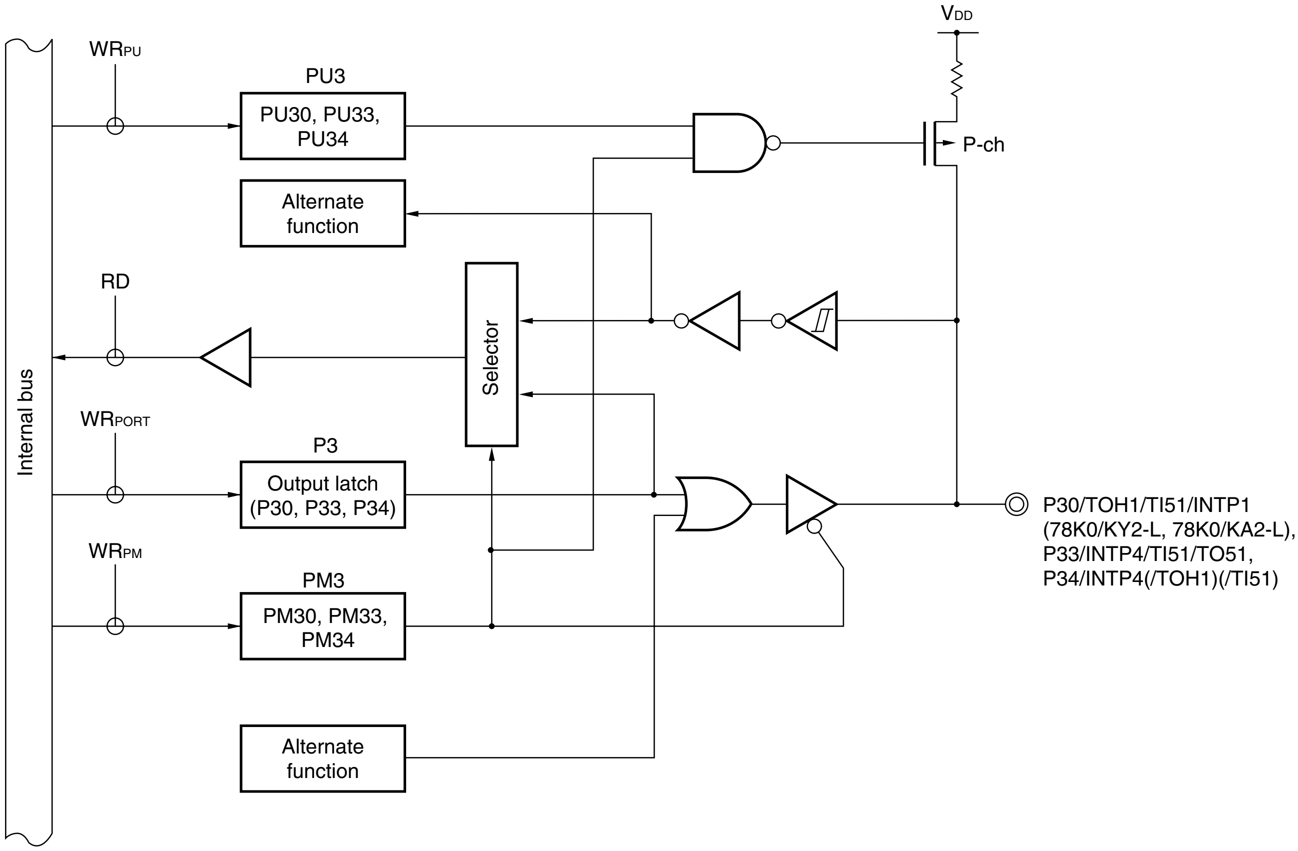
Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0588ga-gam-ax

Figure 4-15. Block Diagram of P30 (78K0/KY2-L, 78K0/KA2-L), P33, P34



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 6-42. Example of Register Settings for PPG Output Operation (1/2)

(a) 16-bit timer mode control register 00 (TMC00)

				TMC003	TMC002	TMC001	OVF00
0	0	0	0	1	1	0	0

TMC003, TMC002: Clears and starts on match between TM00 and CR000.

(b) Capture/compare control register 00 (CRC00)

					CRC002	CRC001	CRC000
0	0	0	0	0	0	0	0

CRC000: CR000 used as compare register

CRC002: CR010 used as compare register

(c) 16-bit timer output control register 00 (TOC00)

	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00
0	0	0	1	0/1	0/1	1	1

TOE00: Enables TO00 output

LVS00, LVR00: Specifies initial value of TO00 output F/F

TOC004, TOC001: 11: Inverts TO00 output on match between TM00 and CR000/CR010.

OSPT00, OSPE00: 00: Disables one-shot pulse output

(d) Prescaler mode register 00 (PRM00)

ES110	ES100	ES010	ES000	3	2	PRM001	PRM000
0	0	0	0	0	0	0/1	0/1

PRM001, PRM000: Selects count clock

(12) Reading of 16-bit timer counter 00 (TM00)

TM00 can be read without stopping the actual counter, because the count values captured to the buffer are fixed when it is read. The buffer, however, may not be updated when it is read immediately before the counter counts up, because the buffer is updated at the timing the counter counts up.

Figure 6-59. 16-bit Timer Counter 00 (TM00) Read Timing

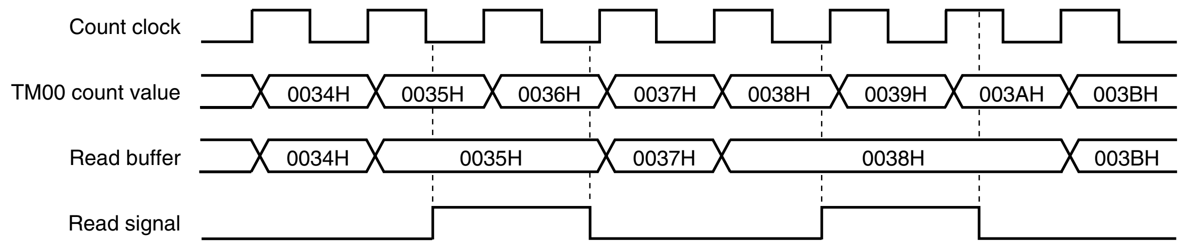


Figure 7-9. Format of 8-Bit Timer Mode Control Register 50 (TMC50) (78K0/KB2-L, 78K0/KC2-L Only)

Address: FF6BH After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC50	TCE50	TMC506	0	0	LVS50	LVR50	TMC501	TOE50

TCE50	TM50 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC506	TM50 operating mode selection
0	Mode in which clear & start occurs on a match between TM50 and CR50
1	PWM (free-running) mode

LVS50	LVR50	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO50 output: low level)
1	0	Timer output F/F set (1) (default value of TO50 output: high level)
1	1	Setting prohibited

TMC501	In other modes (TMC506 = 0)	In PWM mode (TMC506 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE50	Timer output control
0	Output disabled (TO50 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS50 and LVR50 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC501, TMC506: Operation mode setting

<2> Set TOE50 to enable output: Timer output enable

<3> Set LVS50, LVR50 (refer to Caution 1): Timer F/F setting

<4> Set TCE50

3. When TCE50 = 1, setting the other bits of TMC50 is prohibited.

4. The actual TO50/TI50/P17 pin output is determined depending on PM17 and P17 besides TO50 output.

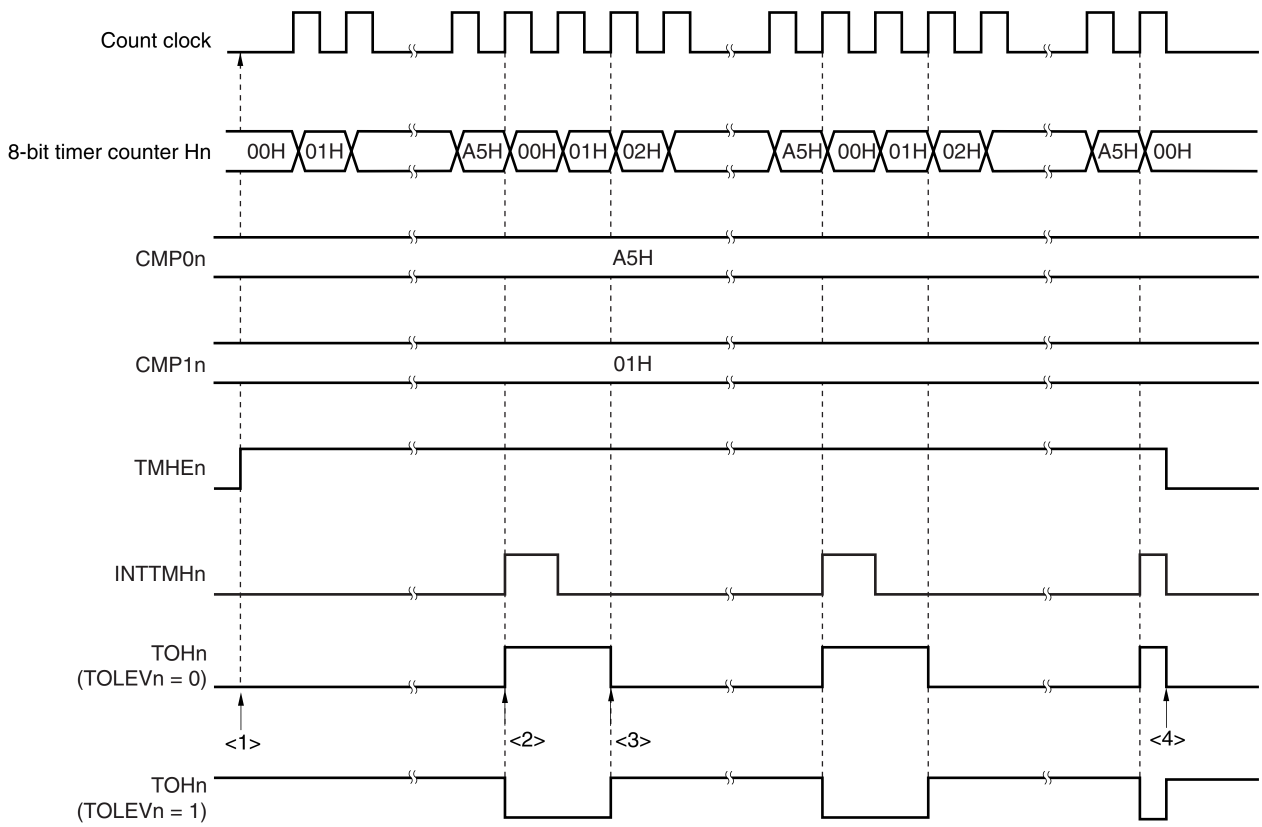
Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE50 to 0.

2. If LVS50 and LVR50 are read, the value is 0.

3. The values of the TMC506, LVS50, LVR50, TMC501, and TOE50 bits are reflected at the TO50 output regardless of the value of TCE50.

Figure 8-15. Operation Timing in PWM Output Mode (1/4)

(a) Basic operation



<1> The count operation is enabled by setting the TMHEn bit to 1. Start the 8-bit timer counter Hn by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> When the values of the 8-bit timer counter Hn and the CMP0n register match, an active level is output. At this time, the value of the 8-bit timer counter Hn is cleared, and the INTTMHn signal is output.

<3> When the values of the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output. At this time, the 8-bit timer counter value is not cleared and the INTTMHn signal is not output.

<4> Clearing the TMHEn bit to 0 during timer Hn operation sets the INTTMHn signal to the default and PWM output to an inactive level.

Remark 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

9.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

(1) Watchdog timer enable register (WDTE)

Writing ACH to WDTE clears the watchdog timer counter and starts counting again.
This register can be set by an 8-bit memory manipulation instruction.
Reset signal generation sets this register to 9AH or 1AH[Note].

Figure 9-2. Format of Watchdog Timer Enable Register (WDTE)

Address: FF99H After reset: 9AH/1AH[Note] R/W

Symbol	7	6	5	4	3	2	1	0
WDTE								

Note The WDTE reset value differs depending on the WDTON setting value of the option byte (0080H). To operate watchdog timer, set WDTON to 1.

WDTON Setting Value	WDTE Reset Value
0 (watchdog timer count operation disabled)	1AH
1 (watchdog timer count operation enabled)	9AH

Cautions 1. If a value other than ACH is written to WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

3. The value read from WDTE is 9AH/1AH (this differs from the written value (ACH)).

(5) Sub-count register (RSUBC)

The RSUBC register is a 16-bit register that counts the reference time of 1 second of the real-time counter. It takes a value of 0000H to 7FFFH and counts 1 second with a clock of 32.768 kHz.

RSUBC can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Cautions 1. When a correction is made by using the SUBCUD register, the value may become 8000H or more.

2. This register is also cleared by reset effected by writing the second count register.

3. The value read from this register is not guaranteed if it is read during operation, because a value that is changing is read.

Figure 10-6. Format of Sub-Count Register (RSUBC)

Address: FFB0H, FFB1H After reset: 0000H R

Symbol	FFB1H								FFB0H							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSUBC																

(6) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It counts up when the sub-counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Set a decimal value of 00 to 59 to this register in BCD code. If a value outside this range is set, the register value returns to the normal value after 1 period.

SEC can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-7. Format of Second Count Register (SEC)

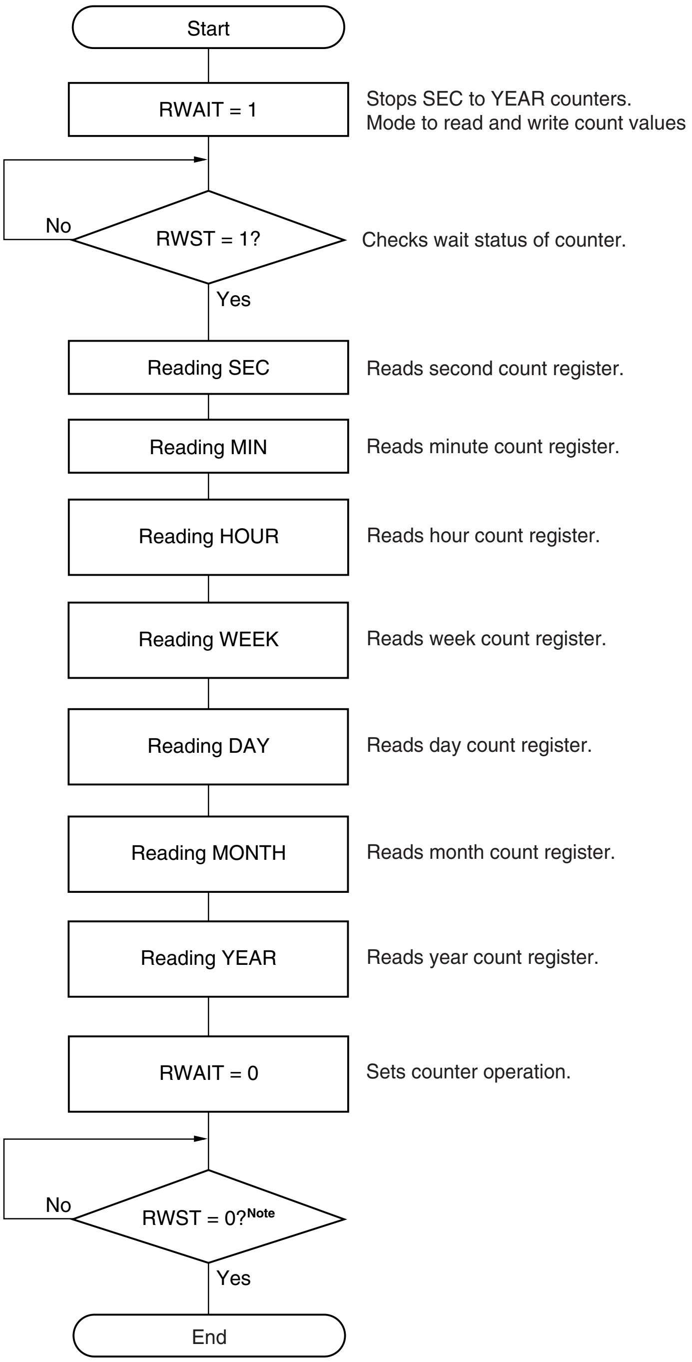
Address: FFB2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SEC	0	SEC40	SEC20	SEC10	SEC8	SEC4	SEC2	SEC1

10.4.3 Reading/writing real-time counter

Read or write the counter after setting 1 to RWAIT first.

Figure 10-21. Procedure for Reading Real-Time Counter



Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of operations of setting RWAIT to 1 to clearing RWAIT to 0 within 1 second.

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be read in any sequence.
All the registers do not have to be set and only some registers may be read.

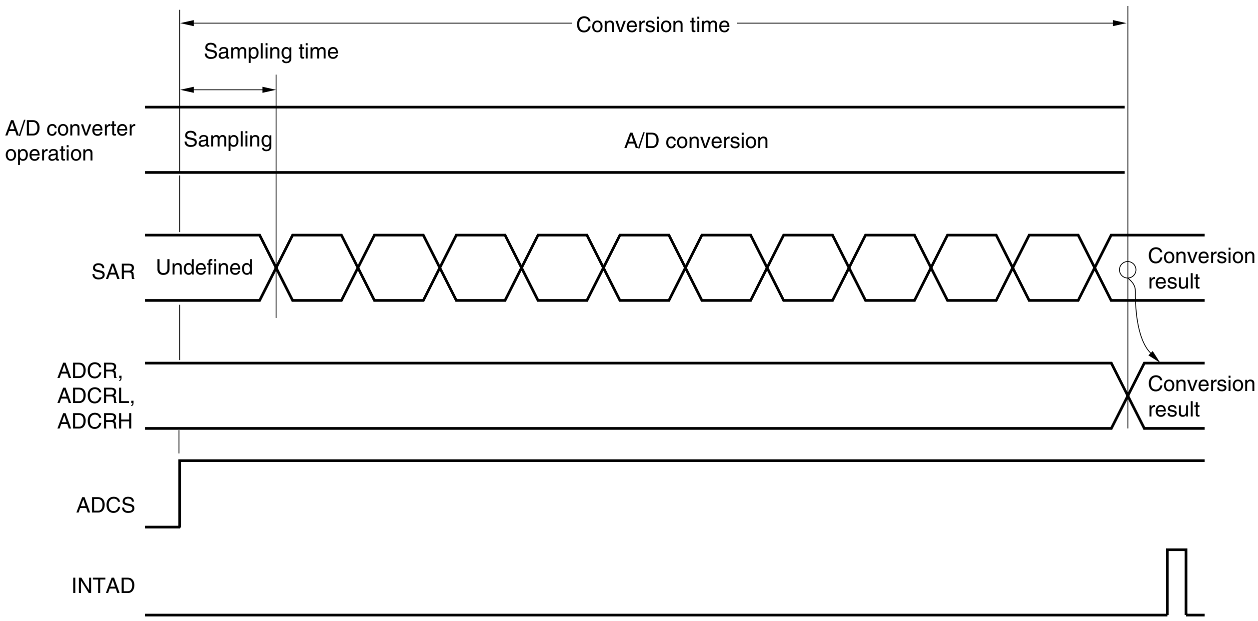
Cautions 1. Make sure the period of <2> to <6> is 1 μs or more.

2. If the timing of <2> is earlier than that of <4>, <2> may be performed any time.

Remark Three types of A/D conversion result registers are available.

- ADCR (16 bits): Store 10-bit A/D conversion value
- ADCRH (8 bits): Store the higher 8-bit A/D conversion value
- ADCRL (8 bits): Store the lower 8-bit A/D conversion value

Figure 12-13. Basic Operation of A/D Converter



A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register 0 (ADM0) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH, ADCRL) to 0000H or 00H.

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale − 3/2LSB) when the digital output changes from 1......110 to 1......111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 12-18. Zero-Scale Error

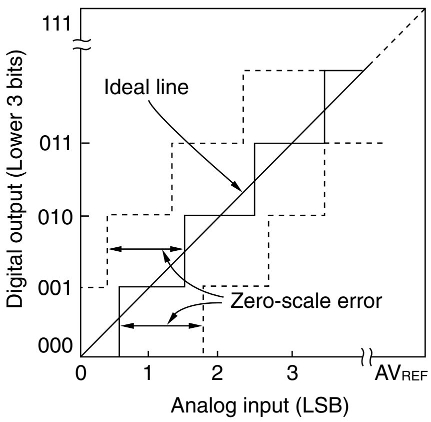


Figure 12-19. Full-Scale Error

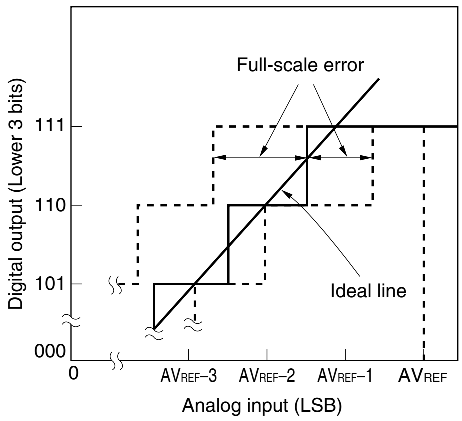


Figure 12-20. Integral Linearity Error

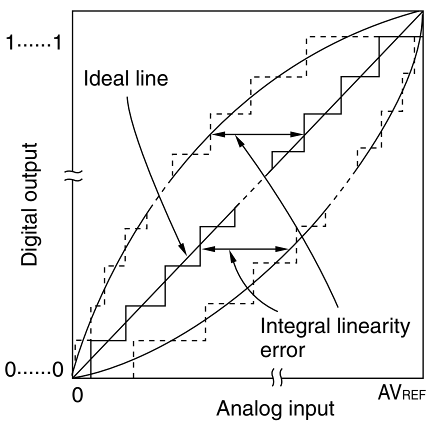
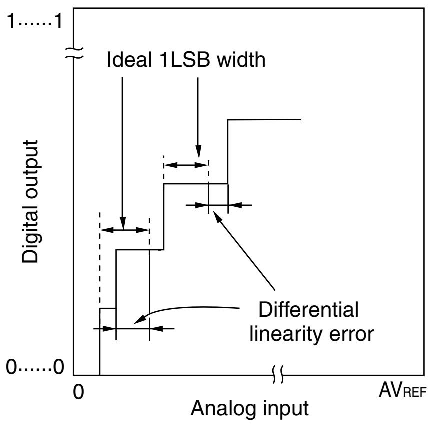


Figure 12-21. Differential Linearity Error



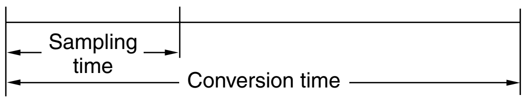
(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



(c) Normal transmission

When bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and bit 6 (TXE6) of ASIM6 is then set to 1, transmission is enabled. Transmission can be started by writing transmit data to transmit buffer register 6 (TXB6). The start bit, parity bit, and stop bit are automatically appended to the data.

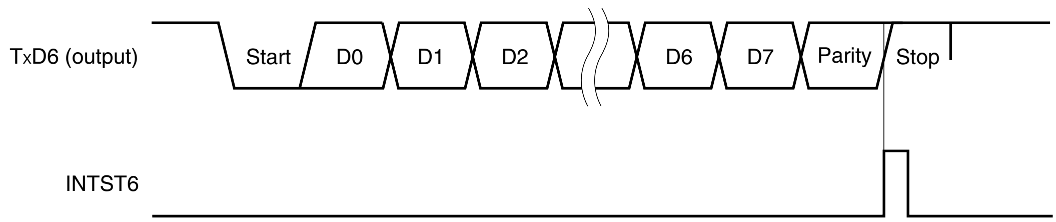
When transmission is started, the data in TXB6 is transferred to transmit shift register 6 (TXS6). After that, the transmit data is sequentially output from TXS6 to the TxD6 pin. When transmission is completed, the parity and stop bits set by ASIM6 are appended and a transmission completion interrupt request (INTST6) is generated.

Transmission is stopped until the data to be transmitted next is written to TXB6.

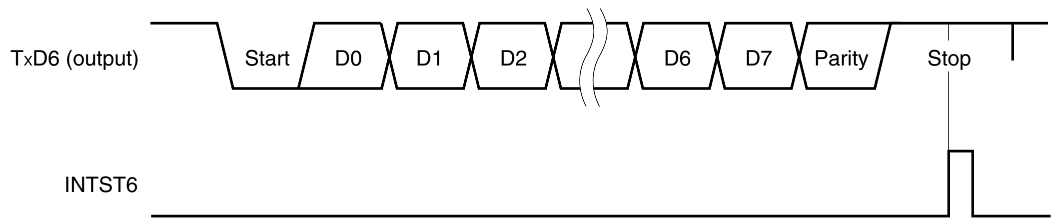
Figure 14-17 shows the timing of the transmission completion interrupt request (INTST6). This interrupt occurs as soon as the last stop bit has been output.

Figure 14-17. Normal Transmission Completion Interrupt Request Timing

1. Stop bit length: 1



2. Stop bit length: 2



An example of the processing procedure of the slave with the INTIICA0 interrupt is explained below (processing is performed assuming that no extension code is used). The INTIICA0 interrupt checks the status, and the following operations are performed.

<1> Communication is stopped if the stop condition is issued.
<2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
<3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I^2C bus remaining in the wait state.

Remark <1> to <3> above correspond to <1> to <3> in Figure 15-32 Slave Operation Flowchart (2).

Figure 15-32. Slave Operation Flowchart (2)

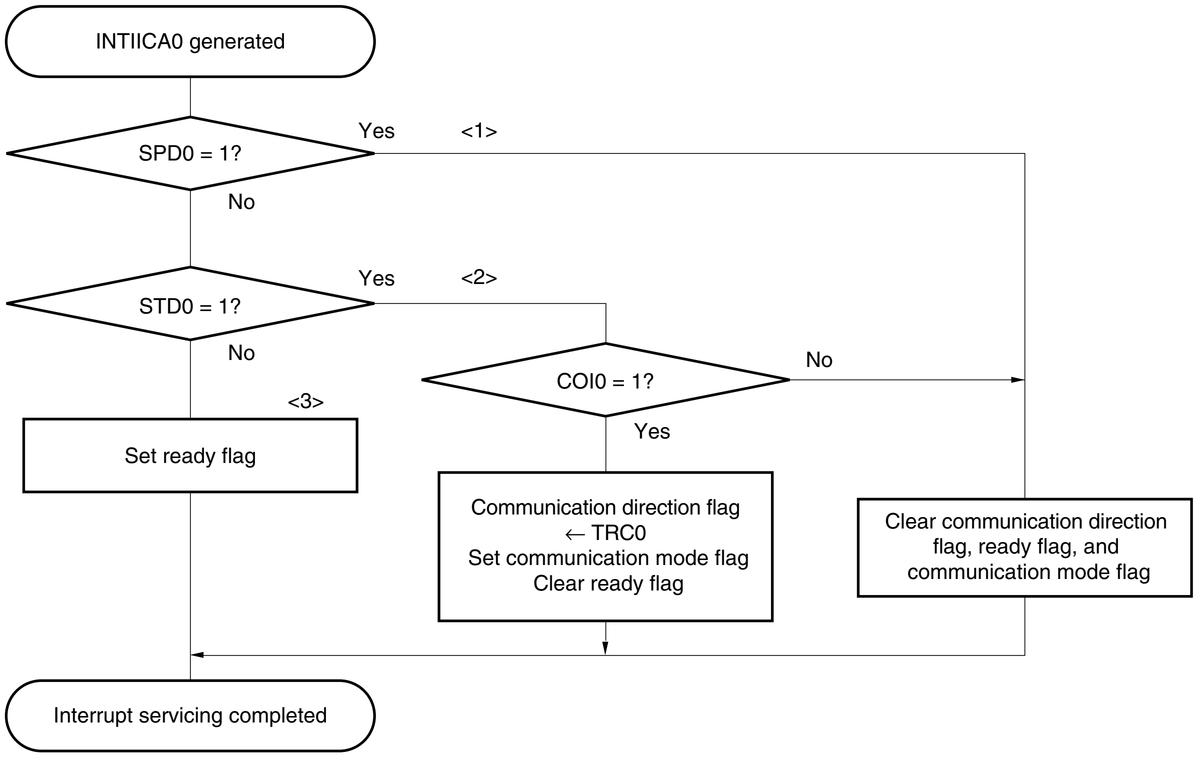
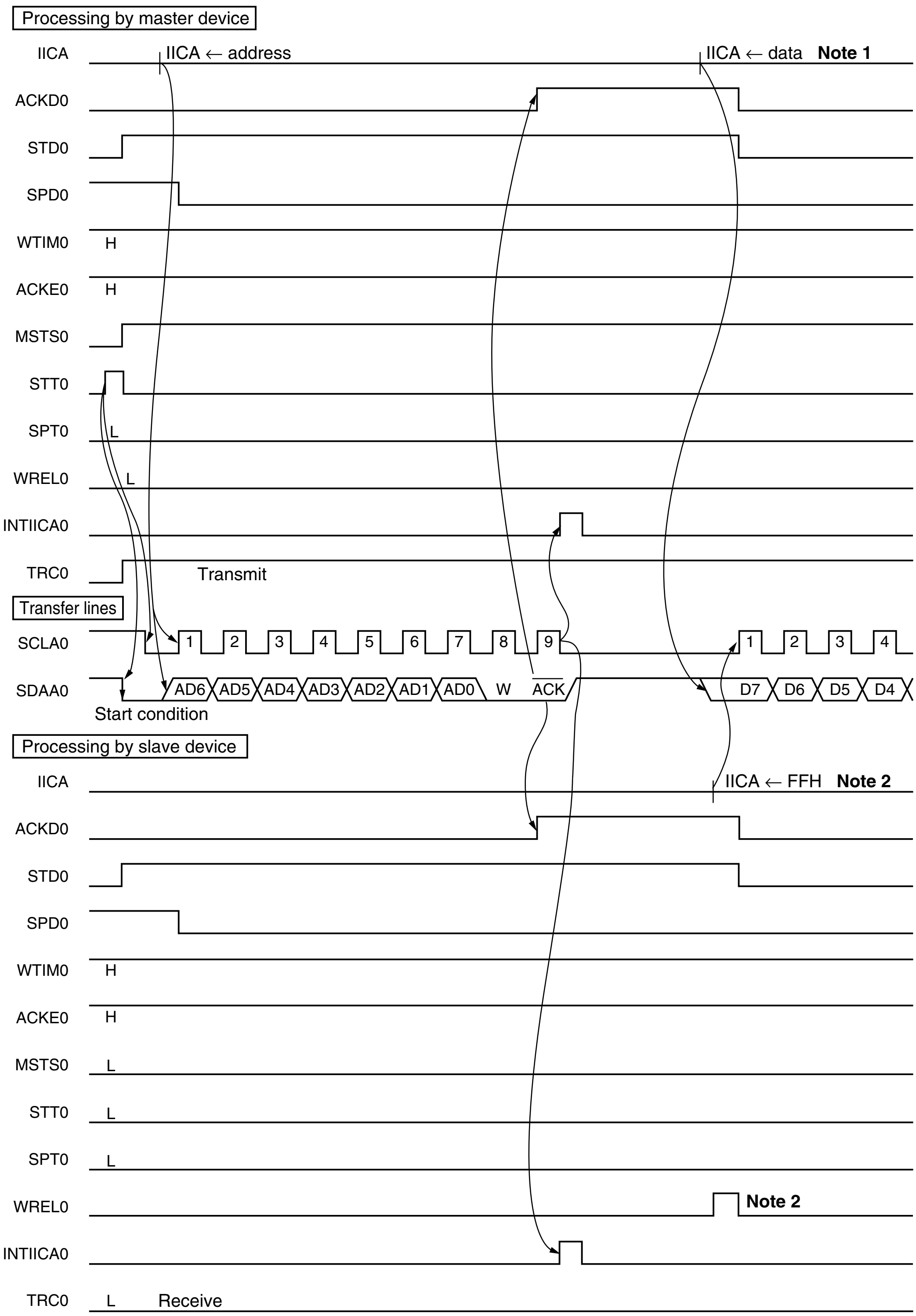


Figure 15-33. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)

(1) Start condition ~ address



Notes 1. Write data to IICA, not setting WREL0, in order to cancel a wait state during master transmission.

2. To cancel slave wait, write “FFH” to IICA or set WREL0.

(2) Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

MK0L, MK0H, MK1L, and MK1H are set by a 1-bit or 8-bit memory manipulation instruction. When MK0L and MK0H, and MK1L and MK1H are combined to form 16-bit registers MK0 and MK1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 17-9. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KY2-L)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
MK0L	SREMK6	1	1	1	1	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	5	4	<3>	2	<1>	<0>
MK0H	TMMK010	TMMK000	1	1	TMMKH1	1	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	7	6	5	4	<3>	2	1	<0>
MK1L	1	1	1	1	TMMK51	1	1	ADMK

Address: FFE7H After reset: FFH R/W

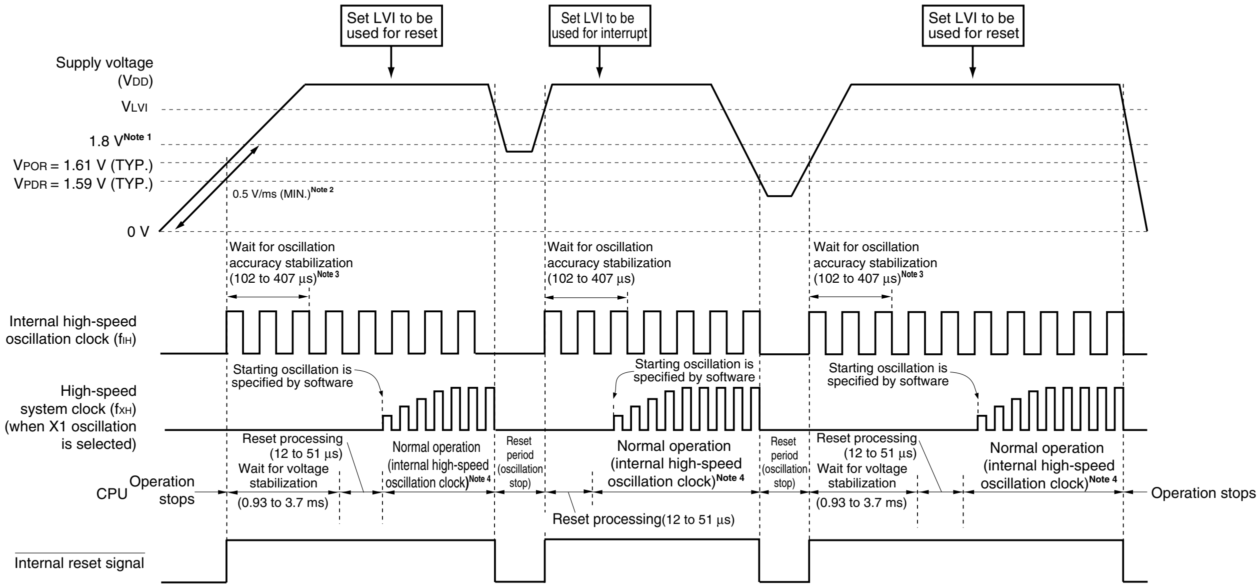
Symbol	7	6	5	4	3	2	1	<0>
MK1H	1	1	1	1	1	1	1	IICAMK0

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution Be sure to set bits 3 to 6 of MK0L, bits 2, 4 and 5 of MK0H, bits 1, 2, 4 to 7 of MK1L, and bits 1 to 7 of MK1H to 1.

Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1/2)

(1) When LVI is OFF upon power application (option byte: LVISTART = 0)



Notes 1. The operation guaranteed range is 1.8 V ≤ V_{DD} ≤ 5.5 V. To make the state at lower than 1.8 V reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input the low level to the $\overline{\text{RESET}}$ pin.

2. If the rate at which the voltage rises to 1.8 V after power application is slower than 0.5 V/ms (MIN.), input a low level to the $\overline{\text{RESET}}$ pin before the voltage reaches to 1.8 V.

3. The internal voltage stabilization wait time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

4. The internal high-speed oscillation clock, high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the OSTC register to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

Caution Set the low-voltage detector by software after the reset status is released (refer to CHAPTER 22 LOW-VOLTAGE DETECTOR).

Remark V_{LVI}: LVI detection voltage

V_{POR}: POC power supply rise detection voltage

V_{PDR}: POC power supply fall detection voltage

(2) Used as interrupt (LVIMD = 0)

- If LVISEL = 0, compares the supply voltage (V_{DD}) and LVI detection voltage (V_{LVI}). When V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$), generates an interrupt signal (INTLVI).
- If LVISEL = 1, compares the input voltage from external input pin (EXLVI) and LVI detection voltage (V_{EXLVI} = 1.21 V ±0.1 V). When EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}), generates an interrupt signal (INTLVI).

While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

Remarks 1. Level detection of input voltage from external input pin (EXLVI) is available only in 78K0/KB2-L and 78K0/KC2-L.

2. LVIMD: Bit 1 of low-voltage detection register (LVIM)
LVISEL: Bit 2 of LVIM

Table 25-9. Processing Time for Each Command When PG-FP5 Is Used (Reference) (3/3)

(2) 78K0/KB2-L, 78K0/KC2-L (2/2)

(b) Products with internal ROMs of the 16 KB: μPD78F0572, 78F0577, 78F0582, 78F0587

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	1 s (typ.)
Erase	1 s (typ.)
Program	2.5 s (typ.)
Verify	1.5 s (typ.)
E.P.V	2.5 s (typ.)
Checksum	1 s (typ.)
Security	1 s (typ.)

(c) Products with internal ROMs of the 32 KB: μPD78F0573, 78F0578, 78F0583, 78F0588

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	1 s (typ.)
Erase	1 s (typ.)
Program	4.5 s (typ.)
Verify	3 s (typ.)
E.P.V	4.5 s (typ.)
Checksum	1 s (typ.)
Security	1 s (typ.)

Caution When executing boot swapping, do not use the E.P.V. command with the dedicated flash memory programmer.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	**OR**	A, #byte	2	4	–	A ← A ∨ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∨ byte	×		
		A, r [Note 3]	2	4	–	A ← A ∨ r	×		
		r, A	2	4	–	r ← r ∨ A	×		
		A, saddr	2	4	5	A ← A ∨ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∨ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∨ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ∨ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ∨ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ∨ (HL + C)	×		
	XOR	A, #byte	2	4	–	A ← A ⊻ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ⊻ byte	×		
		A, r [Note 3]	2	4	–	A ← A ⊻ r	×		
		r, A	2	4	–	r ← r ⊻ A	×		
		A, saddr	2	4	5	A ← A ⊻ (saddr)	×		
		A, !addr16	3	8	9	A ← A ⊻ (addr16)	×		
		A, [HL]	1	4	5	A ← A ⊻ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ⊻ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ⊻ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ⊻ (HL + C)	×		
	CMP	A, #byte	2	4	–	A – byte	×	×	×
		saddr, #byte	3	6	8	(saddr) – byte	×	×	×
		A, r [Note 3]	2	4	–	A – r	×	×	×
		r, A	2	4	–	r – A	×	×	×
		A, saddr	2	4	5	A – (saddr)	×	×	×
		A, !addr16	3	8	9	A – (addr16)	×	×	×
		A, [HL]	1	4	5	A – (HL)	×	×	×
		A, [HL + byte]	2	8	9	A – (HL + byte)	×	×	×
		A, [HL + B]	2	8	9	A – (HL + B)	×	×	×
		A, [HL + C]	2	8	9	A – (HL + C)	×	×	×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

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Page	Description	Classification
CHAPTER 25 FLASH MEMORY		
p.712	Change of **Remark** in **25.8 Flash Memory Programming by Self Programming**	(e)
CHAPTER 26 ON-CHIP DEBUG FUNCTION		
p.718	Addition of **Caution 2** in **26.1 Connecting QB-MINI2 to 78K0/Kx2-L Microcontrollers**	(c)
p.720	Addition of **Figure 26-1. Connection Example of QB-MINI2 and 78K0/Ix2 Microcontrollers (2/3)**	(c)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

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Edition	Description	Chapter
2nd Edition	Modification of **Caution** in **Figure 17-14 Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KB2-L)** to **Figure 17-16 Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (48-pin products of 78K0/KC2-L)**	**CHAPTER 17 INTERRUPT FUNCTIONS**
	Addition of **Caution 4** to **19.1.1 (2) STOP mode**	**CHAPTER 19 STANDBY FUNCTION**
	Addition of 8-bit A/D conversion result register L (ADCRL) to **Table 20-2 Hardware Statuses After Reset Acknowledgment (3/4)**	**CHAPTER 20 RESET FUNCTION**
	Addition of **Note 5** to **Figure 21-2 Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)**	**CHAPTER 21 POWER-ON-CLEAR CIRCUIT**
	Modification of **Note 4** in **Figure 22-2 Format of Low-Voltage Detection Register (LVIM)**	**CHAPTER 22 LOW-VOLTAGE DETECTOR**
	Modification of **Figure 22-3 Format of Low-Voltage Detection Level Select Register (LVIS)**, modification of **Note 1**	
	Modification of description in **22.4.1 (1) (b) When LVI default start function enabled is set (LVISTART = 1) • When starting operation**	
	Modification of description in **22.4.2 (1) (b) When LVI default start function enabled is set (LVISTART = 1) • When starting operation**	
	Modification of **Cautions 1** and **3** in **Figure 23-1 Format of Regulator Mode Control Register (RMC)**	**CHAPTER 23 REGULATOR**
	Modification of **Caution** in **24.1 (2) 0081H/1081H**	**CHAPTER 24 OPTION BYTE**
	Modification of **Note 1** in **Figure 24-1 Format of Option Byte (2/3)**	
	Modification of **Caution 2** in **Figure 24-1 Format of Option Byte (3/3)**	
	Addition of **Note** to **Figure 25-2 Environment for Writing Program to Flash Memory**	**CHAPTER 25 FLASH MEMORY**
	Addition of **Note** to **Table 25-2 Pin Connection**	
	Modification of **25.4.2 TOOLD0 and TOOLD1 pins**	
	Modification of **Caution 3** and **Remark** in **25.7 Flash Memory Programming by Self Programming**	
	Revision of **Figure 26-1 Connection Example of QB-MINI2 and 78K0/Kx2-L Microcontrollers**	**CHAPTER 26 ON-CHIP DEBUG FUNCTION**
	Modification of A/D converter pins in **(2) Non-port functions**	**CHAPTER 28 ELECTRICAL SPECIFICATIONS (TARGET VALUES)**
	Modification of oscillation frequency (f_{IH}) in **Internal High-speed Oscillator Characteristics**	
	Modification of oscillation clock frequency (f_{IL} = 30 kHz) in **Internal Low-speed Oscillator Characteristics**	
	DC Characteristics • Deletion of pull-down resistor (R_{PLD1}) • Modification of supply current (I_{DD1}, I_{DD2}, I_{DD3}) • Modification of real-time counter operating current (I_{RTC}), TMH1 operating current (I_{TMH}), A/D converter operating current (I_{ADC}), and operational amplifier operating current (I_{AMP})	

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