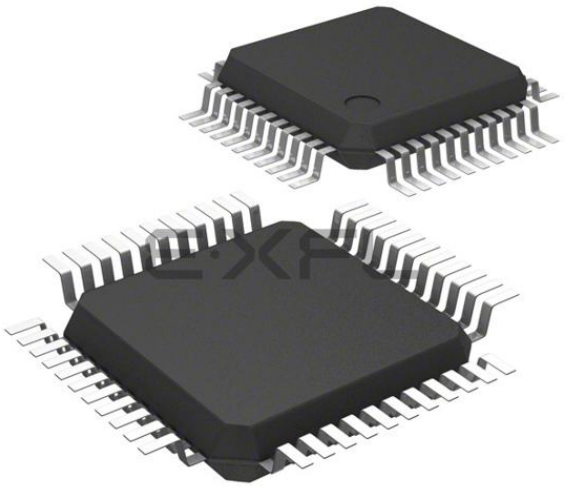
Renesas Electronics America Inc - UPD78F0588GB-GAF-AX Datasheet



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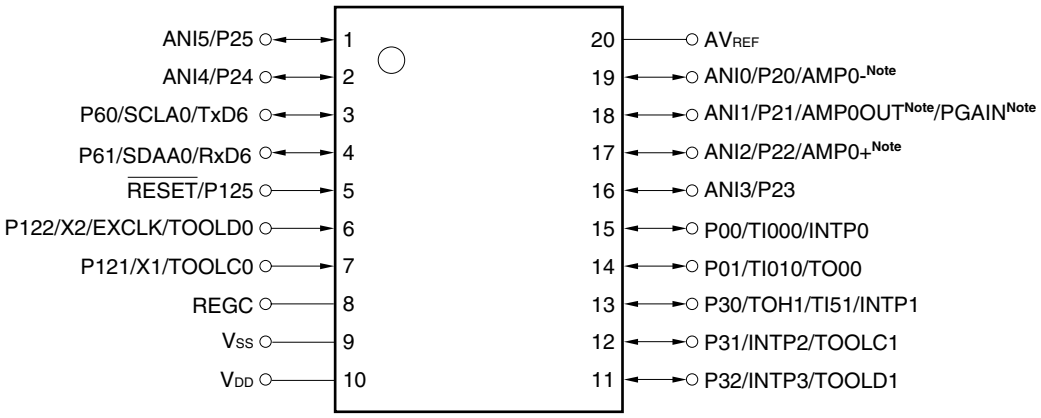
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0588gb-gaf-ax

1.3.2 78K0/KA2-L

(1) 20-pin plastic SSOP (7.62 mm (300))



AMP0-Note, AMP0+Note :	Amplifier Input	P121, P122, P125 :	Port 12
AMP0OUTNote :	Amplifier Output	REGC :	Regulator Capacitance
PGAINNote :	Programmable Gain	$\overline{\text{RESET}}$:	Reset
	Amplifier Input	RxD6 :	Receive Data
ANI0 to ANI5 :	Analog Input	SCLA0 :	Serial Clock Input/Output
AVREF :	Analog Reference	SDAA0 :	Serial Data Input/Output
	Voltage	TI000, TI010, TI51 :	Timer Input
EXCLK :	External Clock Input	TO00, TOH1 :	Timer Output
	(Main System Clock)	TOOLC0, TOOLC1 :	Clock Input for Tool
INTP0 to INTP3 :	External Interrupt	TOOLD0, TOOLD1 :	Data Input/Output for Tool
	Input	TxD6 :	Transmit Data
P00, P01 :	Port 0	VDD :	Power Supply
P20 to P25 :	Port 2	VSS :	Ground
P30 to P32 :	Port 3	X1, X2 :	Crystal Oscillator
P60, P61 :	Port 6		(Main System Clock)

Note μPD78F0565, 78F0566, 78F0567 (products with operational amplifier) only

Cautions 1. VSS functions alternately as the ground potential of the A/D converter. Be sure to connect VSS to a stabilized GND (= 0 V).

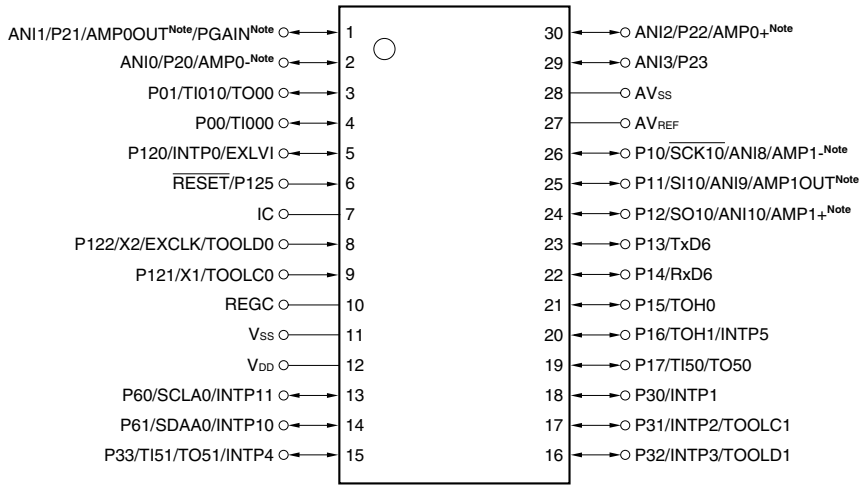
2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 to ANI5/P25 are set in the analog input mode after release of reset.

4. $\overline{\text{RESET}}$/P125 immediately after release of reset is set in the external reset input.

1.3.3 78K0/KB2-L

- 30-pin plastic SSOP (7.62 mm (300))



AMP0- Note, AMP0+ Note,		P20 to P23 :	Port 2
AMP1- Note, AMP1+ Note :	Amplifier Input	P30 to P33 :	Port 3
AMP0OUT Note,		P60, P61 :	Port 6
AMP1OUT Note :	Amplifier Output	P120 to P122, P125 :	Port 12
PGAIN Note :	Programmable Gain	REGC :	Regulator Capacitance
	Amplifier Input	RESET :	Reset
ANI0 to ANI3,		RxD6 :	Receive Data
ANI8 to ANI10 :	Analog Input	SCLA0, SCK10 :	Serial Clock Input/Output
AVREF :	Analog Reference	SDAA0 :	Serial Data Input/Output
	Voltage	SI10 :	Serial Data Input
AVSS :	Analog Ground	SO10 :	Serial Data Output
EXCLK :	External Clock Input	TI000, TI010, TI50, TI51 :	Timer Input
	(Main System Clock)	TO00, TO50, TO51,	
EXLVI :	External potential Input	TOH0, TOH1 :	Timer Output
	for Low-voltage detector	TOOLC0, TOOLC1 :	Clock Input for Tool
IC :	Internally Connected	TOOLD0, TOOLD1 :	Data Input/Output for Tool
INTP0 to INTP5,		TxD6 :	Transmit Data
INTP10, INTP11 :	External Interrupt Input	VDD :	Power Supply
P00, P01 :	Port 0	VSS :	Ground
P10 to P17 :	Port 1	X1, X2 :	Crystal Oscillator
			(Main System Clock)

Note μPD78F0576, 78F0577, 78F0578 (products with operational amplifier) only

Cautions 1. Leave the IC (Internally Connected) pin open.
2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).
3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 are set in the analog input mode, P10/ANI8/AMP1-/SCK10, P11/ANI9/AMP1OUT/SI10, and P12/ANI10/AMP1+/SO10 are set in the digital input mode after release of reset.
4. RESET/P125 immediately after release of reset is set in the external reset input.

<R>1.5 Outline of Functions

(1/2)

Item			78K0/KY2-L (μPD78F055x)	78K0/KA2-L (μPD78F056x)			78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)		
			16 Pins	20 Pins	25 Pins	32 Pins	30 Pins	40 Pins	44 Pins	48 Pins
Internal memory		Flash memory (self-programming supported)	4 KB to 16 KB				8 KB to 32 KB			
		High-Speed RAM	384 bytes to 768 bytes				512 bytes to 1 KB			
Memory space			64 KB							
Clock	Main	High-speed system (crystal/ceramic oscillation, external clock input)	1 to 10 MHz: V_{DD} = 2.7 to 5.5 V/1 to 5 MHz: V_{DD} = 1.8 to 5.5 V							
		Internal high-speed oscillation	4 MHz ± 2 % (T_A = –20 to +70°C), or 8 MHz ± 3 % (T_A = –40 to +85°C): V_{DD} = 1.8 to 5.5 V							
	Subsystem (crystal oscillation, external clock input)		–					32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V		
	Internal low-speed oscillation		30 kHz ± 10 %: V_{DD} = 2.7 to 5.5 V, 30 kHz ± 15 %: V_{DD} = 1.8 to 5.5 V							
General-purpose registers			8 bits × 32 registers (8 bits × 8 registers × 4 banks)							
Instruction set			• 8-bit operation, 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, and Boolean operation) • BCD adjust, etc.							
I/O ports (total)			12	16	21	25	24	34	38	42
	CMOS I/O		9	13	18	22	21	29	33	37
	CMOS input		3	3	3	3	3	5	5	5
Timer	16 bits (TM0)		1 ch (PPG output: 1, capture input: 2)							
	8 bits (TM5)		1 ch				2 ch (PWM output: 2)			
	8 bits (TMH)		1 ch (PWM output: 1)				2 ch (PWM output: 2)			
	Watchdog (WDT)		1 ch							
	Real-time counter		–					1 ch (RTC output : None)	1 ch (RTC output: 2)	
Clock output			–					–	–	1

2.1.1 78K0/KY2-L

(1) Port functions: 78K0/KY2-L

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000/INTP0
P01				TO00/TI010
P20	I/O	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP0-Note
P21				ANI1/AMP0OUTNote/ PGAINNote
P22				ANI2/AMP0+Note
P23				ANI3
P30	I/O	Port 3. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOH1/TI51/INTP1
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Input can be set to SMBus input buffer in 1-bit units. Output can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCLA0/TxD6
P61				SDAA0/RxD6
P121	Input	Port 12. 3-bit input-only port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0
P122				X2/EXCLK/TOOLD0
<R> P125			Reset input	$\overline{\text{RESET}}$

Note μPD78F0555, 78F0556, and 78F0557 (products with operational amplifier) only

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Tables 2-2 to 2-6 show the types of pin I/O circuits and the recommended connections of unused pins.
Refer to **Figure 2-1** for the configuration of the I/O circuit of each type.

Table 2-2. Pin I/O Circuit Types (78K0/KY2-L)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI000/INTP0	5-AQ	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P01/TO00/TI010			
ANI0/P20/AMP0-Note 1	11-P		<Digital input setting> Independently connect to AV_{REF} or V_{SS} via a resistor. <Digital output setting and analog input setting > Leave open. Note 2
<R> ANI1/P21/AMP0OUTNote 1/ PGAINNote 1	11-O		
ANI2/P22/AMP0+Note 1	11-N		
ANI3/P23	11-G		
P30/TOH1/TI51/INTP1	5-AQ		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P60/SCLA0/TxD6	5-AS		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave this pin open at low-level output after clearing the output latch of the port to 0.
P61/SDAA0/RxD6			
P121/X1/TOOLC0Note 3	37-A	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK/ TOOLD0Note 3			
$\overline{\text{RESET}}$/P125	42-A		Connect directly to V_{DD} or via a resistor.
AV_{REF}	–	–	Connect directly to V_{DD}.

Notes 1. μPD78F0555, 78F0556, and 78F0557 (products with operational amplifier) only

<R> **2.** If this pin is left open when specified as an analog input pin, the input voltage level might become undefined. It is therefore recommended to leave this pin open after specifying it as a digital output pin.

3. Use recommended connection above in input port mode (refer to **Figure 5-3 Format of Clock Operation Mode Select Register (OSCCTL)**) when these pins are not used.

Cautions 1. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 are set in the analog input mode after release of reset.

<R> **2. Because $\overline{\text{RESET}}$/P125 is set in the external reset input immediately after release of reset, if a reset signal is generated during low level input, the reset status continues until the input rises to the high level.**

Table 3-6. Special Function Register List: 78K0/KY2-L (3/4)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF51H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF52H															
FF53H	ASIS6	0	0	0	0	0	PE6	FE6	OVE6	R	–	√	–	00H	457
FF54H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF55H	ASIF6	0	0	0	0	0	0	TXBF6	TXSF6	R	–	√	–	00H	458
FF56H	CKSR6	0	0	0	0	TPS63	TPS62	TPS61	TPS60	R/W	–	√	–	00H	458
FF57H	BRGC6	MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60	R/W	–	√	–	FFH	460
FF58H	ASICL6	<SBRF6>	<SBRT6>	SBTT6	SBL62	SBL61	SBL60	DIR6	TXDLV6	R/W	√	√	–	16H	461
FF59H to FF5FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF60H	AMP0M[Note1]	<OPAMP0E>	<PGAEN>	0	0	0	0	AMP0VG1	AMP0VG0	R/W	√	√	–	00H	436
FF61H to FF6BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF6CH	TMHMD1	<TMHE1>	CKS12	CKS11	CKS10	TMMD11	TMMD10	<TOLEV1>	<TOEN1>	R/W	√	√	–	00H	339
FF6DH	TMCYC1	0	0	0	0	0	RMC1	NRZB1	<NRZ1>	R/W	√	√	–	00H	343
FF6EH to FF8BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF8CH	TCL51	0	0	0	0	0	TCL512	TCL511	TCL510	R/W	√	√	–	00H	318
FF8DH to FF98H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF99H	WDTE	–	–	–	–	–	–	–	–	R/W	–	√	–	1AH/9AH[Note2]	365
FF9AH to FF9EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF9FH	OSCCTL	<EXCLK>	<OSCSEL>	0	0	0	0	0	0	R/W	√	√	–	00H	202
FFA0H	RCM	<RSTS>	0	0	0	0	0	<LSRSTOP>	<RSTOP>	R/W	√	√	–	80H[Note3]	207
FFA1H	MCM	0	0	0	0	0	<XSEL>	<MCS>	<MCM0>	R/W	√	√	–	00H	209
FFA2H	MOC	<MSTOP>	0	0	0	0	0	0	0	R/W	√	√	–	80H	208
FFA3H	OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16	R	√	√	–	00H	210, 640
FFA4H	OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	R/W	–	√	–	05H	211, 641
FFA5H	IICA	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	490
FFA6H	SVA0	–	–	–	–	–	–	–	0	R/W	–	√	–	00H	490

Notes 1. This register is incorporated only in products with operational amplifier.

2. The reset value of WDTE is determined by setting of option byte.

3. The value of this register is 00H immediately after a reset release but automatically changes to 80H after oscillation accuracy stabilization of high-speed internal oscillator has been waited.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

(b) To stop X1 oscillation (disabling external clock input) by setting MSTOP to 1

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the high-speed system clock. When CLS = 0 and MCS = 1, the high-speed system clock is supplied to the CPU, so change the CPU clock to a clock other than the high-speed system clock.

- 78K0/KY2-L, 78K0/KA2-L, and 78K0/KB2-L

MCS	CPU Clock Status
0	Internal high-speed oscillation clock
1	High-speed system clock

- 78K0/KC2-L

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

<2> Stopping the high-speed system clock (MOC register)

When MSTOP is set to 1, X1 oscillation is stopped (the input of the external clock is disabled).

Caution Be sure to confirm that MCS = 0 or CLS = 1 when setting MSTOP to 1. In addition, stop peripheral hardware that is operating on the high-speed system clock.

5.6.2 Example of controlling internal high-speed oscillation clock

The following describes examples of clock setting procedures for the following cases.

(1) When restarting oscillation of the internal high-speed oscillation clock
(2) When using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock
(3) When stopping the internal high-speed oscillation clock

(1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock[Note 1]

<1> Setting restart of oscillation of the internal high-speed oscillation clock (RCM register)

When RSTOP is cleared to 0, the internal high-speed oscillation clock starts operating.

<2> Waiting for the oscillation accuracy stabilization time of internal high-speed oscillation clock (RCM register)

Wait until RSTS is set to 1[Note 2].

Notes 1. After a reset release, the internal high-speed oscillator automatically starts oscillating and the internal high-speed oscillation clock is selected as the CPU clock.

2. This wait time is not necessary if high accuracy is not necessary for the CPU clock and peripheral hardware clock.

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (3/4)

(6) CPU clock changing from high-speed system clock (C) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0
(C) → (B)	0	Confirm this flag is 1.	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

(7) CPU clock changing from high-speed system clock (C) to subsystem clock (D)[Note]

Note 78K0/KC2-L only

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	XTSTART	EXCLKS	OSCSELS	Waiting for Oscillation Stabilization	CSS
(C) → (D) (XT1 clock)	0	0	1	Necessary	1
	1	×	×		
(C) → (D) (external subsystem clock)	0	1	1	Unnecessary	1

Unnecessary if the CPU is operating with the subsystem clock

(8) CPU clock changing from subsystem clock (D) to internal high-speed oscillation clock (B)[Note]

Note 78K0/KC2-L only

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0	CSS
(D) → (B)	0	Confirm this flag is 1.	0	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

↑

Unnecessary if XSEL is 0

Remarks 1. (A) to (I) in Table 5-6 correspond to (A) to (I) in Figure 5-18 and 5-19.

2. MCM0: Bit 0 of the main clock mode register (MCM)
EXCLKS, OSCSELS: Bits 5 and 4 of the clock operation mode select register (OSCCTL)
RSTS, RSTOP: Bits 7 and 0 of the internal oscillation mode register (RCM)
XTSTART, CSS: Bits 6 and 4 of the processor clock control register (PCC)
×: Don't care

(1) 8-bit timer H compare register 0n (CMP0n)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in all of the timer operation modes.

This register constantly compares the value set to CMP0n with the count value of the 8-bit timer counter Hn and, when the two values match, generates an interrupt request signal (INTTMHn) and inverts the output level of TOHn.

Rewrite the value of CMP0n while the timer is stopped (TMHEn = 0).

A reset signal generation clears this register to 00H.

Figure 8-3. Format of 8-Bit Timer H Compare Register 0n (CMP0n)

Address: FF18H (CMP00), FF1AH (CMP01) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP0n								

Caution CMP0n cannot be rewritten during timer count operation. CMP0n can be refreshed (the same value is written) during timer count operation.

(2) 8-bit timer H compare register 1n (CMP1n)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in the PWM output mode and carrier generator mode.

In the PWM output mode, this register constantly compares the value set to CMP1n with the count value of the 8-bit timer counter Hn and, when the two values match, inverts the output level of TOHn. No interrupt request signal is generated.

In the carrier generator mode, the CMP1n register always compares the value set to CMP1n with the count value of the 8-bit timer counter Hn and, when the two values match, generates an interrupt request signal (INTTMHn). At the same time, the count value is cleared.

CMP1n can be refreshed (the same value is written) and rewritten during timer count operation.

If the value of CMP1n is rewritten while the timer is operating, the new value is latched and transferred to CMP1n when the count value of the timer matches the old value of CMP1n, and then the value of CMP1n is changed to the new value. If matching of the count value and the CMP1n value and writing a value to CMP1n conflict, the value of CMP1n is not changed.

A reset signal generation clears this register to 00H.

Figure 8-4. Format of 8-Bit Timer H Compare Register 1n (CMP1n)

Address: FF19H (CMP10), FF1BH (CMP11) After reset: 00H R/W

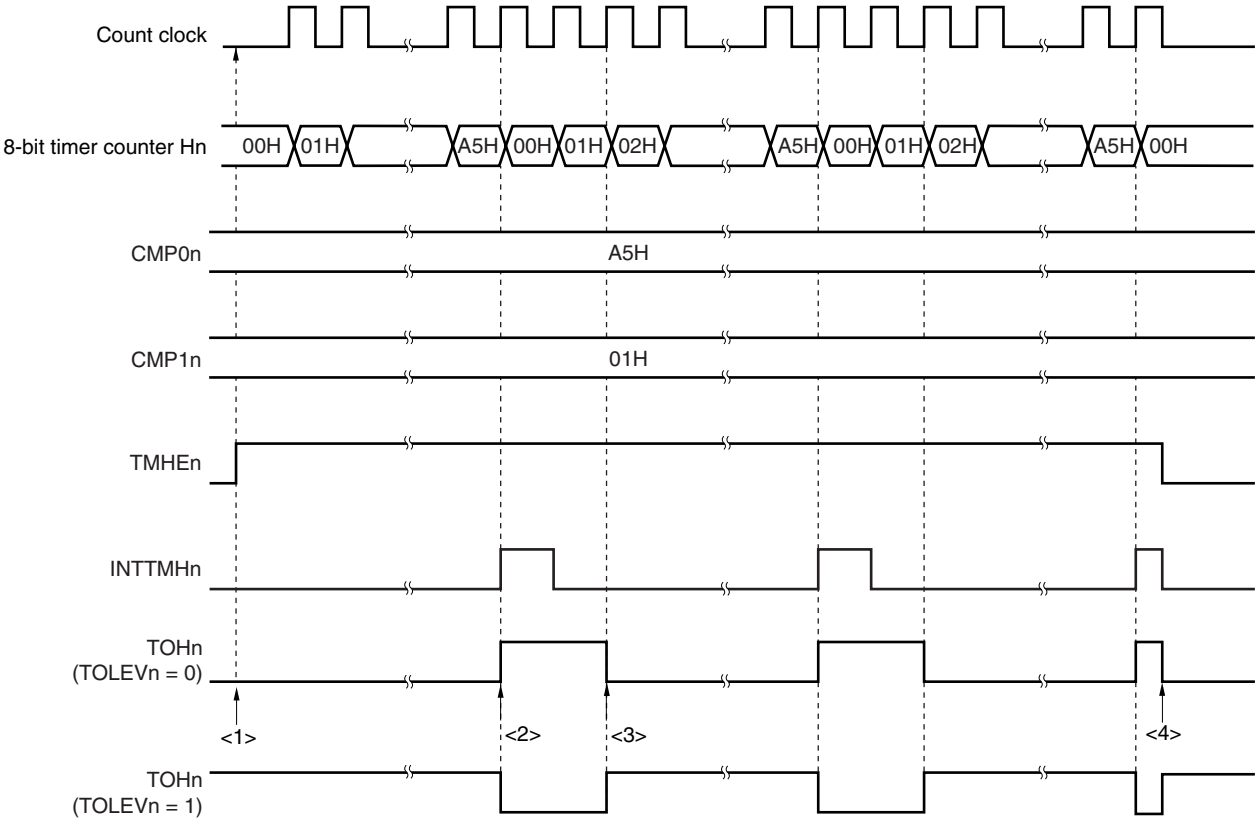
Symbol	7	6	5	4	3	2	1	0
CMP1n								

Caution In the PWM output mode and carrier generator mode, be sure to set CMP1n when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to CMP1n).

Remark 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

Figure 8-15. Operation Timing in PWM Output Mode (1/4)

(a) Basic operation



<1> The count operation is enabled by setting the TMHEn bit to 1. Start the 8-bit timer counter Hn by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> When the values of the 8-bit timer counter Hn and the CMP0n register match, an active level is output. At this time, the value of the 8-bit timer counter Hn is cleared, and the INTTMHn signal is output.

<3> When the values of the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output. At this time, the 8-bit timer counter value is not cleared and the INTTMHn signal is not output.

<4> Clearing the TMHEn bit to 0 during timer Hn operation sets the INTTMHn signal to the default and PWM output to an inactive level.

Remark 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

Table 10-2. Displayed Time Digits

24-Hour Display (AMPM bit = 1)		12-Hour Display (AMPM bit = 0)	
Time	HOUR Register	Time	HOUR Register
0	00H	0 a.m.	12H
1	01H	1 a.m.	01H
2	02H	2 a.m.	02H
3	03H	3 a.m.	03H
4	04H	4 a.m.	04H
5	05H	5 a.m.	05H
6	06H	6 a.m.	06H
7	07H	7 a.m.	07H
8	08H	8 a.m.	08H
9	09H	9 a.m.	09H
10	10H	10 a.m.	10H
11	11H	11 a.m.	11H
12	12H	0 p.m.	32H
13	13H	1 p.m.	21H
14	14H	2 p.m.	22H
15	15H	3 p.m.	23H
16	16H	4 p.m.	24H
17	17H	5 p.m.	25H
18	18H	6 p.m.	26H
19	19H	7 p.m.	27H
20	20H	8 p.m.	28H
21	21H	9 p.m.	29H
22	22H	10 p.m.	30H
23	23H	11 p.m.	31H

(9) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days. It counts up when the hour counter overflows.

This counter counts as follows.

- 01 to 31 (January, March, May, July, August, October, December)
- 01 to 30 (April, June, September, November)
- 01 to 29 (February, leap year)
- 01 to 28 (February, normal year)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.

DAY can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

15.2 Configuration of Serial Interface IICA

Serial interface IICA includes the following hardware.

Table 15-1. Configuration of Serial Interface IICA

Item	Configuration
Registers	IICA shift register (IICA) Slave address register 0 (SVA0)
Control registers	IICA control register 0 (IICACTL0) IICA status register 0 (IICAS0) IICA flag register 0 (IICAF0) IICA control register 1 (IICACTL1) IICA low-level width setting register (IICWL) IICA high-level width setting register (IICWH) Port input mode register 6 (PIM6) Port output mode register 6 (POM6) Port mode register 6 (PM6) Port register 6 (P6)

(1) IICA shift register (IICA)

This register is used to convert 8-bit serial data to 8-bit parallel data and vice versa in synchronization with the serial clock. This register can be used for both transmission and reception.

The actual transmit and receive operations can be controlled by writing and reading operations to this register.

Cancel the wait state and start data transfer by writing data to this register during the wait period.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears IICA to 00H.

Figure 15-3. Format of IICA Shift Register (IICA)

Address: FFA5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICA								

Cautions 1. Do not write data to the IICA register during data transfer.

2. Write or read the IICA register only during the wait period. Accessing the IICA register in a communication state other than during the wait period is prohibited. When the device serves as the master, however, the IICA register can be written only once after the communication trigger bit (STT0) is set to 1.

3. When communication is reserved, write data to the IICA register after the interrupt triggered by a stop condition is detected.

(2) Slave address register 0 (SVA0)

This register stores seven bits of local addresses {A6, A5, A4, A3, A2, A1, A0} when in slave mode.

This register can be set by an 8-bit memory manipulation instruction.

However, rewriting to this register is prohibited while STD0 = 1 (while the start condition is detected).

Reset signal generation clears SVA0 to 00H.

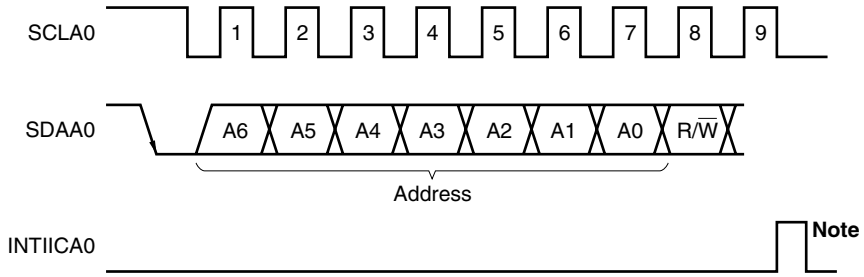
15.5.2 Addresses

The address is defined by the 7 bits of data that follow the start condition.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via the bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in the slave address register 0 (SVA0). If the address data matches the SVA0 register values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

Figure 15-17. Address



Note INTIICA0 is not issued if data other than a local address or extension code is received during slave device operation.

Addresses are output when a total of 8 bits consisting of the slave address and the transfer direction described in **15.5.3 Transfer direction specification** are written to the IICA shift register (IICA). The received addresses are written to the IICA register.

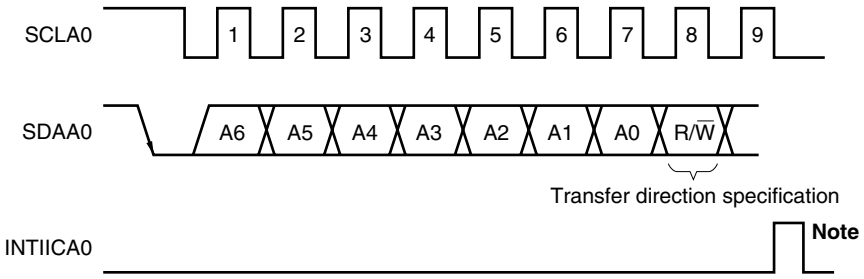
The slave address is assigned to the higher 7 bits of the IICA register.

15.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

When this transfer direction specification bit has a value of “0”, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of “1”, it indicates that the master device is receiving data from a slave device.

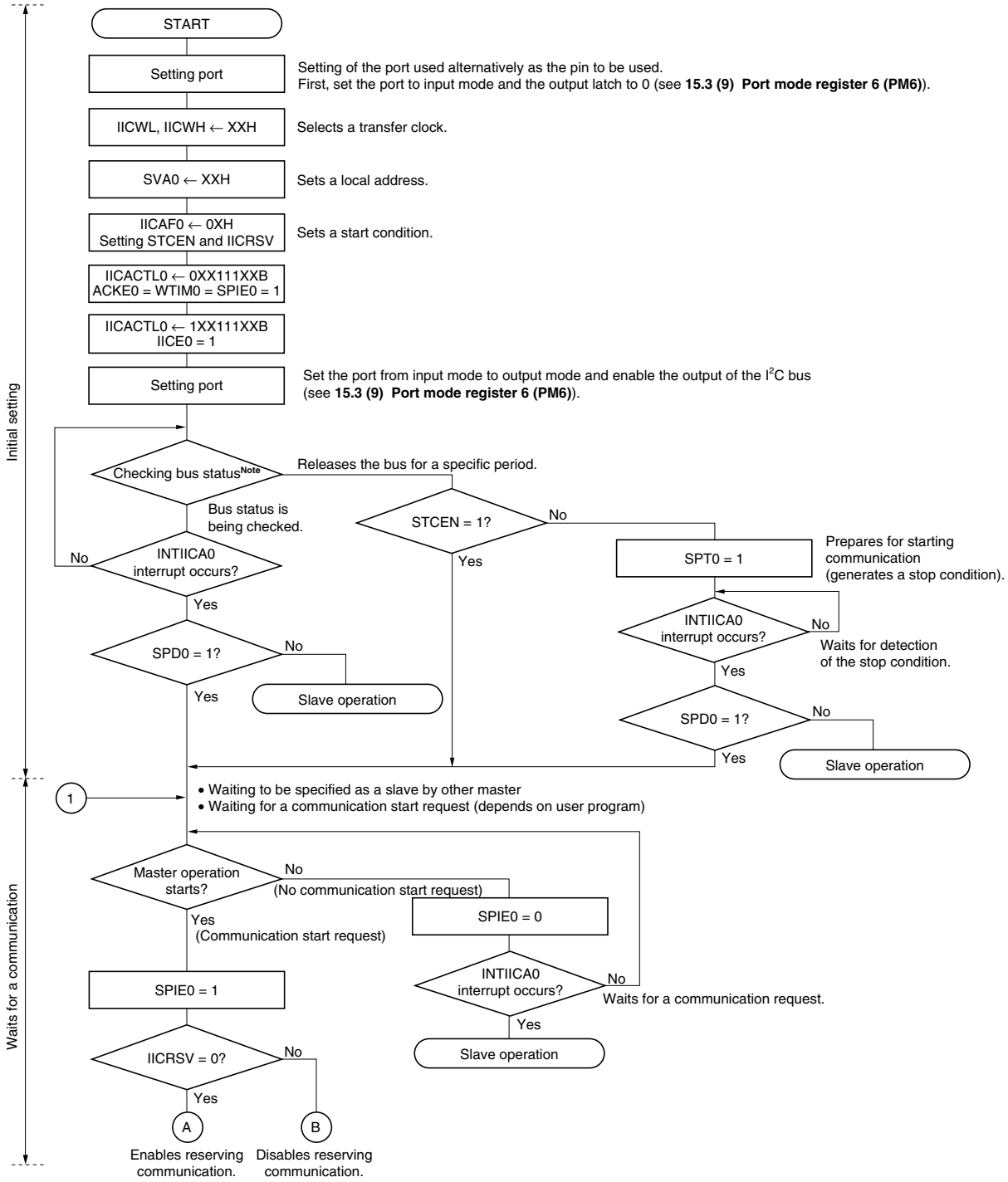
Figure 15-18. Transfer Direction Specification



Note INTIICA0 is not issued if data other than a local address or extension code is received during slave device operation.

(2) Master operation in multi-master system

Figure 15-30. Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLD0 bit = 1, DAD0 bit = 1) for a specific period (for example, for a period of one frame). If the SDAA0 pin is constantly at low level, decide whether to release the I^2C bus (SCLA0 and SDAA0 pins = high level) in conformance with the specifications of the product that is communicating.

Note 2. Do not start communication with the external clock from the $\overline{\text{SCK10}}$ pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. Do not write to CSIC10 while CSIE10 = 1 (operation enabled).

2. To use P10/$\overline{\text{SCK10}}$ and P12/SO10 as general-purpose ports, set CSIC10 in the default status (00H).

3. The phase type of the data clock is type 1 after reset.

Remark f_{PRS}: Peripheral hardware clock frequency

Figure 17-17. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KA2-L (20-pin products))

Address: FFE8H After reset: FFH R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	1	1	PPR3	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	5	4	<3>	2	<1>	<0>
PR0H	TMPR010	TMPR000	1	1	TMPRH1	1	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	7	6	5	4	<3>	2	1	<0>
PR1L	1	1	1	1	TMPR51	1	1	ADPR

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	<0>
PR1H	1	1	1	1	1	1	1	IICAPR0

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Caution Be sure to set bits 5 and 6 of PR0L, bits 2, 4 and 5 of PR0H, bits 1, 2, 4 to 7 of PR1L, and bits 1 to 7 of PR1H to 1.

(2) Low-voltage detection level select register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation input sets this register to 00H.

Figure 22-3. Format of Low-Voltage Detection Level Select Register (LVIS)

Address: FFBFH After reset: 00H[Note] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.22 ±0.1 V)
0	0	0	1	V_{LVI1} (4.07 ±0.1 V)
0	0	1	0	V_{LVI2} (3.92 ±0.1 V)
0	0	1	1	V_{LVI3} (3.76 ±0.1 V)
0	1	0	0	V_{LVI4} (3.61 ±0.1 V)
0	1	0	1	V_{LVI5} (3.45 ±0.1 V)
0	1	1	0	V_{LVI6} (3.30 ±0.1 V)
0	1	1	1	V_{LVI7} (3.15 ±0.1 V)
1	0	0	0	V_{LVI8} (2.99 ±0.1 V)
1	0	0	1	V_{LVI9} (2.84 ±0.1 V)
1	0	1	0	V_{LVI10} (2.68 ±0.1 V)
1	0	1	1	V_{LVI11} (2.53 ±0.1 V)
1	1	0	0	V_{LVI12} (2.38 ±0.1 V)
1	1	0	1	V_{LVI13} (2.22 ±0.1 V)
1	1	1	0	V_{LVI14} (2.07 ±0.07 V)
1	1	1	1	V_{LVI15} (1.91 ±0.1 V)

Note The reset value changes depending on the reset source.

<R> If the LVIS register is reset by LVI resets (except resets by the LVI default start function), it is not reset but holds the current value. The value of this register is reset to “00H” by other resets.

Cautions 1. Be sure to clear bits 4 to 7 to 0.

2. Do not change the value of LVIS during LVI operation.

3. When an input voltage from the external input pin (EXLVI) is detected, the detection voltage (V_{EXLVI} = 1.21 V (TYP.)) is fixed. Therefore, setting of LVIS is not necessary.

25.8.3 Boot swap function

If rewriting the boot area failed by temporary power failure or other reasons, restarting a program by resetting or overwriting is disabled due to data destruction in the boot area.

The boot swap function is used to avoid this problem.

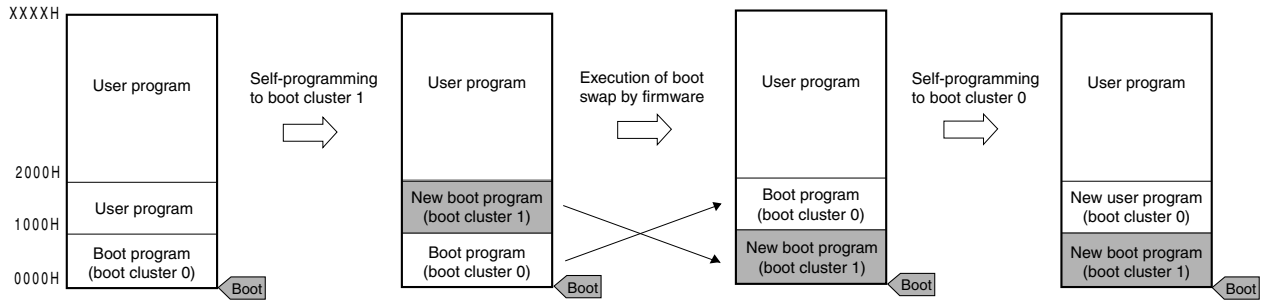
Before erasing boot cluster 0[Note], which is a boot program area, by self programming, write a new boot program to boot cluster 1 in advance. When the program has been correctly written to boot cluster 1, swap this boot cluster 1 and boot cluster 0 by using the set information function of the firmware of the 78K0/Kx2-L microcontrollers, so that boot cluster 1 is used as a boot area. After that, erase or write the original boot program area, boot cluster 0.

As a result, even if a power failure occurs while the boot programming area is being rewritten, the program is executed correctly because it is booted from boot cluster 1 to be swapped when the program is reset and started next.

Note A boot cluster is a 4 KB area and boot clusters 0 and 1 are swapped by the boot swap function.

Caution The products whose ROM size is 4 KB can not use the boot swap function.

Figure 25-10. Boot Swap Function



In an example of above figure, it is as follows.

Boot cluster 0: Boot program area before boot swap

Boot cluster 1: Boot program area after boot swap

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

DC Characteristics (3/8) (78K0/KY2-L, 78K0/KA2-L (20 pins), 78K0/KB2-L, 78K0/KC2-L)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P70 to P75, P120	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA				0.7	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 0.5 mA				0.4	V
	V_{OL2}	P20 to P27	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 15.0 mA				2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA				0.4	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA				0.6	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 3.0 mA				0.4	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA				0.4	V
Input leakage current, high	I_{LIH1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120, P125/$\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH2}	P20 to P27	V_I = AV_{REF} = V_{DD}				1	μA
	I_{LIH3}	P121 to 124	V_I = V_{DD}	I/O port mode			1	μA
		X1, X2		OSC mode			20	μA
		XT1, XT2					10	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120, P125/$\overline{\text{RESET}}$	V_I = V_{SS}				–1	μA
	I_{LIL2}	P20 to P27	V_I = V_{SS}, AV_{REF} = V_{DD}				–1	μA
	I_{LIL3}	P121 to 124	V_I = V_{SS}	I/O port mode			–1	μA
		X1, X2		OSC mode			–20	μA
		XT1, XT2					–10	μA
Pull-up resistor	R_{PLU1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120	V_I = V_{SS}		10	20	100	kΩ
	R_{PLU2}	P125/$\overline{\text{RESET}}$			75	150	300	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.5[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.