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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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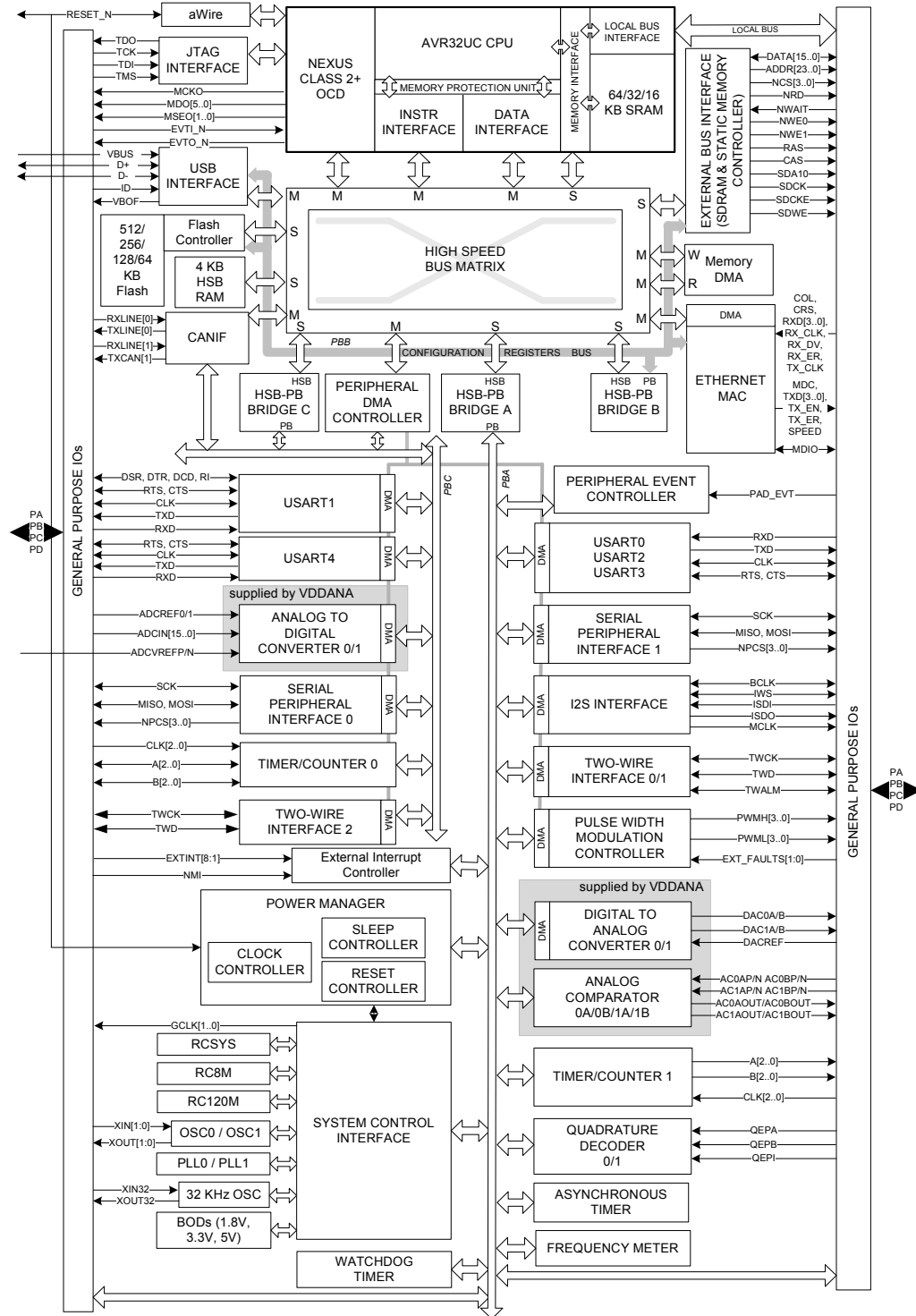
Details

Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, Ethernet, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	45
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3c2128c-a2zr

2. Overview

2.1 Block diagram

Figure 2-1. Block diagram

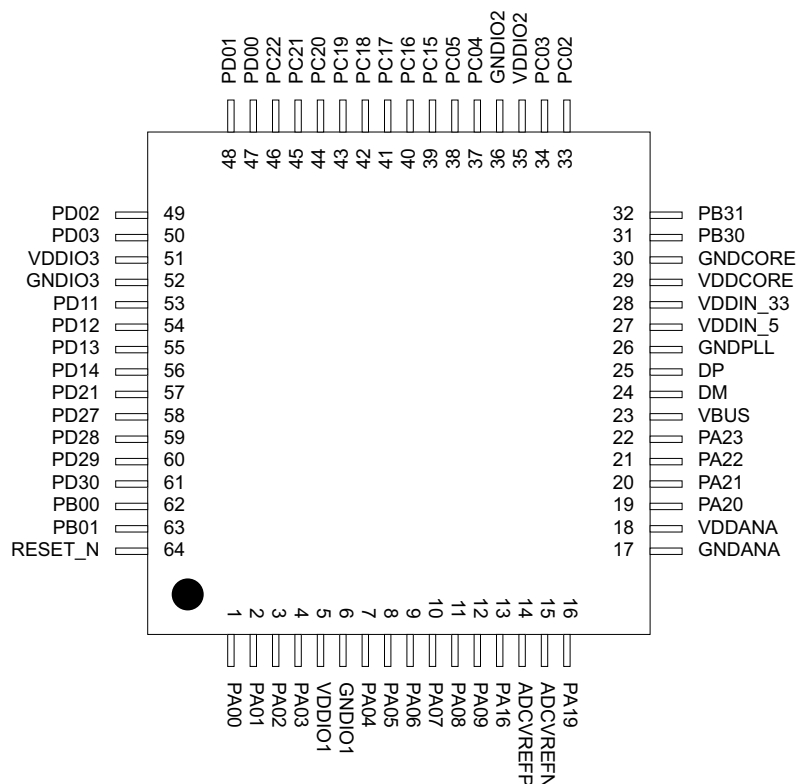


3. Package and Pinout

3.1 Package

The device pins are multiplexed with peripheral functions as described in [Table 3-1 on page 11](#).

Figure 3-1. QFN64/TQFP64 Pinout



Note: on QFN packages, the exposed pad is unconnected.

Table 3-1. GPIO Controller Function Multiplexing

TQFP / QFN 64	TQFP 100	LQFP 144	PIN	G P I O	Supply	Pin Type (1)	GPIO function					
							A	B	C	D	E	F
16	25	36	PA19	19	VDDANA	x1/x2	ADCIN8	EIC - EXTINT[1]				
19	28	39	PA20	20	VDDANA	x1/x2	ADCIN9	AC0AP0	AC0AP0 or DAC0A			
20	29	40	PA21	21	VDDANA	x1/x2	ADCIN10	AC0BN0	AC0BN0 or DAC0B			
21	30	41	PA22	22	VDDANA	x1/x2	ADCIN11	AC0AN0	PEVC - PAD_EVT [4]		MACB - SPEED	
22	31	42	PA23	23	VDDANA	x1/x2	ADCIN12	AC0BP0	PEVC - PAD_EVT [5]		MACB - WOL	
	32	43	PA24	24	VDDANA	x1/x2	ADCIN13	SPI1 - NPCS[2]				
	33	44	PA25	25	VDDANA	x1/x2	ADCIN14	SPI1 - NPCS[3]	EIC - EXTINT[0]			
		45	PA26	26	VDDANA	x1/x2	AC0AP1	EIC - EXTINT[1]				
		46	PA27	27	VDDANA	x1/x2	AC0AN1	EIC - EXTINT[2]				
		47	PA28	28	VDDANA	x1/x2	AC0BP1	EIC - EXTINT[3]				
		48	PA29	29	VDDANA	x1/x2	AC0BN1	EIC - EXTINT[0]				
62	96	140	PB00	32	VDDIO1	x1	USART0 - CLK	CANIF - RXLINE[1]	EIC - EXTINT[8]	PEVC - PAD_EVT [10]		
63	97	141	PB01	33	VDDIO1	x1		CANIF - TXLINE[1]		PEVC - PAD_EVT [11]		
	99	143	PB02	34	VDDIO1	x1		USBC - ID	PEVC - PAD_EVT [6]	TC1 - A1		
	100	144	PB03	35	VDDIO1	x1		USBC - VBOF	PEVC - PAD_EVT [7]			
	7	7	PB04	36	VDDIO1	x1/x2	SPI1 - MOSI	CANIF - RXLINE[0]	QDEC1 - QEPI		MACB - TXD[2]	
	8	8	PB05	37	VDDIO1	x1/x2	SPI1 - MISO	CANIF - TXLINE[0]	PEVC - PAD_EVT [12]	USART3 - CLK	MACB - TXD[3]	
	9	9	PB06	38	VDDIO1	x2/x4	SPI1 - SCK		QDEC1 - QEPA	USART1 - CLK	MACB - TX_ER	
		10	PB07	39	VDDIO1	x1/x2	SPI1 - NPCS[0]	EIC - EXTINT[2]	QDEC1 - QEPB		MACB - RX_DV	
		11	PB08	40	VDDIO1	x1/x2	SPI1 - NPCS[1]	PEVC - PAD_EVT [1]	PWM - PWML[0]		MACB - RXD[0]	
		12	PB09	41	VDDIO1	x1/x2	SPI1 - NPCS[2]		PWM - PWMH[0]		MACB - RXD[1]	
		13	PB10	42	VDDIO1	x1/x2	USART1 - DTR	SPI0 - MOSI	PWM - PWML[1]			

Table 3-1. GPIO Controller Function Multiplexing

TQFP / QFN 64	TQFP 100	LQFP 144	PIN	GPIO	Supply	Pin Type (1)	GPIO function					
							A	B	C	D	E	F
	72	97	PC24	88	VDDIO3	x1/x2	QDEC1 - QEPA	CANIF - TXLINE[1]	EBI - DATA[5]	PEVC - PAD_EVT [4]		
		98	PC25	89	VDDIO3	x1/x2		TC1 - CLK2	EBI - DATA[6]	SCIF - GCLK[0]	USART4 - TXD	
		99	PC26	90	VDDIO3	x1/x2	QDEC1 - QEPI	TC1 - B2	EBI - DATA[7]	SCIF - GCLK[1]	USART4 - RXD	
		100	PC27	91	VDDIO3	x1/x2		TC1 - A2	EBI - DATA[8]	EIC - EXTINT[0]	USART4 - CTS	
		101	PC28	92	VDDIO3	x1/x2	SPI0 - NPCS[3]	TC1 - CLK1	EBI - DATA[9]		USART4 - RTS	
		102	PC29	93	VDDIO3	x1/x2	SPI0 - NPCS[1]	TC1 - B1	EBI - DATA[10]			
		105	PC30	94	VDDIO3	x1/x2	SPI0 - NPCS[2]	TC1 - A1	EBI - DATA[11]			
	73	106	PC31	95	VDDIO3	x1/x2	SPI0 - NPCS[3]	TC1 - B0	EBI - DATA[12]	PEVC - PAD_EVT [5]	USART4 - CLK	
47	74	107	PD00	96	VDDIO3	x1/x2	SPI0 - MOSI	TC1 - CLK0	EBI - DATA[13]	QDEC0 - QEPI	USART0 - TXD	
48	75	108	PD01	97	VDDIO3	x1/x2	SPI0 - MISO	TC1 - A0	EBI - DATA[14]	TC0 - CLK1	USART0 - RXD	
49	76	109	PD02	98	VDDIO3	x2/x4	SPI0 - SCK	TC0 - CLK2	EBI - DATA[15]	QDEC0 - QEPA		
50	77	110	PD03	99	VDDIO3	x1/x2	SPI0 - NPCS[0]	TC0 - B2	EBI - ADDR[0]	QDEC0 - QEPB		
		111	PD04	100	VDDIO3	x1/x2	SPI0 - MOSI		EBI - ADDR[1]			
		112	PD05	101	VDDIO3	x1/x2	SPI0 - MISO		EBI - ADDR[2]			
		113	PD06	102	VDDIO3	x2/x4	SPI0 - SCK		EBI - ADDR[3]			
	78	114	PD07	103	VDDIO3	x1/x2	USART1 - DTR	EIC - EXTINT[5]	EBI - ADDR[4]	QDEC0 - QEPI	USART4 - TXD	
	79	115	PD08	104	VDDIO3	x1/x2	USART1 - DSR	EIC - EXTINT[6]	EBI - ADDR[5]	TC1 - CLK2	USART4 - RXD	
	80	116	PD09	105	VDDIO3	x1/x2	USART1 - DCD	CANIF - RXLINE[0]	EBI - ADDR[6]	QDEC0 - QEPA	USART4 - CTS	
	81	117	PD10	106	VDDIO3	x1/x2	USART1 - RI	CANIF - TXLINE[0]	EBI - ADDR[7]	QDEC0 - QEPB	USART4 - RTS	
53	84	120	PD11	107	VDDIO3	x1/x2	USART1 - TXD	USBC - ID	EBI - ADDR[8]	PEVC - PAD_EVT [6]	MACB - TXD[0]	
54	85	121	PD12	108	VDDIO3	x1/x2	USART1 - RXD	USBC - VBOF	EBI - ADDR[9]	PEVC - PAD_EVT [7]	MACB - TXD[1]	
55	86	122	PD13	109	VDDIO3	x2/x4	USART1 - CTS	USART1 - CLK	EBI - SDCK	PEVC - PAD_EVT [8]	MACB - RXD[0]	
56	87	123	PD14	110	VDDIO3	x1/x2	USART1 - RTS	EIC - EXTINT[7]	EBI - ADDR[10]	PEVC - PAD_EVT [9]	MACB - RXD[1]	

Table 3-7. Signal Description List

Signal Name	Function	Type	Active Level	Comments
RX_CLK	Receive Clock	Input		
RX_DV	Receive Data Valid	Input		
RX_ER	Receive Coding Error	Input		
SPEED	Speed	Output		
TXD[3:0]	Transmit Data	Output		
TX_CLK	Transmit Clock or Reference Clock	Input		
TX_EN	Transmit Enable	Output		
TX_ER	Transmit Coding Error	Output		
WOL	Wake-On-LAN	Output		
Peripheral Event Controller - PEVC				
PAD_EVT[15:0]	Event Input Pins	Input		
Power Manager - PM				
RESET_N	Reset Pin	Input	Low	
Pulse Width Modulator - PWM				
PWMH[3:0] PWML[3:0]	PWM Output Pins	Output		
EXT_FAULT[1:0]	PWM Fault Input Pins	Input		
Quadrature Decoder- QDEC0/QDEC1				
QEPA	QEPA quadrature input	Input		
QEPB	QEPB quadrature input	Input		
QEPI	Index input	Input		
System Controller Interface- SCIF				
XIN0, XIN1, XIN32	Crystal 0, 1, 32K Inputs	Analog		
XOUT0, XOUT1, XOUT32	Crystal 0, 1, 32K Output	Analog		
GCLK0 - GCLK1	Generic Clock Pins	Output		
Serial Peripheral Interface - SPI0, SPI1				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		

4. Processor and Architecture

Rev: 2.1.2.0

This chapter gives an overview of the AVR32UC CPU. AVR32UC is an implementation of the AVR32 architecture. A summary of the programming model, instruction set, and MPU is presented. For further details, see the *AVR32 Architecture Manual* and the *AVR32UC Technical Reference Manual*.

4.1 Features

- **32-bit load/store AVR32A RISC architecture**
 - 15 general-purpose 32-bit registers
 - 32-bit Stack Pointer, Program Counter and Link Register reside in register file
 - Fully orthogonal instruction set
 - Privileged and unprivileged modes enabling efficient and secure operating systems
 - Innovative instruction set together with variable instruction length ensuring industry leading code density
 - DSP extension with saturating arithmetic, and a wide variety of multiply instructions
- **3-stage pipeline allowing one instruction per clock cycle for most instructions**
 - Byte, halfword, word, and double word memory access
 - Multiple interrupt priority levels
- **MPU allows for operating systems with memory protection**
- **FPU enables hardware accelerated floating point calculations**
- **Secure State for supporting FlashVault technology**

4.2 AVR32 Architecture

AVR32 is a new, high-performance 32-bit RISC microprocessor architecture, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption and high code density. In addition, the instruction set architecture has been tuned to allow a variety of microarchitectures, enabling the AVR32 to be implemented as low-, mid-, or high-performance processors. AVR32 extends the AVR family into the world of 32- and 64-bit applications.

Through a quantitative approach, a large set of industry recognized benchmarks has been compiled and analyzed to achieve the best code density in its class. In addition to lowering the memory requirements, a compact code size also contributes to the core's low power characteristics. The processor supports byte and halfword data types without penalty in code size and performance.

Memory load and store operations are provided for byte, halfword, word, and double word data with automatic sign- or zero extension of halfword and byte data. The C-compiler is closely linked to the architecture and is able to exploit code optimization features, both for size and speed.

In order to reduce code size to a minimum, some instructions have multiple addressing modes. As an example, instructions with immediates often have a compact format with a smaller immediate, and an extended format with a larger immediate. In this way, the compiler is able to use the format giving the smallest code size.

Another feature of the instruction set is that frequently used instructions, like add, have a compact format with two operands as well as an extended format with three operands. The larger format increases performance, allowing an addition and a data move in the same instruction in a

Table 4-3. System Registers (Continued)

Reg #	Address	Name	Function
24	96	JAVA_LV1	Unused in AVR32UC
25	100	JAVA_LV2	Unused in AVR32UC
26	104	JAVA_LV3	Unused in AVR32UC
27	108	JAVA_LV4	Unused in AVR32UC
28	112	JAVA_LV5	Unused in AVR32UC
29	116	JAVA_LV6	Unused in AVR32UC
30	120	JAVA_LV7	Unused in AVR32UC
31	124	JTBA	Unused in AVR32UC
32	128	JBCR	Unused in AVR32UC
33-63	132-252	Reserved	Reserved for future use
64	256	CONFIG0	Configuration register 0
65	260	CONFIG1	Configuration register 1
66	264	COUNT	Cycle Counter register
67	268	COMPARE	Compare register
68	272	TLBEHI	Unused in AVR32UC
69	276	TLBELO	Unused in AVR32UC
70	280	PTBR	Unused in AVR32UC
71	284	TLBEAR	Unused in AVR32UC
72	288	MMUCR	Unused in AVR32UC
73	292	TLBARLO	Unused in AVR32UC
74	296	TLBARHI	Unused in AVR32UC
75	300	PCCNT	Unused in AVR32UC
76	304	PCNT0	Unused in AVR32UC
77	308	PCNT1	Unused in AVR32UC
78	312	PCCR	Unused in AVR32UC
79	316	BEAR	Bus Error Address Register
80	320	MPUAR0	MPU Address Register region 0
81	324	MPUAR1	MPU Address Register region 1
82	328	MPUAR2	MPU Address Register region 2
83	332	MPUAR3	MPU Address Register region 3
84	336	MPUAR4	MPU Address Register region 4
85	340	MPUAR5	MPU Address Register region 5
86	344	MPUAR6	MPU Address Register region 6
87	348	MPUAR7	MPU Address Register region 7
88	352	MPUPSR0	MPU Privilege Select Register region 0
89	356	MPUPSR1	MPU Privilege Select Register region 1

7.7 Flash Characteristics

Table 7-15 gives the device maximum operating frequency depending on the number of flash wait states. The FSW bit in the FLASHC FSR register controls the number of wait states used when accessing the flash memory.

Table 7-15. Maximum Operating Frequency

Flash Wait States	Read Mode	Maximum Operating Frequency
0	1 cycle	25MHz
1	2 cycles	50MHz

Table 7-16. Flash Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FPP}	Page programming time	$f_{CLK_HSB} = 50\text{MHz}$		17		ms
t_{FPE}	Page erase time			17		
t_{FFP}	Fuse programming time			1.3		
t_{FEA}	Full chip erase time (EA)			18.3		
t_{FCE}	JTAG chip erase time (CHIP_ERASE)	$f_{CLK_HSB} = 115\text{kHz}$		640		

Table 7-17. Flash Endurance and Data Retention

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{FARRAY}	Array endurance (write/page)		10k			cycles
N_{FFUSE}	General Purpose fuses endurance (write/bit)		500			cycles
t_{RET}	Data retention		15			years

Table 7-29. ADC Decoupling requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{ADCREFPN}$	ADCREFP/ADCREFN capacitance	No voltage reference applied on ADCREFP/ADCREFN		100		nF

Table 7-30. ADC Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADCINn}	ADC input voltage range		0		V_{VDDANA}	V
C_{ONCHIP}	Internal Capacitance	ADC used without S/H			5	pF
		ADC used with S/H			4	
R_{ONCHIP}	Switch resistance	ADC used without S/H			5.1	k Ω
		ADC used with S/H			4.6	

Figure 7-3. ADC input

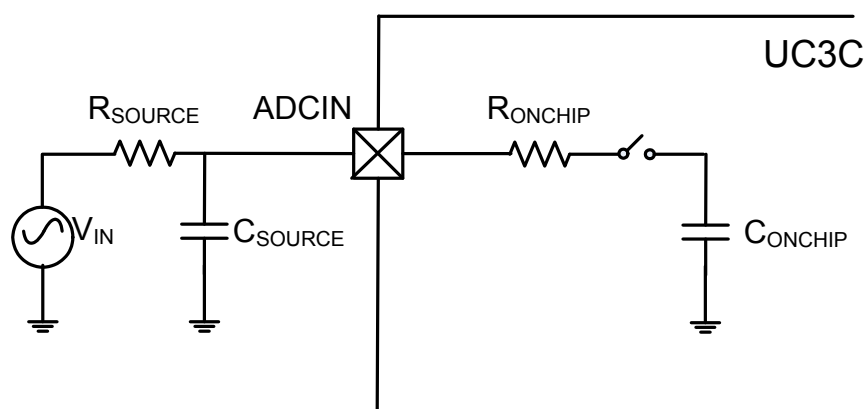


Table 7-31. ADC Transfer Characteristics 12-bit Resolution Mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	Differential mode, $V_{VDDANA} = 3V$, $V_{ADCREFO} = 1V$, $ADCFIA.SEQCFGn.SRES = 0$ ($F_{adc} = 1.2MHz$)			12	Bit
INL	Integral Non-Linearity				6	LSB
DNL	Differential Non-Linearity				5	LSB
	Offset error		-10		10	mV
	Gain error		-30		30	mV

Table 7-31. ADC Transfer Characteristics (Continued) 12-bit Resolution Mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	Differential mode,			12	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 5V$,			5	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 3V$,			4	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 0	-20		20	mV
	Gain error	($F_{adc} = 1.5MHz$)	-30		30	mV

Note: 1. The measures are done without any I/O activity on VDDANA/GNDANA power domain.

Table 7-32. ADC Transfer Characteristics 10-bit Resolution Mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	Differential mode,			10	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 3V$,			1.25	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 1V$,			1.25	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 1	-10		10	mV
	Gain error	($F_{adc} = 1.5MHz$)	-20		20	mV
RES	Resolution	Differential mode,			10	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 5V$,			1.25	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 3V$,			1.25	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 1	-20		20	mV
	Gain error	($F_{adc} = 1.5MHz$)	-25		25	mV

Note: 1. The measures are done without any I/O activity on VDDANA/GNDANA power domain.

Table 7-33. ADC Transfer Characteristics 8-bit Resolution Mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	Differential mode,			8	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 3V$,			0.3	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 1V$,			0.3	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 2	-10		10	mV
	Gain error	($F_{adc} = 1.5MHz$)	-20		20	mV
RES	Resolution	Differential mode,			8	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 5V$,			0.3	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 3V$,			0.25	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 2	-25		25	mV
	Gain error	($F_{adc} = 1.5MHz$)	-25		25	mV

Note: 1. The measures are done without any I/O activity on VDDANA/GNDANA power domain.

Table 7-34. ADC and S/H Transfer Characteristics 12-bit Resolution Mode and S/H gain = 1⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	Differential mode,			12	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 3V$,			6	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 1V$,			5	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 0, S/H gain = 1	-10		10	mV
	Gain error	($F_{adc} = 1.2MHz$)	-30		30	mV
RES	Resolution	Differential mode,			12	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 5V$,			6	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 3V$,			4	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 0, S/H gain = 1	-15		15	mV
	Gain error	($F_{adc} = 1.5MHz$)	-30		30	mV

Note: 1. The measures are done without any I/O activity on VDDANA/GNDANA power domain.

Table 7-35. ADC and S/H Transfer Characteristics 12-bit Resolution Mode and S/H gain from 1 to 8⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	Differential mode,			12	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 3V$,			30	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 1V$,			30	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 0, S/H gain from 1 to 8	-10		10	mV
	Gain error	($F_{adc} = 1.2MHz$)	-25		25	mV
RES	Resolution	Differential mode,			12	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 5V$,			10	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 3V$,			15	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 0, S/H gain from 1 to 8	-20		20	mV
	Gain error	($F_{adc} = 1.5MHz$)	-30		30	mV

Note: 1. The measures are done without any I/O activity on VDDANA/GNDANA power domain

Table 7-36. ADC and S/H Transfer Characteristics 10-bit Resolution Mode and S/H gain from 1 to 16⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	Differential mode,			10	Bit
INL	Integral Non-Linearity	$V_{VDDANA} = 3V$,			4	LSB
DNL	Differential Non-Linearity	$V_{ADCREFO} = 1V$,			4	LSB
	Offset error	ADCFIA.SEQCFGn.SRES = 1, S/H gain from 1 to 16	-15		15	mV
	Gain error	($F_{adc} = 1.5MHz$)	-25		25	mV

Figure 7-4. DAC output

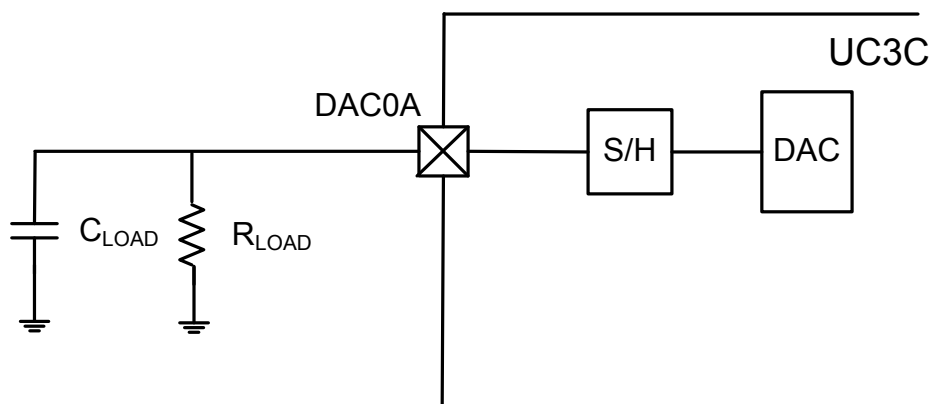


Table 7-40. Transfer Characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	$V_{VDDANA} = 3V$, $V_{DACREF} = 2V$, One S/H			12	Bit
INL	Integral Non-Linearity				20	LSB
DNL	Differential Non-linearity				20	LSB
	Offset error				80	mV
	Gain error				100	mV
RES	Resolution	$V_{VDDANA} = 5V$, $V_{DACREF} = 3V$, One S/H			12	Bit
INL	Integral Non-Linearity				20	LSB
DNL	Differential Non-linearity				20	LSB
	Offset error				120	mV
	Gain error				100	mV

Note: 1. The measures are done without any I/O activity on VDDANA/GNDANA power domain.

7.9.3 USART in SPI Mode Timing

7.9.3.1 Master mode

Figure 7-6. USART in SPI Master Mode With (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

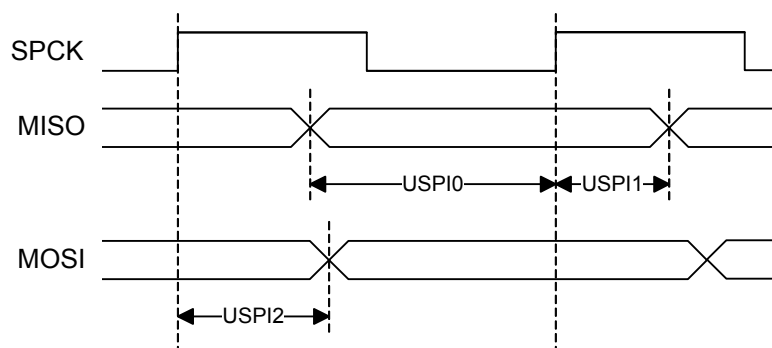


Figure 7-7. USART in SPI Master Mode With (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

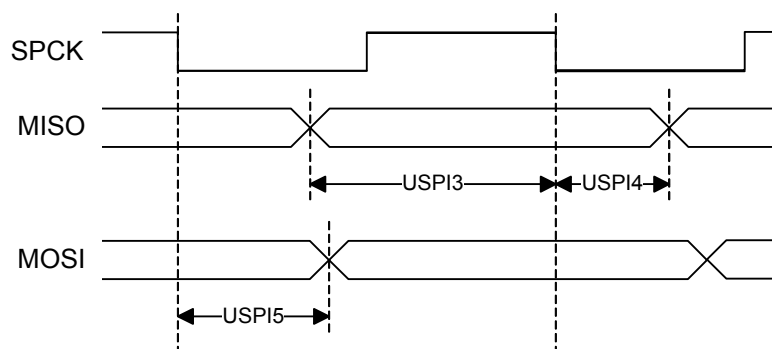


Table 7-46. USART in SPI Mode Timing, Master Mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Units
USPI0	MISO setup time before SPCK rises	external capacitor = 40pF	$27.5 + t_{SAMPLE}^{(2)}$		ns
USPI1	MISO hold time after SPCK rises		0		ns
USPI2	SPCK rising to MOSI delay			12	ns
USPI3	MISO setup time before SPCK falls		$27.5 + t_{SAMPLE}^{(2)}$		ns
USPI4	MISO hold time after SPCK falls		0		ns
USPI5	SPCK falling to MOSI delay			12.5	ns

Note: 1. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left(\left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor \times \frac{1}{2} \right) \times t_{CLKUSART}$

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = \min\left(\frac{f_{CLKSPI} \times 2}{9}, \frac{1}{SPI_{In}}\right)$$

Where SPI_{In} is the MOSI setup and hold time, USPI7 + USPI8 or USPI10 + USPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

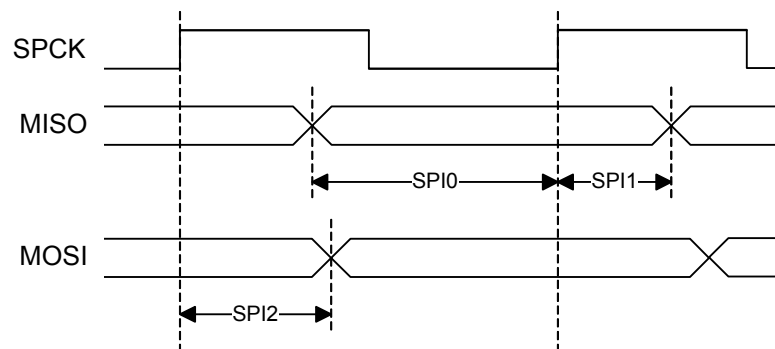
$$f_{SPCKMAX} = \min\left(\frac{f_{CLKSPI} \times 2}{9}, f_{PINMAX}, \frac{1}{SPI_{In} + t_{SETUP}}\right)$$

Where SPI_{In} is the MISO delay, USPI6 or USPI9 depending on CPOL and NCPHA. T_{SETUP} is the SPI master setup time. Please refer to the SPI masterdatasheet for $T_{SETUP} \cdot f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock. f_{PINMAX} is the maximum frequency of the SPI pins. Please refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

7.9.4 SPI Timing

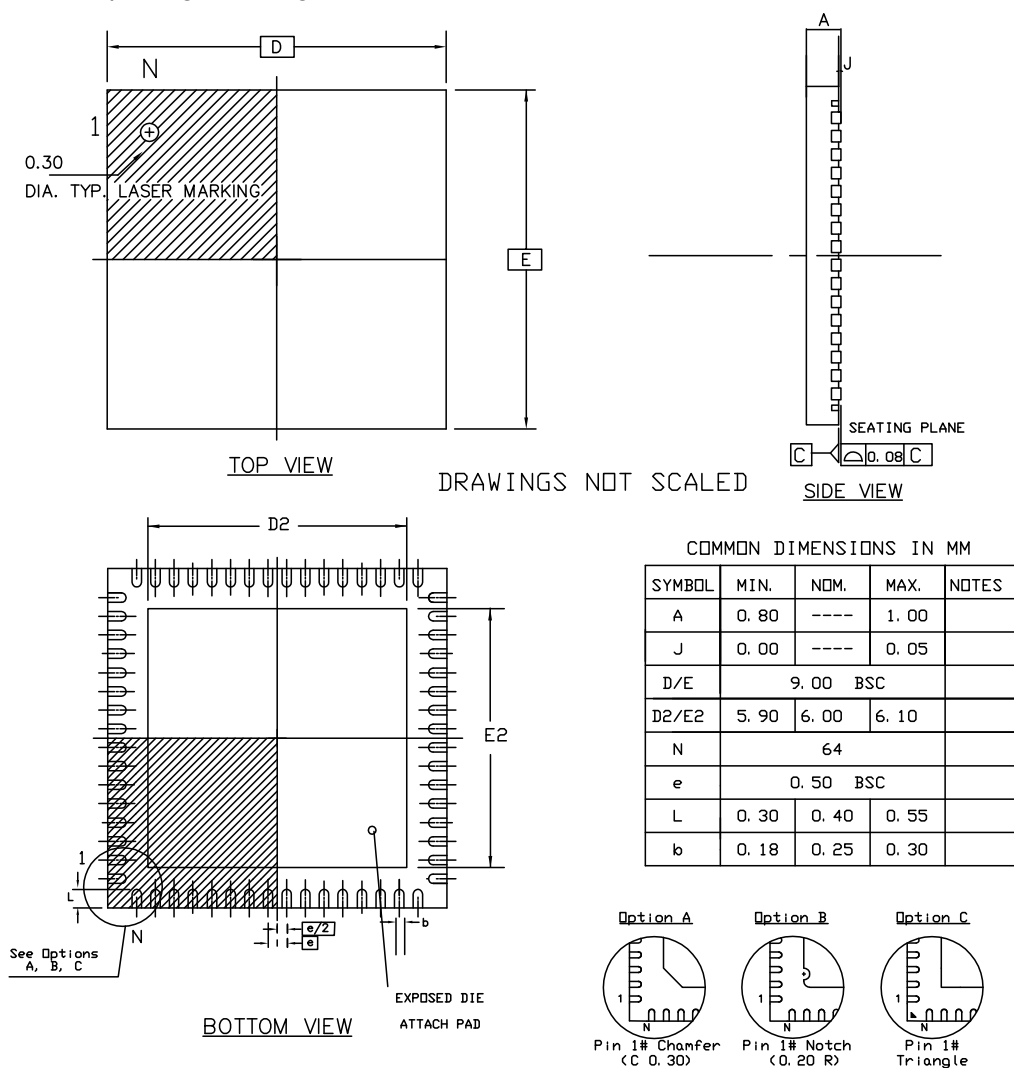
7.9.4.1 Master mode

Figure 7-11. SPI Master Mode With (CPOL= NCPHA= 0) or (CPOL= NCPHA= 1)



8.2 Package Drawings

Figure 8-1. QFN-64 package drawing



Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 8-2. Device and Package Maximum Weight

200	mg
-----	----

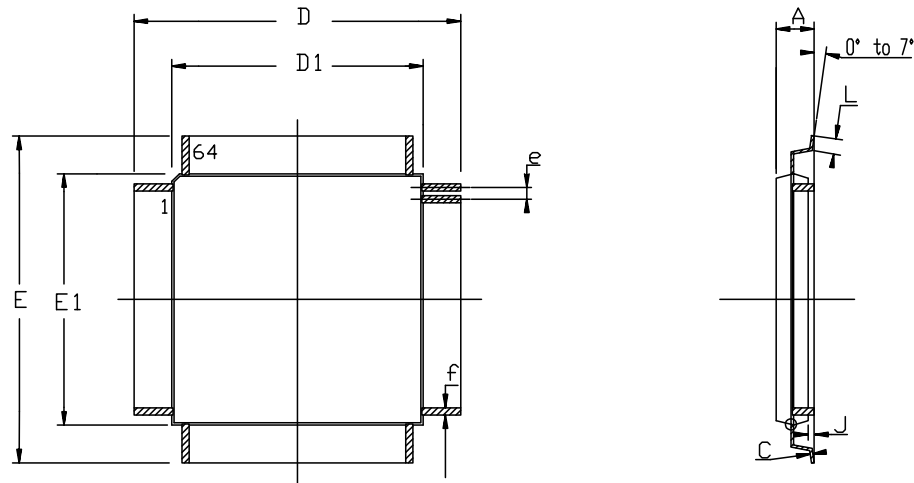
Table 8-3. Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3
----------------------------	-------------------------

Table 8-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 8-2. TQFP-64 package drawing



COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

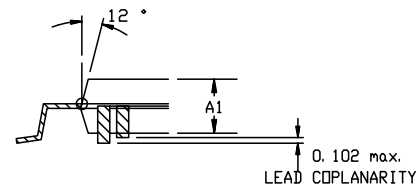


Table 8-5. Device and Package Maximum Weight

300	mg
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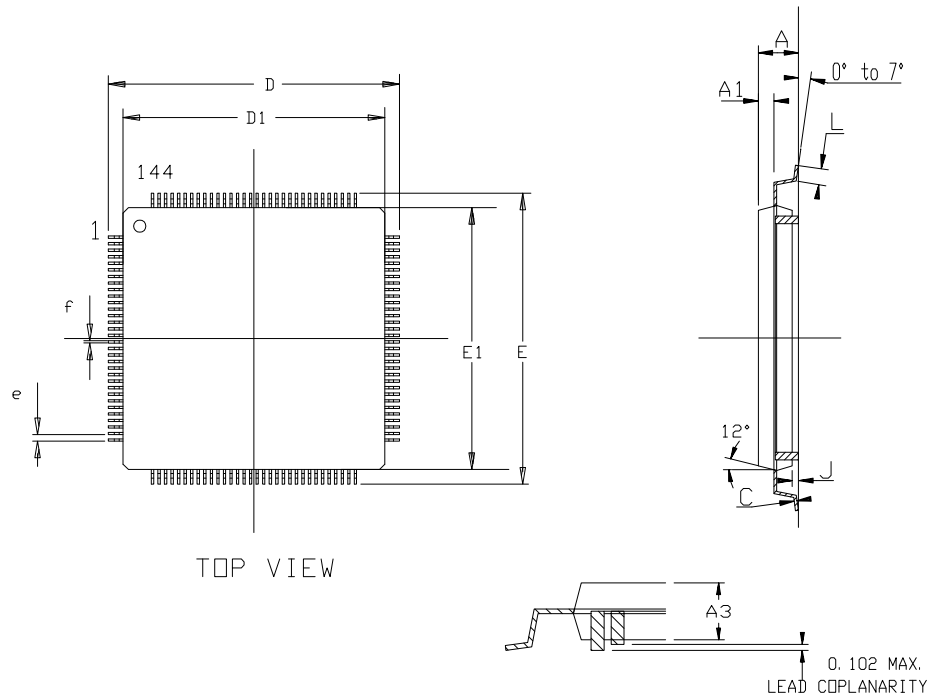
Table 8-6. Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3
----------------------------	-------------------------

Table 8-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 8-4. LQFP-144 package drawing



	Min	MM Nom	Max	Min	INCH Nom	Max
A	–	–	1.60	–	–	.063
C	0.09	–	0.20	.004	–	.008
A3	1.35	1.40	1.45	.053	.055	.057
D	21.90	22.00	22.10	.862	.866	.870
D1	19.90	20.00	20.10	.783	.787	.791
E	21.90	22.00	22.10	.862	.866	.870
E1	19.90	20.00	20.10	.783	.787	.791
J	0.05	–	0.15	.002	–	.006
L	0.45	0.60	0.75	.018	.024	.030
e	0.50 BSC			.0197 BSC		
f	0.22 BSC			.009 BSC		

Table 8-11. Device and Package Maximum Weight

1300	mg
------	----

Table 8-12. Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3
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Table 8-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Fix/Workaround

None.

3 In host mode, the disconnection during OUT transition is not supported

In USB host mode, a pipe can not work if the previous USB device disconnection has occurred during a USB transfer.

Fix/Workaround

Reset the USBC (USBCON.USB=0 and =1) after a device disconnection (UHINT.DDISCI).

4 In USB host mode, entering suspend mode can fail

In USB host mode, entering suspend mode can fail when UHCON.SOF=0 is done just after a SOF reception (UHINT.HSOFI).

Fix/Workaround

Check that UHNUM.FLENHIGH is below 185 in Full speed and below 21 in Low speed before clearing UHCON.SOF.

5 In USB host mode, entering suspend mode for low speed device can fail when the USB freeze (USBCON.FRZCLK=1) is done just after UHCON.SOF=0.**Fix/Workaround**

When entering suspend mode (UHCON.SOF is cleared), check that USBFSM.DRDSTATE is not equal to three before freezing the clock (USBCON.FRZCLK=1).

10.1.11 WDT**1 WDT Control Register does not have synchronization feedback**

When writing to the Timeout Prescale Select (PSEL), Time Ban Prescale Select (TBAN), Enable (EN), or WDT Mode (MODE) fields of the WDT Control Register (CTRL), a synchronizer is started to propagate the values to the WDT clock domain. This synchronization takes a finite amount of time, but only the status of the synchronization of the EN bit is reflected back to the user. Writing to the synchronized fields during synchronization can lead to undefined behavior.

Fix/Workaround

-When writing to the affected fields, the user must ensure a wait corresponding to 2 clock cycles of both the WDT peripheral bus clock and the selected WDT clock source.

-When doing writes that changes the EN bit, the EN bit can be read back until it reflects the written value.

- 4 SCIF: Added VREGCR register
- 5 AST: Updated digital tuner formula
- 6 SDRAMC: cleaned-up SDCS/NCS names. Added VERSION register
- 7 SAU: Updated SR.IDLE
- 8 USART: Updated
- 9 CANIF: Updated address map figure
- 10 USBC: Updated
- 11 DACIFB: Updated
- 12 Programming and Debugging: Added JTAG Data Registers section
- 13 Electrical Characteristics: Updated
- 14 Ordering Information: Updated
- 15 Errata: Updated

11.4 Rev. A – 10/10

- 1 Initial revision

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