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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604bamll6

Table 1. MPC5604B/C device comparison[1] (continued)

Feature	Device															
	MPC5602BxLH	MPC5602BxLL	MPC5602BxLQ	MPC5602CxLH	MPC5602CxLL	MPC5603BxLH	MPC5603BxLL	MPC5603BxLQ	MPC5603CxLH	MPC5603CxLL	MPC5604BxLH	MPC5604BxLL	MPC5604BxLQ	MPC5604CxLH	MPC5604CxLL	MPC5604BxMG
• PWM + IC/OC[4]	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	40 ch
• IC/OC[4]	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	6 ch
SCI (LINFlex)	3[5]			4												
SPI (DSPI)	2	3		2	3	2	3		2	3	2	3		2	3	
CAN (FlexCAN)	2[6]			5	6	3[7]			5	6	3[7]			5	6	
I^2C	1															
32 kHz oscillator	Yes															
GPIO[8]	45	79	123	45	79	45	79	123	45	79	45	79	123	45	79	123
Debug	JTAG															Nexus2+
Package	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	208 MAPBGA[9]

1 Feature set dependent on selected peripheral multiplexing—table shows example implementation.

2 Based on 125 °C ambient operating temperature.

3 See the eMIOS section of the device reference manual for information on the channel configuration and functions.

4 IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter.

5 SCI0, SCI1 and SCI2 are available. SCI3 is not available.

6 CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.

7 CAN0, CAN3 and either CAN1 or CAN4 are available. CAN2, CAN5 and CAN6 are not available

8 I/O count based on multiplexing with peripherals.

9 208 MAPBGA available only as development package for Nexus2+.

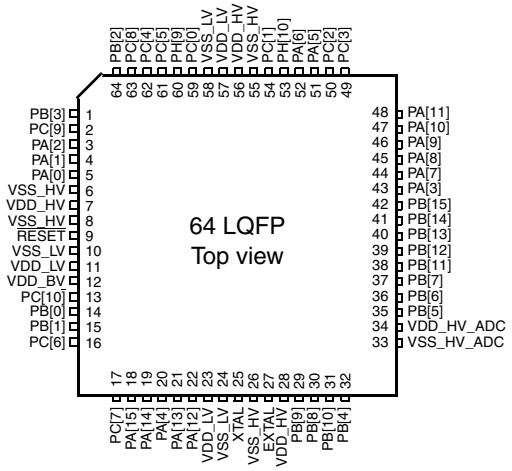


Figure 2. MPC560xB LQFP 64-pin configuration

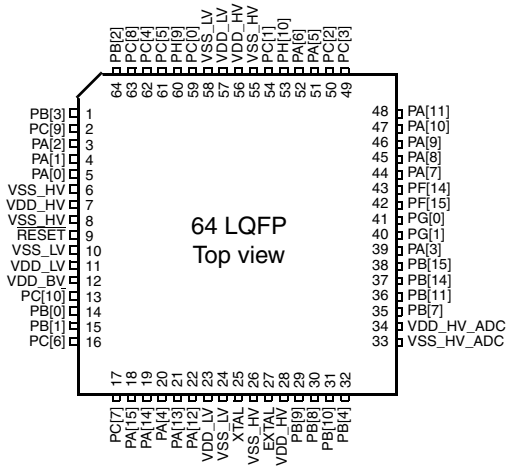


Figure 3. MPC560xC LQFP 64-pin configuration

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ANS[0] OSC32K_XTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	30	30	39	53	R9
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ANS[1] OSC32K_EXTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	29	29	38	52	T9
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ANS[2] WKPU[8][4]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	31	40	54	P9
PB[11][8]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	36	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	—	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	—	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	37	65	87	L16

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	38	67	89	L13
PC[0][9]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	59	87	126	A8
PC[1][9]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO[10] —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	54	82	121	C9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX[11] — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M	Tristate	50	50	78	117	A11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX[11] EIRQ[6]	SIUL DSPI_1 ADC — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O — I I I	S	Tristate	49	49	77	116	B11
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 CAN3RX[11]	SIUL — — — DSPI_1 FlexCAN_3	I/O — — — I I	M	Tristate	62	62	92	131	B7
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX[11] — EIRQ[7]	SIUL DSPI1 FlexCAN_3 — SIUL	I/O O O — I	M	Tristate	61	61	91	130	A7
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	16	25	36	R2

2.8 Electrical characteristics

2.9 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

2.10 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 7 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 7. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

2.14 Thermal characteristics

2.14.1 Package thermal characteristics

Table 14. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[3]	Single-layer board - 1s	64	60	°C/W
					100	64	
					144	64	
				Four-layer board - 2s2p	64	42	
					100	51	
					144	49	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[4]	Single-layer board - 1s	64	24	°C/W
					100	36	
					144	37	
				Four-layer board - 2s2p	64	24	
					100	34	
					144	35	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case[5]	Single-layer board - 1s	64	11	°C/W
					100	22	
					144	22	
				Four-layer board - 2s2p	64	11	
					100	22	
					144	22	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	33	
					144	34	
				Four-layer board - 2s2p	64	TBD	
					100	34	
					144	35	

Table 22. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 23 provides the weight of concurrent switching I/Os.

Due to the dynamic current limitations, the sum of the weight of concurrent switching I/Os on a single segment must not exceed 100% to ensure device functionality.

Table 23. I/O weight[1]

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP[2]		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
4	4	3	PB[3]	10%	—	12%	—	10%	—	12%	—
			PC[9]	10%	—	12%	—	10%	—	12%	—
		—	PC[14]	9%	—	11%	—	—	—	—	—
		—	PC[15]	9%	13%	11%	12%	—	—	—	—
	—	—	PG[5]	9%	—	11%	—	—	—	—	—
	—	—	PG[4]	9%	12%	10%	11%	—	—	—	—
	—	—	PG[3]	9%	—	10%	—	—	—	—	—
4	—	—	PG[2]	8%	12%	10%	10%	—	—	—	—
	4	3	PA[2]	8%	—	9%	—	8%	—	9%	—
		—	PE[0]	8%	—	9%	—	—	—	—	—
		3	PA[1]	7%	—	9%	—	7%	—	9%	—
		—	PE[1]	7%	10%	8%	9%	—	—	—	—
		—	PE[8]	7%	9%	8%	8%	—	—	—	—
		—	PE[9]	6%	—	7%	—	—	—	—	—
		—	PE[10]	6%	—	7%	—	—	—	—	—
		3	PA[0]	5%	8%	6%	7%	5%	8%	6%	7%
		—	PE[11]	5%	—	6%	—	—	—	—	—

Table 23. I/O weight[1] (continued)

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP[2]		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	6%	—	7%	—	6%	—	7%	—
	—	—	PF[0]	6%	—	7%	—	—	—	—	—
	—	—	PF[1]	7%	—	8%	—	—	—	—	—
	—	—	PF[2]	7%	—	8%	—	—	—	—	—
	—	—	PF[3]	7%	—	9%	—	—	—	—	—
	—	—	PF[4]	8%	—	9%	—	—	—	—	—
	—	—	PF[5]	8%	—	10%	—	—	—	—	—
	—	—	PF[6]	8%	—	10%	—	—	—	—	—
	—	—	PF[7]	9%	—	10%	—	—	—	—	—
	2	—	PD[0]	1%	—	1%	—	—	—	—	—
		—	PD[1]	1%	—	1%	—	—	—	—	—
		—	PD[2]	1%	—	1%	—	—	—	—	—
		—	PD[3]	1%	—	1%	—	—	—	—	—
		—	PD[4]	1%	—	1%	—	—	—	—	—
		—	PD[5]	1%	—	1%	—	—	—	—	—
		—	PD[6]	1%	—	1%	—	—	—	—	—
		—	PD[7]	1%	—	1%	—	—	—	—	—
		—	PD[8]	1%	—	1%	—	—	—	—	—
		2	PB[4]	1%	—	1%	—	1%	—	1%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
		—	PD[9]	1%	—	1%	—	—	—	—	—
		—	PD[10]	1%	—	1%	—	—	—	—	—
		—	PD[11]	1%	—	1%	—	—	—	—	—
		2	PB[11]	11%	—	13%	—	17%	—	21%	—
		—	PD[12]	11%	—	13%	—	—	—	—	—
		2	PB[12]	11%	—	13%	—	18%	—	21%	—
		—	PD[13]	10%	—	12%	—	—	—	—	—

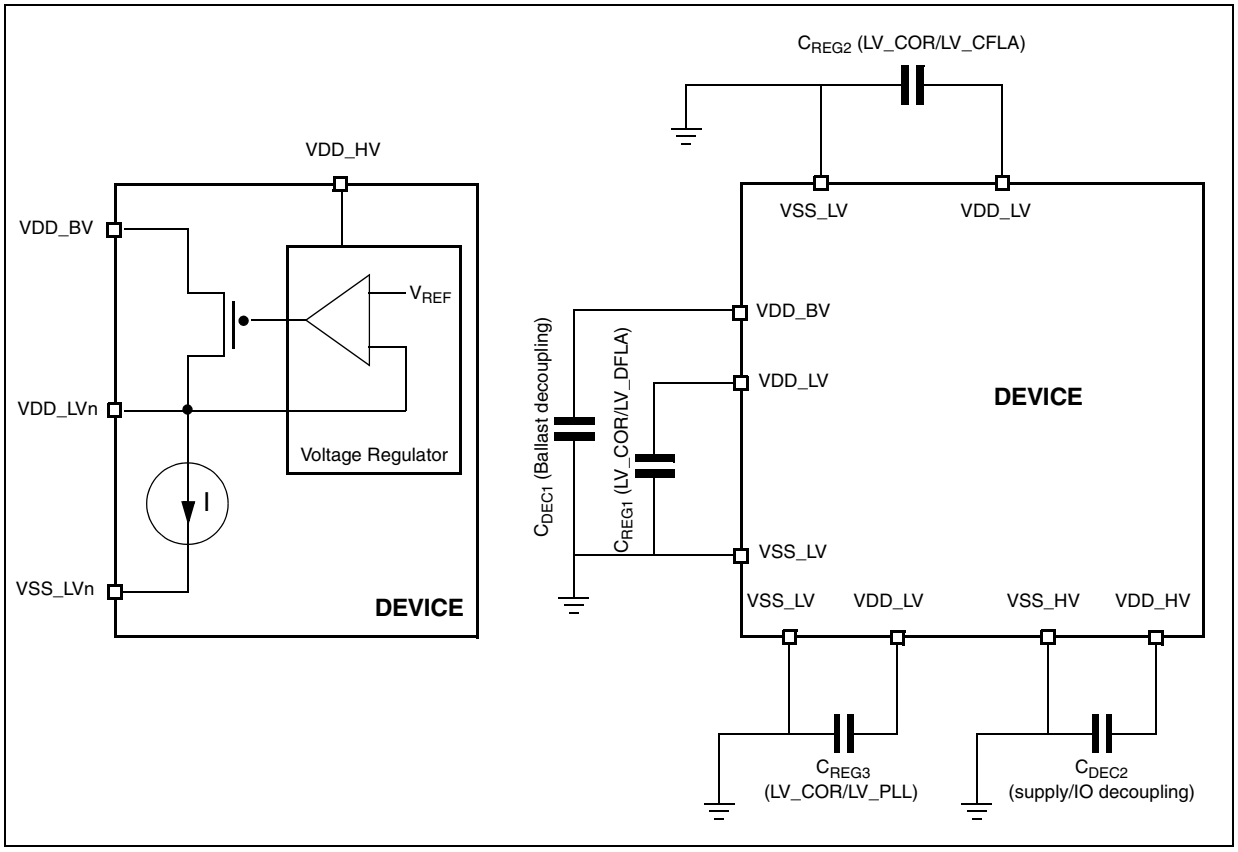


Figure 10. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see 2.13, Recommended operating conditions).

The internal voltage regulator requires a controlled slew rate of both V_{DD_HV} and V_{DD_BV} as described in Figure 11.

2.20.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations: The software flowchart must include the management of runaway conditions such as:
  - — Corrupted program counter
  - — Unexpected reset
  - — Critical data corruption (control registers...)
- Prequalification trials: Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

2.20.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

Table 33. EMI radiated emission measurement[1,2]

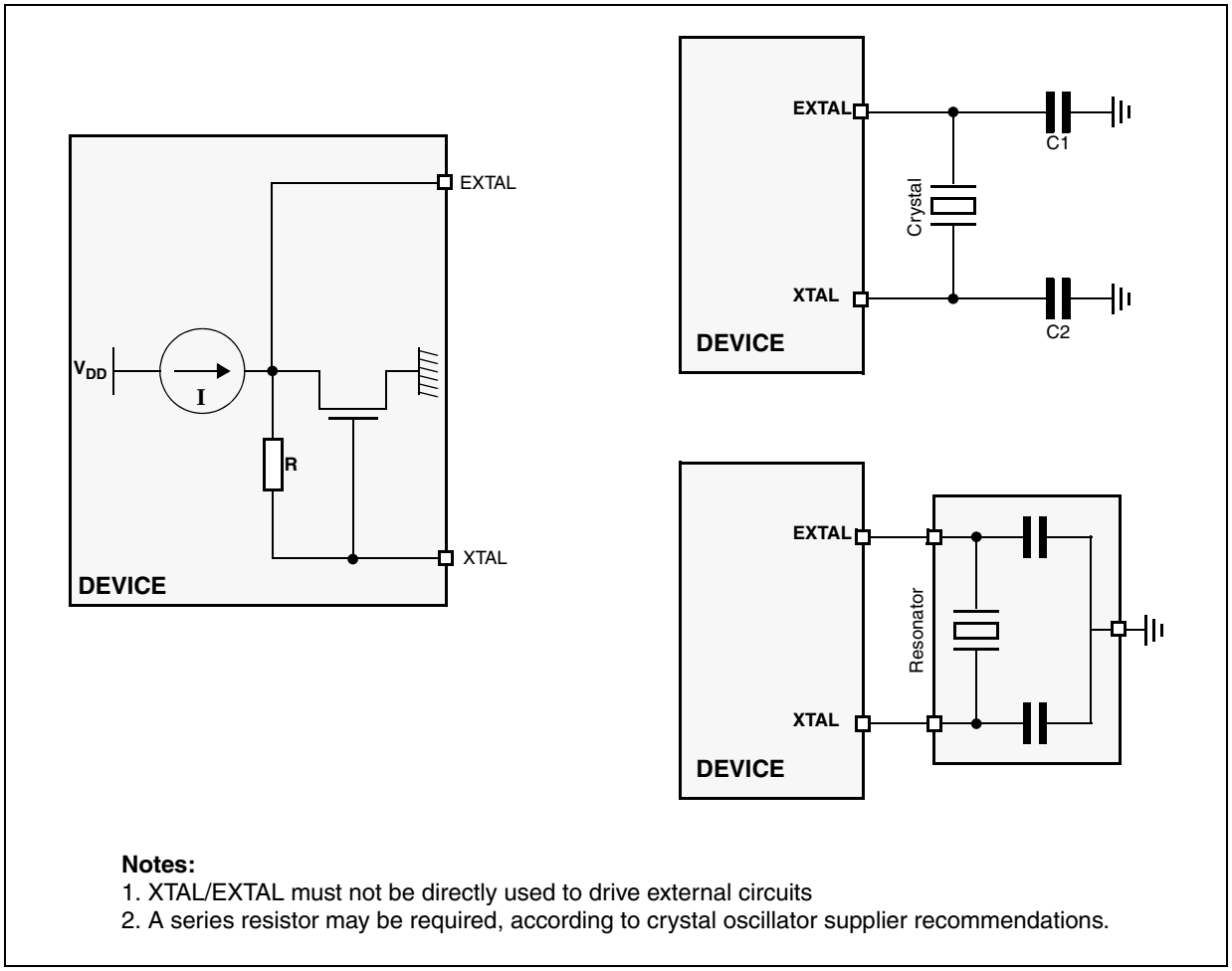
Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150	—	1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBµV
					±2% PLL frequency modulation	—	—	14	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

2.20.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.



Notes:
1. XTAL/EXTAL must not be directly used to drive external circuits
2. A series resistor may be required, according to crystal oscillator supplier recommendations.

Figure 14. Crystal oscillator and resonator connection scheme

Table 36. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

3 Maximum ESR (R_m) of the crystal is 50 kΩ

4 C0 includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins

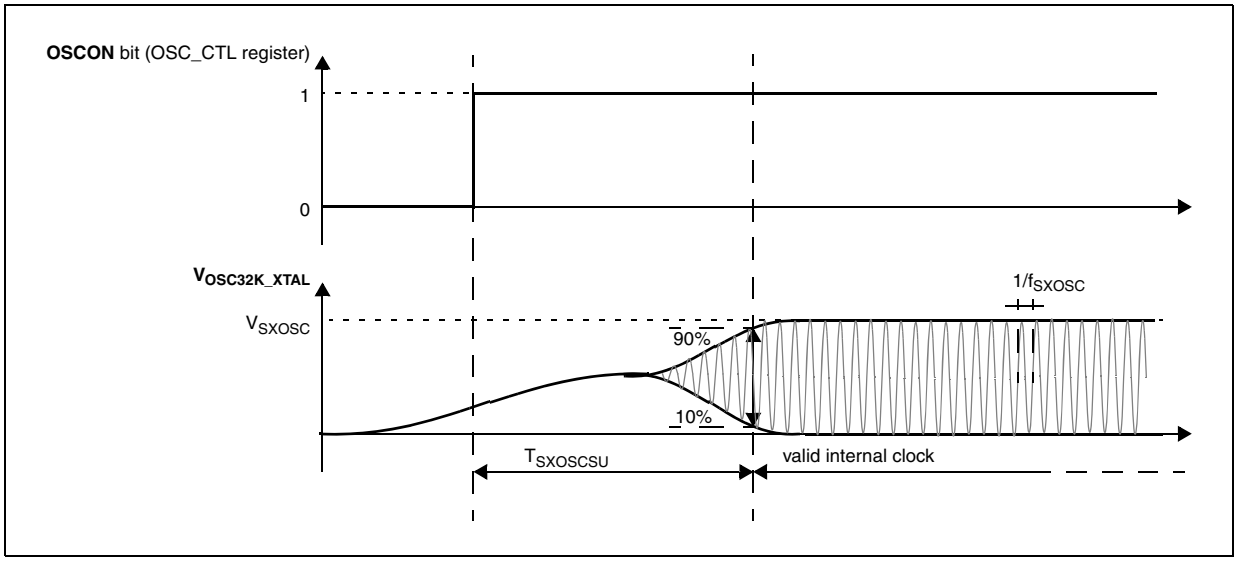


Figure 18. Slow external crystal oscillator (32 kHz) timing diagram

Table 39. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	—	2.5	—	µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2^2	s

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified. Values are specified for no neighbor GPIO pin activity. If oscillator is enabled (OSC32K_XTAL and OSC32K_EXTAL pins), neighboring pins should not toggle.

2 Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

2.23 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

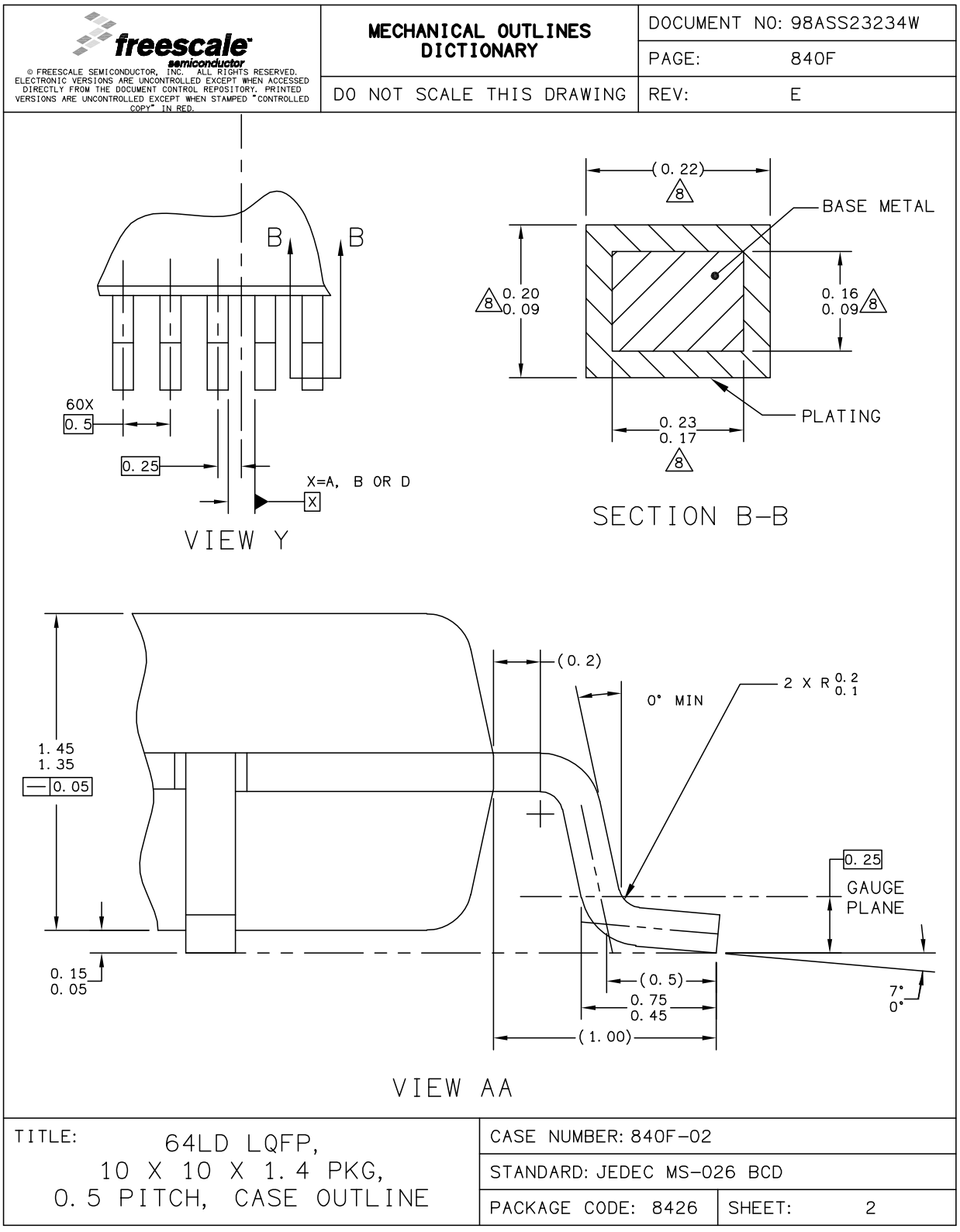


Figure 36. 64 LQFP package mechanical drawing (2 of 3)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

Figure 37. 64 LQFP package mechanical drawing (3 of 3)

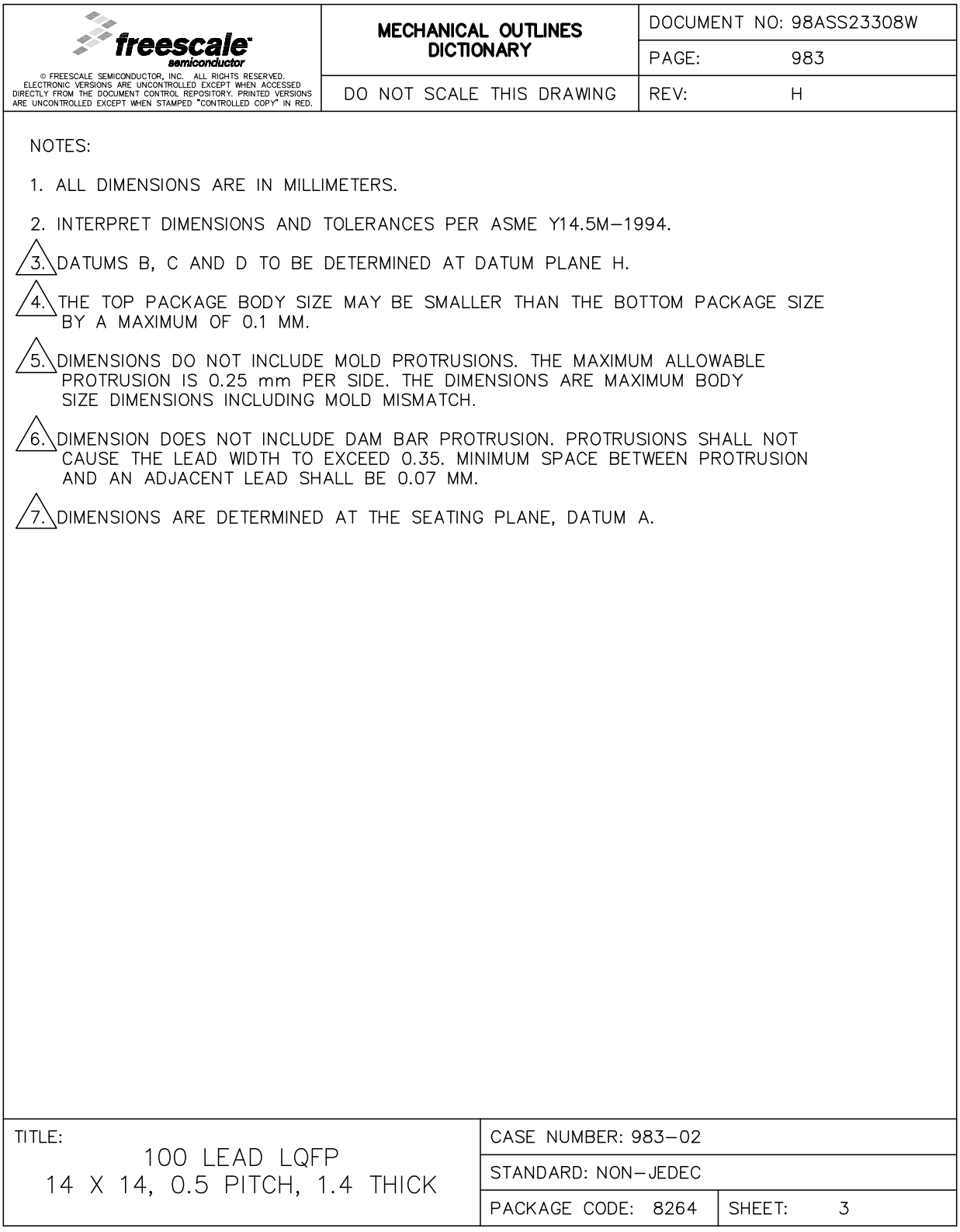
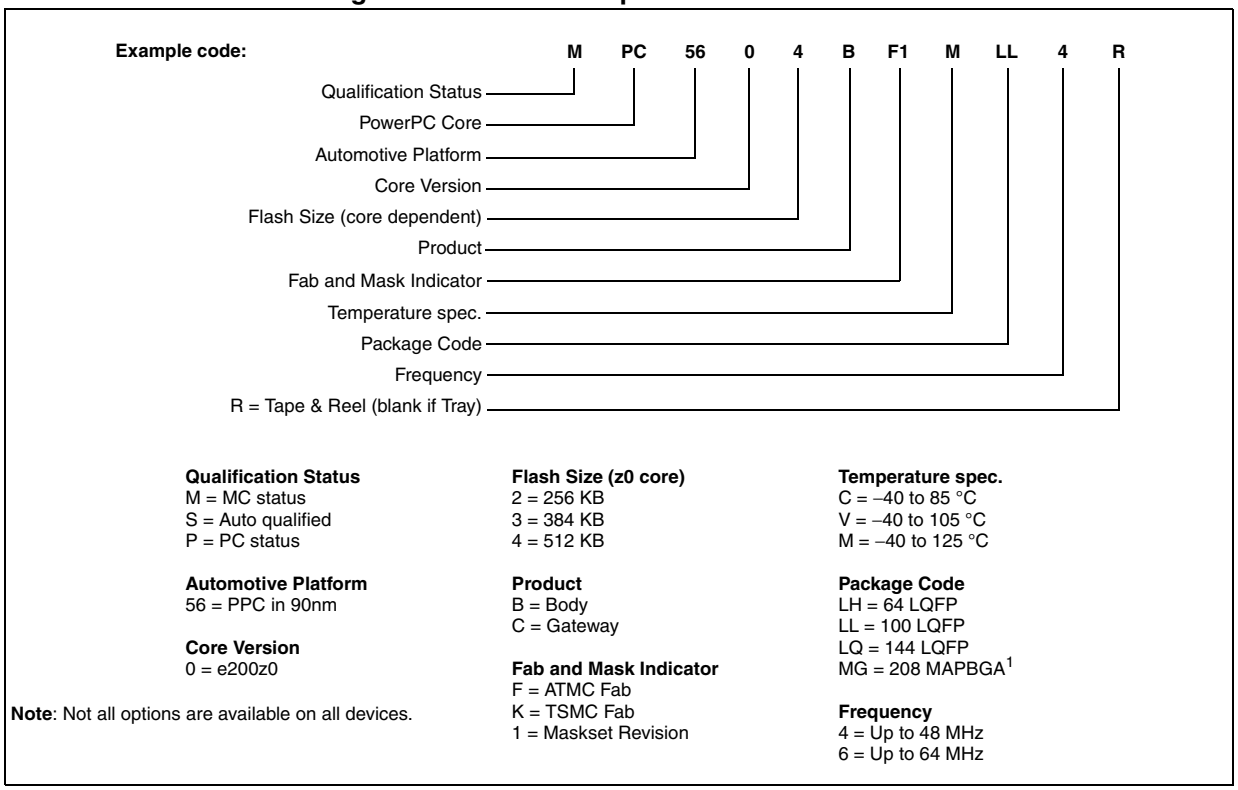


Figure 40. 100 LQFP package mechanical drawing (3 of 3)

4 Ordering information

Figure 45. Commercial product code structure



[1] 208 MAPBGA available only as development package for Nexus2+

5 Document revision history

Table 49 summarizes revisions to this document.

Table 49. Revision history

Revision	Date	Description of Changes
1	04-Apr-2008	Initial release.

Table 49. Revision history (continued)

Revision	Date	Description of Changes
2 (cont.)	06-Mar-2009	Updated Table 15, Table 16, Table 17, Table 18 and Table 19 Added 2.15.4, Output pin transition times Updated Table 22 Updated Figure 8 Updated Table 24 2.17.1, Voltage regulator electrical characteristics: Amended description of LV_PLL Figure 10: Exchanged position of symbols C_{DEC1} and C_{DEC2} Updated Table 25 Added Figure 13 Updated Table 26 and Table 27 Updated 2.19, Flash memory electrical characteristics Added 2.20, Electromagnetic compatibility (EMC) characteristics Updated 2.21, Fast external crystal oscillator (4 to 16 MHz) electrical characteristics Updated 2.22, Slow external crystal oscillator (32 kHz) electrical characteristics Updated Table 40, Table 41 and Table 42 Added 2.27, On-chip peripherals Added Table 43 Updated Table 44 Updated Table 47 Added Appendix A, Abbreviations
4	06-Aug-2009	Updated Figure 6 Table 11 • V_{DD_ADC}: changed min value for “relative to V_{DD}” condition • V_{IN}: changed min value for “relative to V_{DD}” condition • I_{CORELV}: added new row Table 13 • $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$: added new rows • Changed capacitance value in footnote Table 20 • MEDIUM configuration: added condition for PAD3V5V = 0 Updated Figure 10 Table 25 • C_{DEC1}: changed min value • $I_{MREG:}$ changed max value • I_{DD_BV}: added max value footnote Table 26 • $V_{LVDHV3H}$: changed max value • $V_{LVDHV3L}$: added max value • $V_{LVDHV5H}$: changed max value • $V_{LVDHV5L}$: added max value Updated Table 27 Table 29 • Retention: deleted min value footnote for “Blocks with 100,000 P/E cycles“ Table 37 • I_{FXOSC}: added typ value Table 39 • V_{SXOSC}: changed typ value • $T_{SXOSCSU}$: added max value footnote Table 40 • Δt_{LTJIT}: added max value Updated Figure 38

Table 49. Revision history (continued)

Revision	Date	Description of Changes
5	02-Nov-2009	In the “MPC5604B/C series block summary” table, added a new row. In the “Absolute maximum ratings” table, changed max value of V_{DD_BV}, V_{DD_ADC}, and V_{IN}. In the “Recommended operating conditions (3.3 V)” table, deleted min value of TV_{DD}. In the “Reset electrical characteristics” table, changed footnotes 3 and 5. In the “Voltage regulator electrical characteristics” table: • C_{REGn}: changed max value. • C_{DEC1}: split into 2 rows. • Updated voltage values in footnote 4 In the “Low voltage monitor electrical characteristics” table: • Updated column Conditions. • $V_{LVDLVCORL}$, $V_{LVDLVBKPL}$: changed min/max value. In the “Program and erase specifications” table, added initial max value of $T_{dwprogram}$. In the “Flash module life” table, changed min value for blocks with 100K P/E cycles In the “Flash power supply DC electrical characteristics” table: • I_{FREAD}, I_{FMOD}: added typ value. • Added footnote 1. Added *“NVUSRO[WATCHDOG_EN] field description” section.* *Section 4.18: “ADC electrical characteristics”* has been moved up in hierarchy (it was Section 4.18.5). In the “ADC conversion characteristics” table, changed initial max value of R_{AD}. In the “On-chip peripherals current consumption” table: • Removed min/max from the heading. • Changed unit of measurement and consequently rounded the values.

Table 49. Revision history (continued)

Revision	Date	Description of Changes
6	15-Mar-2010	In the “Introduction” section, relocated a note. In the “MPC5604B/C device comparison” table, added footnote regarding SCI and CAN. In the “Absolute maximum ratings” table, removed the min value of V_{IN} relative to V_{DD}. In the “Recommended operating conditions (3.3 V)” table: • $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$: added new rows. • TV_{DD}: made single row. In the “LQFP thermal characteristics” table, added more rows. Removed “208 MAPBGA thermal characteristics” table. In the “I/O consumption” table: • Removed I_{DYNSEG} row. • Added “I/O weight” table. In the “Voltage regulator electrical characteristics” table: • Updated the values. • Removed $I_{VREGREF}$ and $I_{VREDLVD12}$. • Added a note about I_{DD_BC}. In the “Low voltage monitor electrical characteristics” table: • Updated V_{PORH} values. • Updated $V_{LVDLVCORL}$ value. Entirely updated the “Low voltage power domain electrical characteristics” table. In the “Program and erase specifications” table, inserted T_{eslat} row. Entirely updated the “Flash power supply DC electrical characteristics” table. Entirely updated the “Start-up time/Switch-off time” table. In the “Crystal oscillator and resonator connection scheme” figure, relocated a note. In the “Slow external crystal oscillator (32 kHz) electrical characteristics” table: • Removed g_{mSXOSC} row. • Inserted values of $I_{SXOSCBIAS}$. Entirely updated the “Fast internal RC oscillator (16 MHz) electrical characteristics” table. In the “ADC conversion characteristics” table: updated the description of the conditions of t_{ADC_PU} and t_{ADC_S}. Entirely updated the “DSPI characteristics” table. In the “Orderable part number summary” table, modified some orderable part number. Updated the “Commercial product code structure” figure. Removed the note about the condition from “Flash read access timing” table Removed the notes that assert the values need to be confirmed before validation Exchanged the order of “LQFP 100-pin configuration” and “LQFP 144-pin configuration” Exchanged the order of “LQFP 100-pin package mechanical drawing” and “LQFP 144-pin package mechanical drawing”

Table 49. Revision history (continued)

Revision	Date	Description of Changes
9	16 June 2011	Formatting and minor editorial changes throughout Harmonized oscillator nomenclature Removed all instances of note “All 64 LQFP information is indicative and must be confirmed during silicon validation.” Device comparison table: changed temperature value in footnote 2 from 105 °C to 125 °C MPC560xB LQFP 64-pin configuration and MPC560xC LQFP 64-pin configuration: renamed pin 6 from VPP_TEST to VSS_HV Removed “Pin Muxing” section; added sections “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins,” “Functional ports”, and “Nexus 2+ pins” Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V): updated conditions for ambient and junction temperature characteristics I/O input DC electrical characteristics: updated I_{LKG} characteristics Section “I/O pad current specification”: removed content referencing the I_{DYNSEG} maximum value I/O consumption: replaced instances of “Root medium square” with “Root mean square” I/O weight: replaced instances of bit “SRE” with “SRC”; added pads PH[9] and PH[10]; added supply segments; removed weight values in 64-pin LQFP for pads that do not exist in that package Reset electrical characteristics: updated parameter classification for $\|I_{WPU}\|$ Updated Voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$; replaced “LVD_DIGBKP” with “LVDLVBKP” in note Updated section “Power consumption” Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$ Crystal oscillator and resonator connection scheme: added footnote about possibility of adding a series resistor Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1 FMPLL electrical characteristics: added short term jitter characteristics; inserted “—” in empty min value cell of t_{lock} row Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 11 ADC input leakage current: updated I_{LKG} characteristics ADC conversion characteristics: updated symbols On-chip peripherals current consumption: changed “supply current on “$V_{DD\_HV\_ADC}$” to “supply current on” V_{DD_HV}” in $I_{DD\_HV(FLASH)}$ row; updated $I_{DD\_HV(PLL)}$ value—was 3 * f_{periph}, is 30 * f_{periph}; updated footnotes DSPI characteristics: added rows t_{PCSC} and t_{PASC} Added DSPI PCS strobe (PCSS) timing diagram