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Details

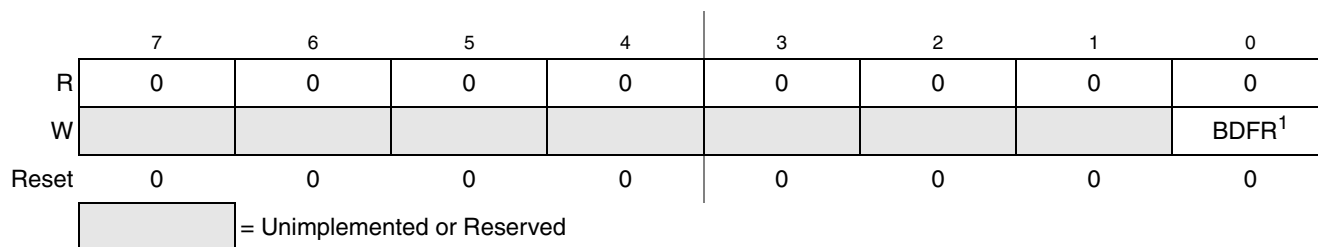
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08ac8mfde

Table 5-4. SRS Register Field Descriptions (continued)

Field	Description
3 ILAD	<p>Illegal Address — Reset was caused by an attempt to access a designated illegal address.</p> <p>0 Reset not caused by an illegal address access. 1 Reset caused by an illegal address access.</p> <p>Illegal address areas in the MC9S08AC16 are: 0x0470 - 0x17FF — Gap from end of RAM to start of high page registers 0x1860 - 0xBFFF — Gap from end of high page registers to start of Flash memory</p> <p>Unused and reserved locations in register areas are not considered illegal addresses and do not trigger illegal address resets.</p>
2 ICG	<p>Internal Clock Generation Module Reset — Reset was caused by an ICG module reset.</p> <p>0 Reset not caused by ICG module. 1 Reset caused by ICG module.</p>
1 LVD	<p>Low Voltage Detect — If the LVDRE and LVDSE bits are set and the supply drops below the LVD trip voltage, an LVD reset will occur. This bit is also set by POR.</p> <p>0 Reset not caused by LVD trip or POR. 1 Reset caused by LVD trip or POR.</p>

5.9.3 System Background Debug Force Reset Register (SBD FR)

This register contains a single write-only control bit. A serial background command such as WRITE_BYTE must be used to write to SBD FR. Attempts to write this register from a user program are ignored. Reads always return 0x00.



¹ BDFR is writable only through serial background debug commands, not from user programs.

Figure 5-4. System Background Debug Force Reset Register (SBD FR)
Table 5-5. SBD FR Register Field Descriptions

Field	Description
0 BDFR	<p>Background Debug Force Reset — A serial background command such as WRITE_BYTE may be used to allow an external debug host to force a target system reset. Writing logic 1 to this bit forces an MCU reset. This bit cannot be written from a user program.</p>

5.9.9 System Power Management Status and Control 2 Register (SPMSC2)

This register is used to report the status of the low voltage warning function, and to configure the stop mode behavior of the MCU.

	7	6	5	4	3	2	1	0
R	LVWF	0	LVDV	LVWV	PPDF	0		PPDC ¹
W		LVWACK						
Power-on reset:	0 ⁽²⁾	0	0	0	0	0	0	0
LVD reset:	0 ⁽²⁾	0	U	U	0	0	0	0
Any other reset:	0 ⁽²⁾	0	U	U	0	0	0	0

= Unimplemented or Reserved
 U = Unaffected by reset

¹ This bit can be written only one time after reset. Additional writes are ignored.

² LVWF will be set in the case when V_{Supply} transitions below the trip point or after reset and V_{Supply} is already below V_{LVW} .

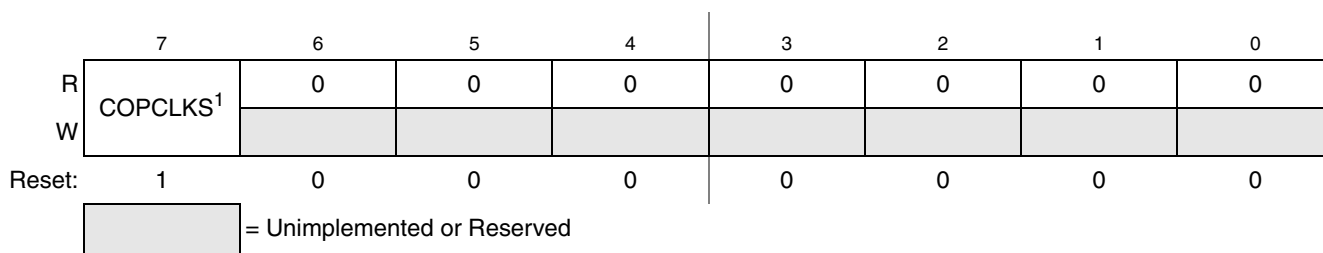
Figure 5-11. System Power Management Status and Control 2 Register (SPMSC2)

Table 5-13. SPMSC2 Register Field Descriptions

Field	Description
7 LVWF	Low-Voltage Warning Flag — The LVWF bit indicates the low voltage warning status. 0 Low voltage warning not present. 1 Low voltage warning is present or was present.
6 LVWACK	Low-Voltage Warning Acknowledge — The LVWACK bit is the low-voltage warning acknowledge. Writing a 1 to LVWACK clears LVWF to a 0 if a low voltage warning is not present.
5 LVDV	Low-Voltage Detect Voltage Select — The LVDV bit selects the LVD trip point voltage (V_{LVD}). 0 Low trip point selected ($V_{LVD} = V_{LVDDL}$). 1 High trip point selected ($V_{LVD} = V_{LVDDH}$).
4 LVWV	Low-Voltage Warning Voltage Select — The LVWV bit selects the LVW trip point voltage (V_{LVW}). 0 Low trip point selected ($V_{LVW} = V_{LVWDL}$). 1 High trip point selected ($V_{LVW} = V_{LVWDH}$).
3 PPDF	Partial Power Down Flag — The PPDF bit indicates that the MCU has exited the stop2 mode. 0 Not stop2 mode recovery. 1 Stop2 mode recovery.
2 PPDACK	Partial Power Down Acknowledge — Writing a 1 to PPDACK clears the PPDF bit.
0 PPDC	Partial Power Down Control — The write-once PPDC bit controls whether stop2 or stop3 mode is selected. 0 Stop3 mode enabled. 1 Stop2, partial power down, mode enabled.

5.9.10 System Options Register 2 (SOPT2)

This high page register contains bits to configure MCU specific features on the MC9S08AC16 Series devices.



¹ This bit can be written only one time after reset. Additional writes are ignored.

Figure 5-12. System Options Register 2 (SOPT2)

Table 5-14. SOPT2 Register Field Descriptions

Field	Description
7 COPCLKS	COP Watchdog Clock Select — This write-once bit selects the clock source of the COP watchdog. 0 Internal 1-kHz clock is source to COP. 1 Bus clock is source to COP.

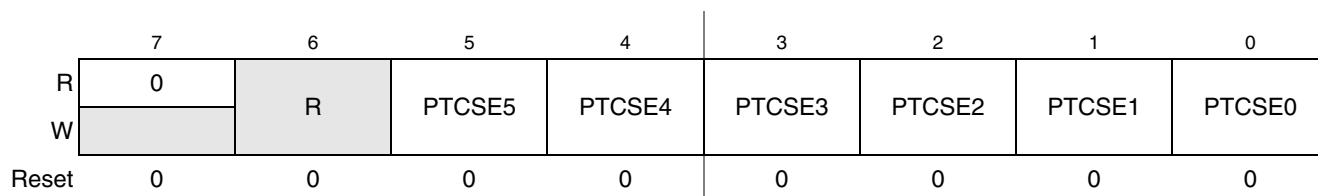


Figure 6-23. Output Slew Rate Control Enable for Port C (PTCSE)¹

¹ Bit 6 is a reserved bit that must always be written to 0.

Table 6-14. PTCSE Register Field Descriptions

Field	Description
5:0 PTCSE[5:0]	<p>Output Slew Rate Control Enable for Port C Bits — Each of these control bits determine whether output slew rate control is enabled for the associated PTC pin. For port C pins that are configured as inputs, these bits have no effect.</p> <p>0 Output slew rate control disabled for port C bit n. 1 Output slew rate control enabled for port C bit n.</p>

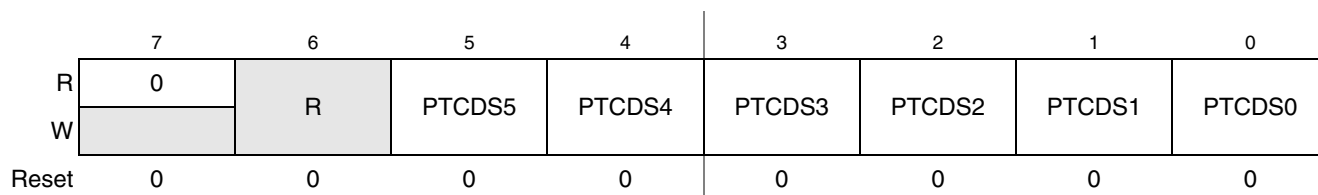


Figure 6-24. Output Drive Strength Selection for Port C (PTCDS)¹

¹ Bit 6 is a reserved bit that must always be written to 0.

Table 6-15. PTCDS Register Field Descriptions

Field	Description
5:0 PTCDS[5:0]	<p>Output Drive Strength Selection for Port C Bits — Each of these control bits selects between low and high output drive for the associated PTC pin.</p> <p>0 Low output drive enabled for port C bit n. 1 High output drive enabled for port C bit n.</p>

8.1 Introduction

The ICG provides multiple options for clock sources. This offers a user great flexibility when making choices between cost, precision, current draw, and performance. As seen in Figure 8-3, the ICG consists of four functional blocks. Each of these is briefly described here and then in more detail in a later section.

- **Oscillator block** — The oscillator block provides means for connecting an external crystal or resonator. Two frequency ranges are software selectable to allow optimal startup and stability. Alternatively, the oscillator block can be used to route an external square wave to the system clock. External sources can provide a very precise clock source. The oscillator is capable of being configured for low power mode or high amplitude mode as selected by HGO.
- **Internal reference generator** — The internal reference generator consists of two controlled clock sources. One is designed to be approximately 8 MHz and can be selected as a local clock for the background debug controller. The other internal reference clock source is typically 243 kHz and can be trimmed for finer accuracy via software when a precise timed event is input to the MCU. This provides a highly reliable, low-cost clock source.
- **Frequency-locked loop** — A frequency-locked loop (FLL) stage takes either the internal or external clock source and multiplies it to a higher frequency. Status bits provide information when the circuit has achieved lock and when it falls out of lock. Additionally, this block can monitor the external reference clock and signals whether the clock is valid or not.
- **Clock select block** — The clock select block provides several switch options for connecting different clock sources to the system clock tree. ICGDCLK is the multiplied clock frequency out of the FLL, ICGERCLK is the reference clock frequency from the crystal or external clock source, and FFE (fixed frequency enable) is a control signal used to control the system fixed frequency clock (XCLK). ICGLCLK is the clock source for the background debug controller (BDC).

8.1.1 Features

The module is intended to be very user friendly with many of the features occurring automatically without user intervention. To quickly configure the module, go to Section 8.5, “Initialization/Application Information” and pick an example that best suits the application needs.

Features of the ICG and clock distribution system:

- Several options for the primary clock source allow a wide range of cost, frequency, and precision choices:
 - 32 kHz–100 kHz crystal or resonator
 - 1 MHz–16 MHz crystal or resonator
 - External clock
 - Internal reference generator
- Defaults to self-locked mode to minimize startup delays
- Frequency-locked loop (FLL) generates 8 MHz to 40 MHz (for bus rates up to 20 MHz)
 - Uses external or internal clock as reference frequency
- Automatic lockout of non-running clock sources
- Reset or interrupt on loss of clock or loss of FLL lock

8.3.2 ICG Control Register 2 (ICGC2)

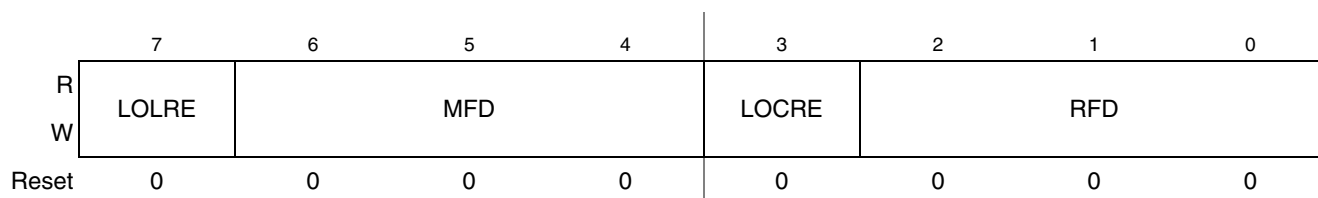


Figure 8-7. ICG Control Register 2 (ICGC2)

Table 8-2. ICGC2 Register Field Descriptions

Field	Description
7 LOLRE	<p>Loss of Lock Reset Enable — The LOLRE bit determines what type of request is made by the ICG following a loss of lock indication. The LOLRE bit only has an effect when LOLS is set.</p> <p>0 Generate an interrupt request on loss of lock. 1 Generate a reset request on loss of lock.</p>
6:4 MFD	<p>Multiplication Factor — The MFD bits control the programmable multiplication factor in the FLL loop. The value specified by the MFD bits establishes the multiplication factor (N) applied to the reference frequency. Writes to the MFD bits will not take effect if a previous write is not complete. Select a low enough value for N such that $f_{ICGDCLK}$ does not exceed its maximum specified value.</p> <p>000 Multiplication factor = 4 001 Multiplication factor = 6 010 Multiplication factor = 8 011 Multiplication factor = 10 100 Multiplication factor = 12 101 Multiplication factor = 14 110 Multiplication factor = 16 111 Multiplication factor = 18</p>
3 LOCRE	<p>Loss of Clock Reset Enable — The LOCRE bit determines how the system manages a loss of clock condition.</p> <p>0 Generate an interrupt request on loss of clock. 1 Generate a reset request on loss of clock.</p>
2:0 RFD	<p>Reduced Frequency Divider — The RFD bits control the value of the divider following the clock select circuitry. The value specified by the RFD bits establishes the division factor (R) applied to the selected output clock source. Writes to the RFD bits will not take effect if a previous write is not complete.</p> <p>000 Division factor = 1 001 Division factor = 2 010 Division factor = 4 011 Division factor = 8 100 Division factor = 16 101 Division factor = 32 110 Division factor = 64 111 Division factor = 128</p>

9.4.2 KBI Pin Enable Register (KBIPE)

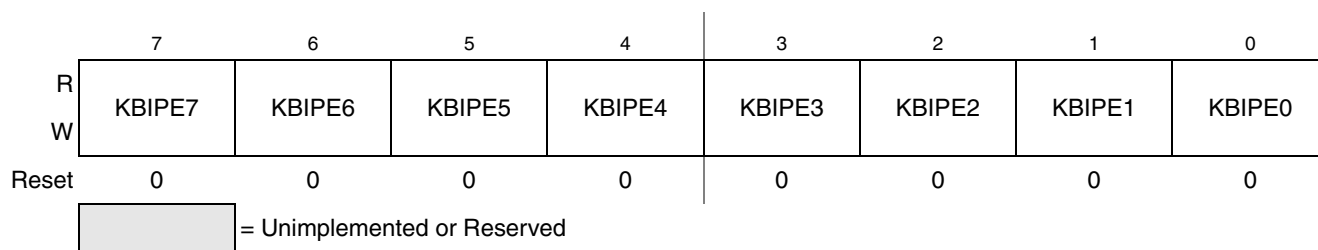


Figure 9-4. KBI Pin Enable Register (KBIPE)

Table 9-2. KBIPE Register Field Descriptions

Field	Description
7:0 KBIPE[7:0]	Keyboard Pin Enable for KBI Port Bits — Each of these read/write bits selects whether the associated KBI port pin is enabled as a keyboard interrupt input or functions as a general-purpose I/O pin. 0 Bit n of KBI port is a general-purpose I/O pin not associated with the KBI 1 Bit n of KBI port enabled as a keyboard interrupt input

9.5 Functional Description

9.5.1 Pin Enables

The KBIPE_n control bits in the KBIPE register allow a user to enable (KBIPE_n = 1) any combination of KBI-related port pins to be connected to the KBI module. Pins corresponding to 0s in KBIPE are general-purpose I/O pins that are not associated with the KBI module.

9.5.2 Edge and Level Sensitivity

Synchronous logic is used to detect edges. Prior to detecting an edge, enabled keyboard inputs in a KBI module must be at the deasserted logic level.

A falling edge is detected when an enabled keyboard input signal is seen as a logic 1 (the deasserted level) during one bus cycle and then a logic 0 (the asserted level) during the next cycle.

A rising edge is detected when the input signal is seen as a logic 0 during one bus cycle and then a logic 1 during the next cycle.

The KBIMOD control bit can be set to reconfigure the detection logic so that it detects edges and levels. In KBIMOD = 1 mode, the KBF status flag becomes set when an edge is detected (when one or more enabled pins change from the deasserted to the asserted level while all other enabled pins remain at their deasserted levels), but the flag is continuously set (and cannot be cleared) as long as any enabled keyboard input pin remains at the asserted level. When the MCU enters stop mode, the synchronous edge-detection logic is bypassed (because clocks are stopped). In stop mode, KBI inputs act as asynchronous level-sensitive inputs so they can wake the MCU from stop mode.

Table 11-4. SCIx2 Field Descriptions (continued)

Field	Description
2 RE	Receiver Enable — When the SCI receiver is off, the RxD pin reverts to being a general-purpose port I/O pin. If LOOPS = 1 the RxD pin reverts to being a general-purpose I/O pin even if RE = 1. 0 Receiver off. 1 Receiver on.
1 RWU	Receiver Wakeup Control — This bit can be written to 1 to place the SCI receiver in a standby state where it waits for automatic hardware detection of a selected wakeup condition. The wakeup condition is either an idle line between messages (WAKE = 0, idle-line wakeup), or a logic 1 in the most significant data bit in a character (WAKE = 1, address-mark wakeup). Application software sets RWU and (normally) a selected hardware condition automatically clears RWU. Refer to Section 11.3.3.2, “Receiver Wakeup Operation” for more details. 0 Normal SCI receiver operation. 1 SCI receiver in standby waiting for wakeup condition.
0 SBK	Send Break — Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 or 11 (13 or 14 if BRK13 = 1) bit times of logic 0 are queued as long as SBK = 1. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. Refer to Section 11.3.2.1, “Send Break and Queued Idle” for more details. 0 Normal transmitter operation. 1 Queue break character(s) to be sent.

11.2.4 SCI Status Register 1 (SCIxS1)

This register has eight read-only status flags. Writes have no effect. Special software sequences (which do not involve writing to this register) are used to clear these status flags.

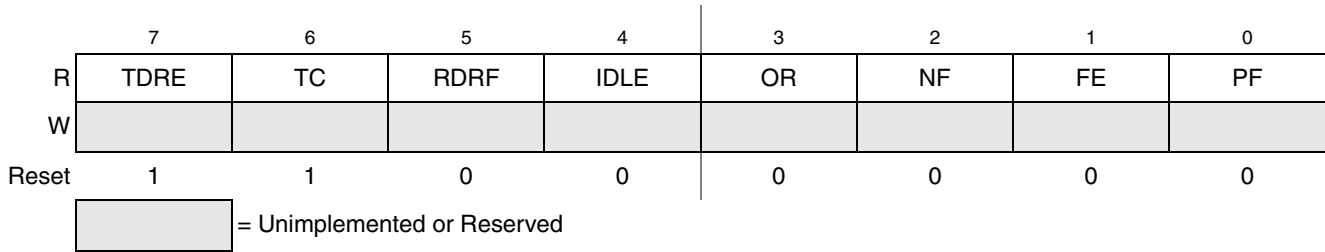


Figure 11-8. SCI Status Register 1 (SCIxS1)

Table 12-5. SPI Baud Rate Prescaler Divisor

SPPR2:SPPR1:SPPR0	Prescaler Divisor
0:0:0	1
0:0:1	2
0:1:0	3
0:1:1	4
1:0:0	5
1:0:1	6
1:1:0	7
1:1:1	8

Table 12-6. SPI Baud Rate Divisor

SPR2:SPR1:SPR0	Rate Divisor
0:0:0	2
0:0:1	4
0:1:0	8
0:1:1	16
1:0:0	32
1:0:1	64
1:1:0	128
1:1:1	256

12.4.4 SPI Status Register (SPI1S)

This register has three read-only status bits. Bits 6, 3, 2, 1, and 0 are not implemented and always read 0. Writes have no meaning or effect.

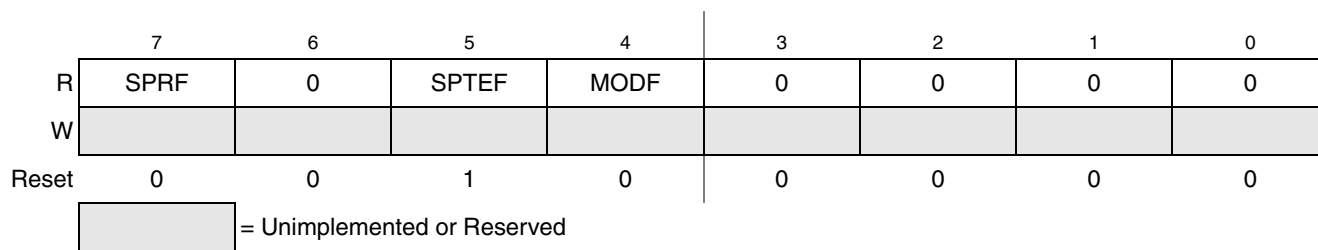


Figure 12-8. SPI Status Register (SPI1S)

13.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such a case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

13.4.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it. If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

13.4.2 10-bit Address

For 10-bit addressing, 0x11110 is used for the first 5 bits of the first address byte. Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing.

13.4.2.1 Master-Transmitter Addresses a Slave-Receiver

The transfer direction is not changed (see Table 13-9). When a 10-bit address follows a start condition, each slave compares the first seven bits of the first byte of the slave address (11110XX) with its own address and tests whether the eighth bit (R/\overline{W} direction bit) is 0. More than one device can find a match and generate an acknowledge (A1). Then, each slave that finds a match compares the eight bits of the second byte of the slave address with its own address. Only one slave finds a match and generates an acknowledge (A2). The matching slave remains addressed by the master until it receives a stop condition (P) or a repeated start condition (Sr) followed by a different slave address.

S	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 0	A1	Slave Address 2nd byte AD[8:1]	A2	Data	A	...	Data	A/A	P
---	--	----------	----	-----------------------------------	----	------	---	-----	------	-----	---

Table 13-9. Master-Transmitter Addresses Slave-Receiver with a 10-bit Address

After the master-transmitter has sent the first byte of the 10-bit address, the slave-receiver sees an IIC interrupt. Software must ensure the contents of IICD are ignored and not treated as valid data for this interrupt.

13.4.2.2 Master-Receiver Addresses a Slave-Transmitter

The transfer direction is changed after the second R/\overline{W} bit (see Table 13-10). Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a slave-receiver. After the repeated start condition (Sr), a matching slave remembers that it was addressed before. This slave then checks whether the first seven bits of the first byte of the slave address following Sr are the same as they were after the start condition (S) and tests whether the eighth (R/\overline{W}) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a stop condition (P) or a repeated start condition (Sr) followed by a different slave address.

Table 14-1. ADC Channel Assignment (continued)

ADCH	Channel	Input	Pin Control	ADCH	Channel	Input	Pin Control
01111	AD15	V _{REFL}	N/A	11111	module disabled	None	N/A

NOTE

Selecting the internal bandgap channel requires BGBE = 1 in SPMSC1 see Section 5.9.8, “System Power Management Status and Control 1 Register (SPMSC1).” For value of bandgap voltage reference see Section A.6, “DC Characteristics.”

14.2.1 Alternate Clock

The ADC module is capable of performing conversions using the MCU bus clock, the bus clock divided by two, the local asynchronous clock (ADACK) within the module, or the alternate clock, ALTCLK. The alternate clock for the MC9S08AC16 Series MCU devices is the external reference clock (ICGERCLK) from the internal clock generator (ICG) module.

Because ICGERCLK is active only while an external clock source is enabled, the ICG must be configured for either FBE or FEE mode (CLKS1 = 1). ICGERCLK must run at a frequency such that the ADC conversion clock (ADCK) runs at a frequency within its specified range (f_{ADCK}) after being divided down from the ALTCLK input as determined by the ADIV bits. For example, if the ADIV bits are set up to divide by four, then the minimum frequency for ALTCLK (ICGERCLK) is four times the minimum value for f_{ADCK} and the maximum frequency is four times the maximum value for f_{ADCK} . Because of the minimum frequency requirement, when an oscillator circuit is used it must be configured for high range operation (RANGE = 1).

ALTCLK is active while the MCU is in wait mode provided the conditions described above are met. This allows ALTCLK to be used as the conversion clock source for the ADC while the MCU is in wait mode.

ALTCLK cannot be used as the ADC conversion clock source while the MCU is in stop3.

14.2.2 Hardware Trigger

The ADC hardware trigger, ADHWT, is output from the real time interrupt (RTI) counter. The RTI counter can be clocked by either ICGERCLK or a nominal 1 kHz clock source within the RTI block. The 1-kHz clock source can be used with the MCU in run, wait, or stop3. With the ICG configured for either FBE or FEE mode, ICGERCLK can be used with the MCU in run or wait.

The period of the RTI is determined by the input clock frequency and the RTIS bits. When the ADC hardware trigger is enabled, a conversion is initiated upon an RTI counter overflow. The RTI counter is a free running counter that generates an overflow at the RTI rate determined by the RTIS bits.

14.2.2.1 Analog Pin Enables

The ADC on MC9S08AC16 Series contains only two analog pin enable registers, APCTL1 and APCTL2.

14.7.2 Sources of Error

Several sources of error exist for A/D conversions. These are discussed in the following sections.

14.7.2.1 Sampling Error

For proper conversions, the input must be sampled long enough to achieve the proper accuracy. Given the maximum input resistance of approximately $7\text{k}\Omega$ and input capacitance of approximately 5.5 pF , sampling to within $1/4\text{LSB}$ (at 10-bit resolution) can be achieved within the minimum sample window (3.5 cycles @ 8 MHz maximum ADCK frequency) provided the resistance of the external analog source (R_{AS}) is kept below $5\text{ k}\Omega$.

Higher source resistances or higher-accuracy sampling is possible by setting ADLSMP (to increase the sample window to 23.5 cycles) or decreasing ADCK frequency to increase sample time.

14.7.2.2 Pin Leakage Error

Leakage on the I/O pins can cause conversion error if the external analog source resistance (R_{AS}) is high. If this error cannot be tolerated by the application, keep R_{AS} lower than $V_{DDAD} / (2^N \cdot I_{LEAK})$ for less than $1/4\text{LSB}$ leakage error ($N = 8$ in 8-bit mode or 10 in 10-bit mode).

14.7.2.3 Noise-Induced Errors

System noise which occurs during the sample or conversion process can affect the accuracy of the conversion. The ADC accuracy numbers are guaranteed as specified only if the following conditions are met:

- There is a $0.1\text{ }\mu\text{F}$ low-ESR capacitor from V_{REFH} to V_{REFL} .
- There is a $0.1\text{ }\mu\text{F}$ low-ESR capacitor from V_{DDAD} to V_{SSAD} .
- If inductive isolation is used from the primary supply, an additional $1\text{ }\mu\text{F}$ capacitor is placed from V_{DDAD} to V_{SSAD} .
- V_{SSAD} (and V_{REFL} , if connected) is connected to V_{SS} at a quiet point in the ground plane.
- Operate the MCU in wait or stop3 mode before initiating (hardware triggered conversions) or immediately after initiating (hardware or software triggered conversions) the ADC conversion.
 - For software triggered conversions, immediately follow the write to the ADC1SC1 with a WAIT instruction or STOP instruction.
 - For stop3 mode operation, select ADACK as the clock source. Operation in stop3 reduces V_{DD} noise but increases effective conversion time due to stop recovery.
- There is no I/O switching, input or output, on the MCU during the conversion.

There are some situations where external system activity causes radiated or conducted noise emissions or excessive V_{DD} noise is coupled into the ADC. In these situations, or when the MCU cannot be placed in wait or stop3 or I/O activity cannot be halted, these recommended actions may reduce the effect of noise on the accuracy:

- Place a $0.01\text{ }\mu\text{F}$ capacitor (C_{AS}) on the selected input channel to V_{REFL} or V_{SSAD} (this will improve noise issues but will affect sample rate based on the external analog source resistance).

converter yields the lower code (and vice-versa). However, even very small amounts of system noise can cause the converter to be indeterminate (between two codes) for a range of input voltages around the transition voltage. This range is normally around $\pm 1/2$ LSB and will increase with noise. This error may be reduced by repeatedly sampling the input and averaging the result. Additionally the techniques discussed in Section 14.7.2.3 will reduce this error.

Non-monotonicity is defined as when, except for code jitter, the converter converts to a lower code for a higher input voltage. Missing codes are those values which are never converted for any input value.

In 8-bit or 10-bit mode, the ADC is guaranteed to be monotonic and to have no missing codes.

Chapter 15

Development Support

15.1 Introduction

Development support systems in the HCS08 include the background debug controller (BDC) and the on-chip debug module (DBG). The BDC provides a single-wire debug interface to the target MCU that provides a convenient interface for programming the on-chip FLASH and other nonvolatile memories. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

In the HCS08 Family, address and data bus signals are not available on external pins (not even in test modes). Debug is done through commands fed into the target MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals.

The alternate BDC clock source for MC9S08AC16 Series is the ICGCLK. See Chapter 8, “Internal Clock Generator (S08ICGV4)” for more information about ICGCLK and how to select clock sources.

A.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

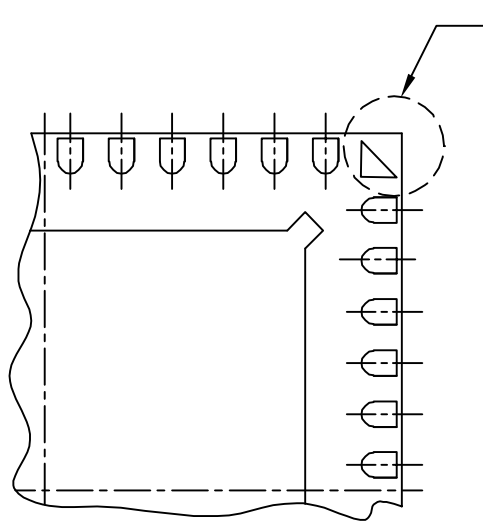
A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-4. ESD and Latch-up Test Conditions

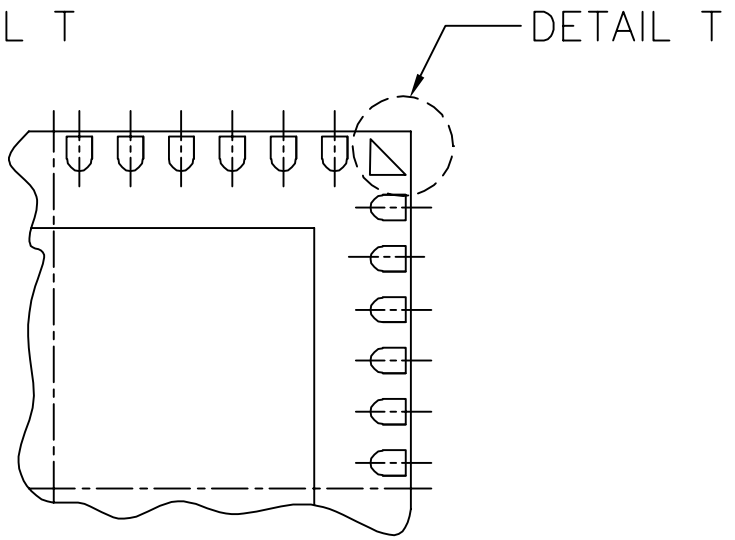
Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		– 2.5	V
	Maximum input voltage limit		7.5	V

Table A-5. ESD and Latch-Up Protection Characteristics

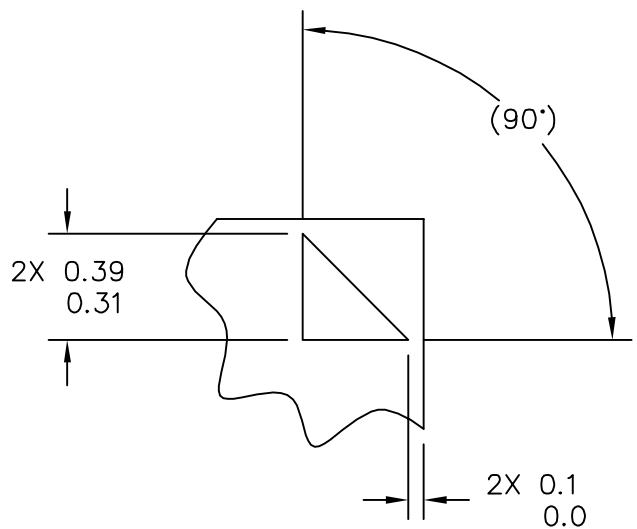
Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	± 2000	–	V
2	C	Machine Model (MM)	V_{MM}	± 200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	± 500	–	V
4	C	Latch-up Current at $T_A = 125^\circ\text{C}$	I_{LAT}	± 100	–	mA



DETAIL M
PIN 1 BACKSIDE IDENTIFIER OPTION

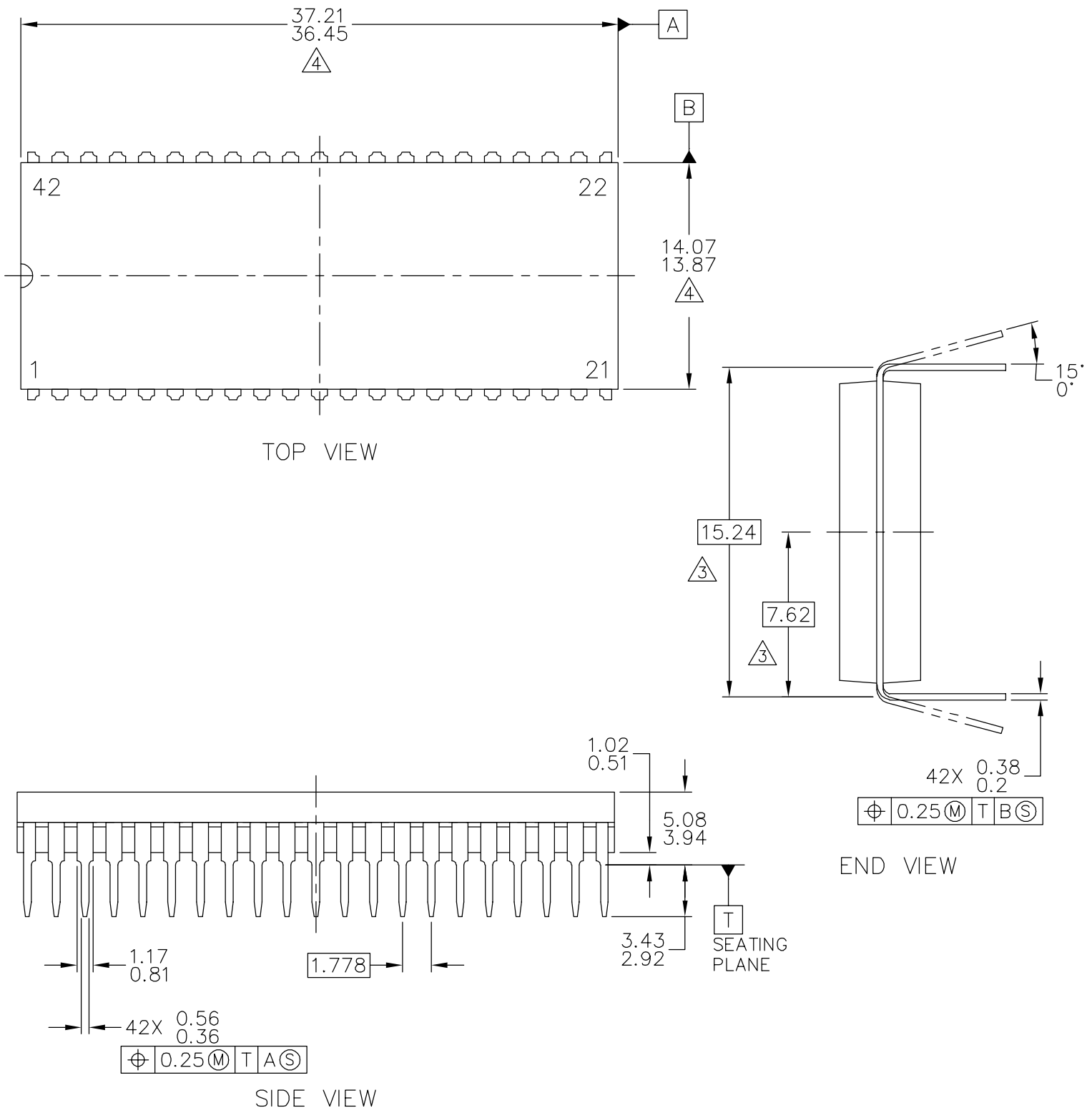


DETAIL M
PIN 1 BACKSIDE IDENTIFIER OPTION

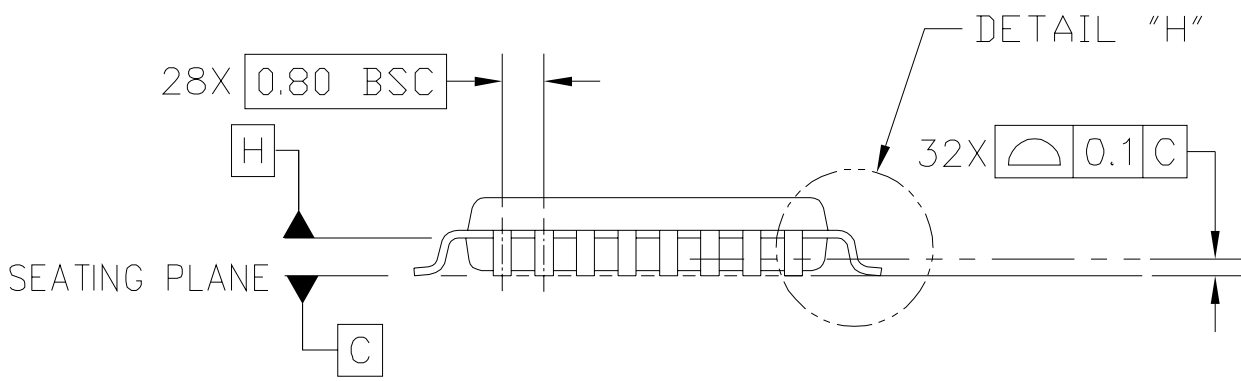
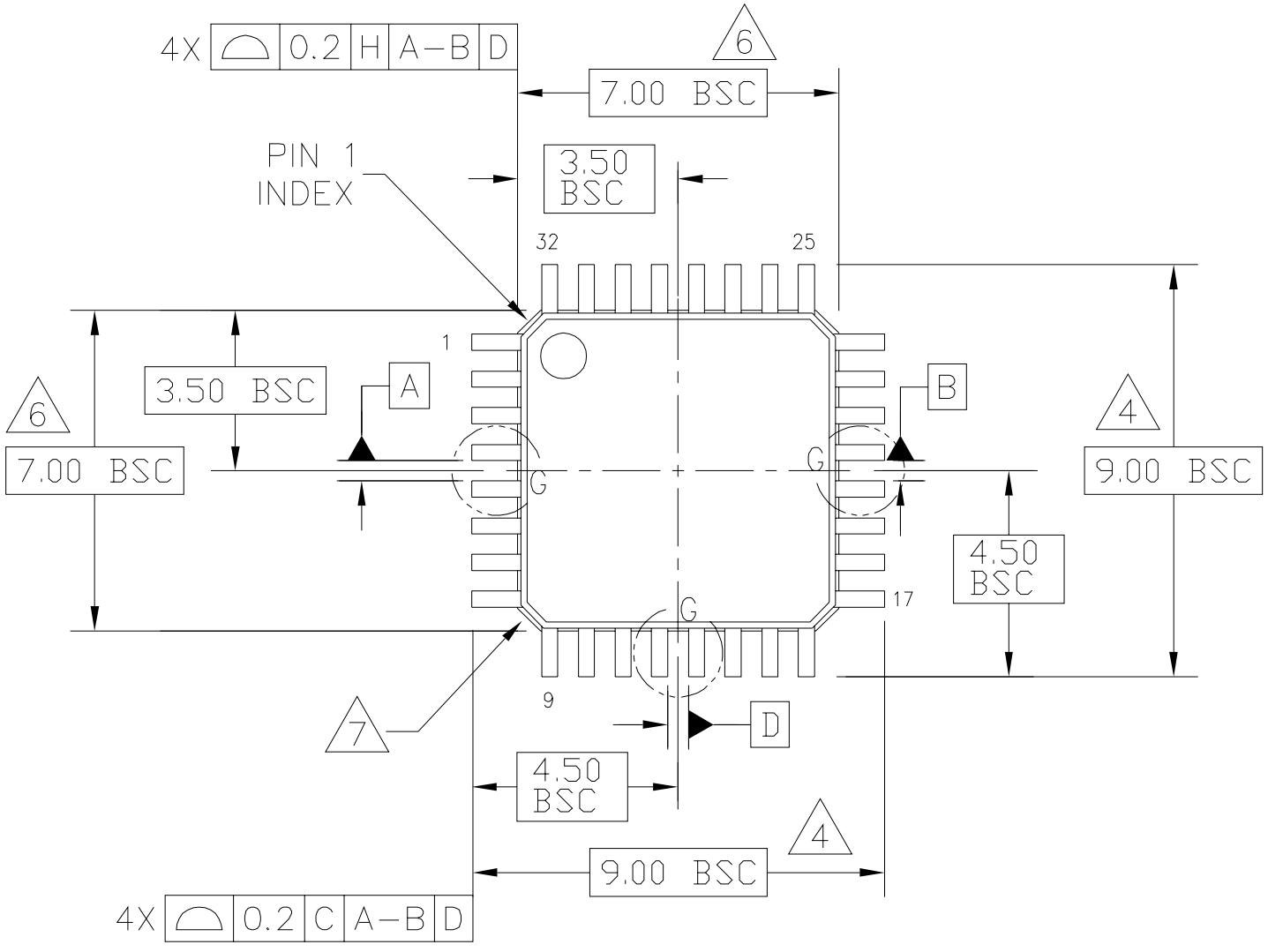


DETAIL T

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	CASE NUMBER: 1314-05	05 DEC 2005	
	STANDARD: JEDEC-MO-220 VKKD-2		



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	CASE NUMBER: 873A-03	19 MAY 2005	
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