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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

|                                 |   |
|---------------------------------|---|
| Product Status                  | Obsolete  |
| Programmable Type               | In System Programmable  |
| Delay Time tpd(1) Max           | 15 ns   |
| Voltage Supply - Internal       | 4.75V ~ 5.25V   |
| Number of Logic Elements/Blocks | 16  |
| Number of Macrocells            | 64  |
| Number of Gates                 | 2000  |
| Number of I/O                   | 64  |
| Operating Temperature           | 0°C ~ 70°C (TA)   |
| Mounting Type                   | Surface Mount   |
| Package / Case                  | 100-LQFP  |
| Supplier Device Package         | 100-TQFP (14x14)  |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-2064a-80ltn100">https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-2064a-80ltn100</a> |

## Features

### • ENHANCEMENTS

- ispLSI 2064A is Fully Form and Function Compatible to the ispLSI 2064, with Identical Timing Specifications and Packaging
- ispLSI 2064A is Built on an Advanced 0.35 Micron E<sup>2</sup>CMOS<sup>®</sup> Technology

### • HIGH DENSITY PROGRAMMABLE LOGIC

- 2000 PLD Gates
- 64 I/O Pins, Four Dedicated Inputs
- 64 Registers
- High Speed Global Interconnect
- Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
- Small Logic Block Size for Random Logic

### • HIGH PERFORMANCE E<sup>2</sup>CMOS<sup>®</sup> TECHNOLOGY

- $f_{max} = 125$  MHz Maximum Operating Frequency
- $t_{pd} = 7.5$  ns Propagation Delay
- TTL Compatible Inputs and Outputs
- Electrically Erasable and Reprogrammable
- Non-Volatile
- 100% Tested at Time of Manufacture
- Unused Product Term Shutdown Saves Power

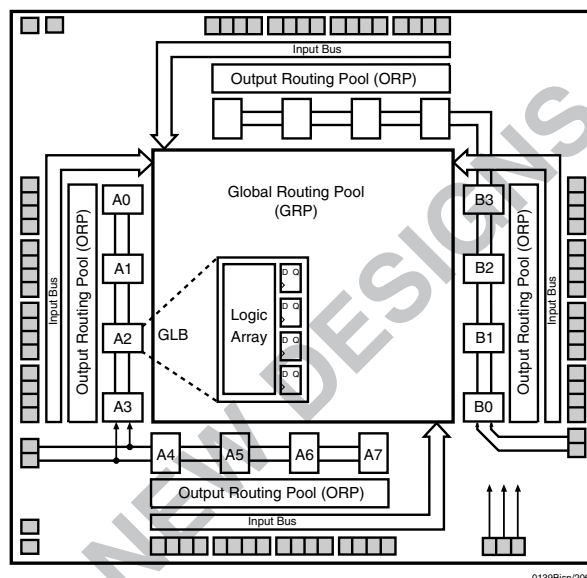
### • IN-SYSTEM PROGRAMMABLE

- In-System Programmable (ISP<sup>™</sup>) 5V Only
- Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
- Reprogram Soldered Devices for Faster Prototyping

### • OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS

- Complete Programmable Device Can Combine Glue Logic and Structured Designs
- Enhanced Pin Locking Capability
- Three Dedicated Clock Input Pins
- Synchronous and Asynchronous Clocks
- Programmable Output Slew Rate Control to Minimize Switching Noise
- Flexible Pin Placement
- Optimized Global Routing Pool Provides Global Interconnectivity
- Lead-Free Package Options

## Functional Block Diagram



## Description

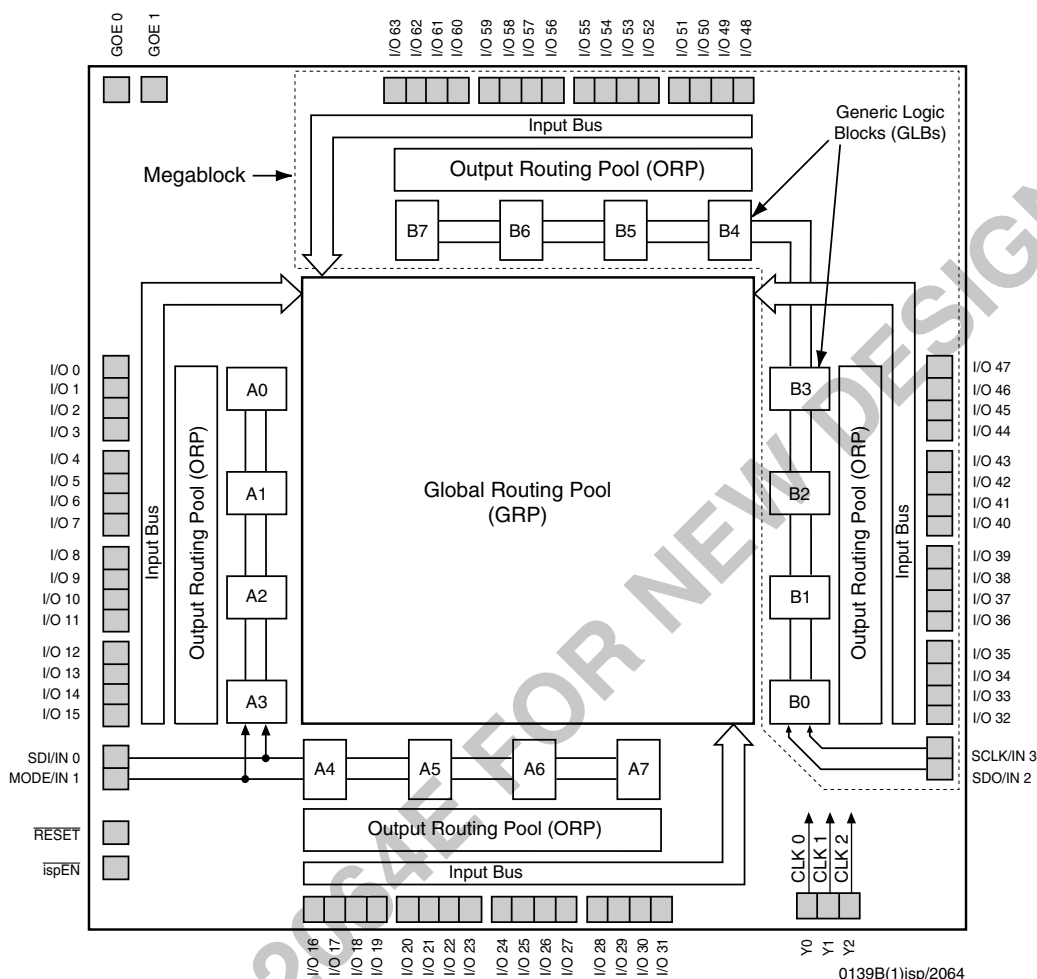
The ispLSI 2064 and 2064A are High Density Programmable Logic Devices. The devices contain 64 Registers, 64 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The 2064 and 2064A feature 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2064 and 2064A offer non-volatile reprogrammability of the logic, as well as the interconnect, to provide truly reconfigurable systems.

The basic unit of logic on these devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1...B7 (Figure 1). There are a total of 16 GLBs in the ispLSI 2064 and 2064A devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

**Select devices have been discontinued.  
See Ordering Information section for product status.**

## Functional Block Diagram

Figure 1. ispLSI 2064/A Functional Block Diagram



The devices also have 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by two ORPs. Each ispLSI 2064 and 2064A device contains two Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2064 and 2064A devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Select devices have been discontinued.  
See Ordering Information section for product status.

## Absolute Maximum Ratings <sup>1</sup>

Supply Voltage  $V_{CC}$  ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to  $V_{CC} + 1.0V$

Off-State Output Voltage Applied ..... -2.5 to  $V_{CC} + 1.0V$

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. ( $T_J$ ) with Power Applied ..... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## DC Recommended Operating Condition

| SYMBOL   | PARAMETER          |  | MIN. | MAX.       | UNITS |
|----------|--------------------|--|------|------------|-------|
| $V_{CC}$ | Supply Voltage     | Commercial $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   | 4.75 | 5.25       | V     |
|          |                    | Industrial $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | 4.5  | 5.5        | V     |
| $V_{IL}$ | Input Low Voltage  |  | 0    | 0.8        | V     |
| $V_{IH}$ | Input High Voltage |  | 2.0  | $V_{CC}+1$ | V     |

Table 2 - 0005/2064

## Capacitance ( $T_A=25^\circ\text{C}$ , $f=1.0\text{ MHz}$ )

| SYMBOL | PARAMETER                   | TYPICAL | UNITS | TEST CONDITIONS                    |
|--------|-----------------------------|---------|-------|------------------------------------|
| $C_1$  | Dedicated Input Capacitance | 8       | pf    | $V_{CC} = 5.0V$ , $V_{IN} = 2.0V$  |
| $C_2$  | I/O Capacitance             | 9       | pf    | $V_{CC} = 5.0V$ , $V_{I/O} = 2.0V$ |
| $C_3$  | Clock Capacitance           | 15      | pf    | $V_{CC} = 5.0V$ , $V_Y = 2.0V$     |

Table 2-0006/2064

## Data Retention Specifications

| PARAMETER              | MINIMUM | MAXIMUM | UNITS  |
|------------------------|---------|---------|--------|
| Data Retention         | 20      | —       | Years  |
| Erase/Reprogram Cycles | 10000   | —       | Cycles |

Table 2-0008/2064

Select devices have been discontinued.  
See Ordering Information section for product status.

## Switching Test Conditions

|  |              |             |
|--|--------------|-------------|
| Input Pulse Levels                     | GND to 3.0V  |             |
| Input Rise and Fall Time<br>10% to 90% | -125         | $\leq 2$ ns |
|  | Others       | $\leq 3$ ns |
| Input Timing Reference Levels          | 1.5V         |             |
| Output Timing Reference Levels         | 1.5V         |             |
| Output Load                            | See Figure 2 |             |

3-state levels are measured 0.5V from steady-state active level.

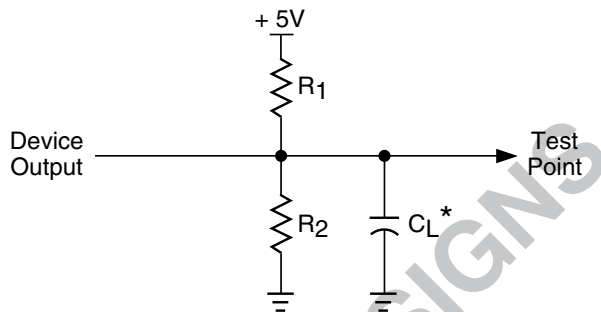
Table 2-0003/2064

### Output Load Conditions (see Figure 2)

| TEST CONDITION |                                      | R1           | R2           | CL   |
|----------------|--------------------------------------|--------------|--------------|------|
| A              |                                      | 470 $\Omega$ | 390 $\Omega$ | 35pF |
| B              | Active High                          | $\infty$     | 390 $\Omega$ | 35pF |
|                | Active Low                           | 470 $\Omega$ | 390 $\Omega$ | 35pF |
| C              | Active High to Z<br>at $V_{OH}-0.5V$ | $\infty$     | 390 $\Omega$ | 5pF  |
|                | Active Low to Z<br>at $V_{OL}+0.5V$  | 470 $\Omega$ | 390 $\Omega$ | 5pF  |

Table 2-0004/2064

Figure 2. Test Load



\*CL includes Test Fixture and Probe Capacitance.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

| SYMBOL         | PARAMETER                               | CONDITION   | MIN.       | TYP. <sup>3</sup> | MAX. | UNITS   |
|----------------|---|---|------------|-------------------|------|---------|
| $V_{OL}$       | Output Low Voltage                      | $I_{OL} = 8$ mA                                       | —          | —                 | 0.4  | V       |
| $V_{OH}$       | Output High Voltage                     | $I_{OH} = -4$ mA                                      | 2.4        | —                 | —    | V       |
| $I_{IL}$       | Input or I/O Low Leakage Current        | $0V \leq V_{IN} \leq V_{IL} (Max.)$                   | —          | —                 | -10  | $\mu A$ |
| $I_{IH}$       | Input or I/O High Leakage Current       | $3.5V \leq V_{IN} \leq V_{CC}$                        | —          | —                 | 10   | $\mu A$ |
| $I_{IL-isp}$   | $\bar{isp}EN$ Input Low Leakage Current | $0V \leq V_{IN} \leq V_{IL}$                          | —          | —                 | -150 | $\mu A$ |
| $I_{IL-PU}$    | I/O Active Pull-Up Current              | $0V \leq V_{IN} \leq V_{IL}$                          | —          | —                 | -150 | $\mu A$ |
| $I_{OS}^1$     | Output Short Circuit Current            | $V_{CC} = 5V, V_{OUT} = 0.5V$                         | —          | —                 | -200 | mA      |
| $I_{CC}^{2,4}$ | Operating Power Supply Current          | $V_{IL} = 0.0V, V_{IH} = 3.0V$<br>$f_{CLOCK} = 1$ MHz | Commercial | —                 | 95   | 175 mA  |
|                |   |   | Industrial | —                 | 95   | — mA    |

Table 2-0007/2064

- One output at a time for a maximum duration of one second.  $V_{OUT} = 0.5V$  was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
- Measured using four 16-bit counters.
- Typical values are at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .
- Maximum  $I_{CC}$  varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum  $I_{CC}$ .

Select devices have been discontinued.  
See Ordering Information section for product status.

## External Timing Parameters

Over Recommended Operating Conditions

| PARAMETER                     | TEST COND. <sup>4</sup> | # <sup>2</sup> | DESCRIPTION <sup>1</sup>   | -125 |      | -100 |      | -80  |      | UNITS |
|-------------------------------|-------------------------|----------------|--|------|------|------|------|------|------|-------|
|                               |                         |                |  | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |       |
| <b>t<sub>pd1</sub></b>        | A                       | 1              | Data Propagation Delay, 4PT Bypass, ORP Bypass                           | –    | 7.5  | –    | 10.0 | –    | 15.0 | ns    |
| <b>t<sub>pd2</sub></b>        | A                       | 2              | Data Propagation Delay   | –    | 10.0 | –    | 13.0 | –    | 18.5 | ns    |
| <b>f<sub>max</sub></b>        | A                       | 3              | Clock Frequency with Internal Feedback <sup>3</sup>                      | 125  | –    | 100  | –    | 81.0 | –    | MHz   |
| <b>f<sub>max</sub> (Ext.)</b> | –                       | 4              | Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ ) | 100  | –    | 77.0 | –    | 57.0 | –    | MHz   |
| <b>f<sub>max</sub> (Tog.)</b> | –                       | 5              | Clock Frequency, Max. Toggle   | 125  | –    | 111  | –    | 100  | –    | MHz   |
| <b>t<sub>su1</sub></b>        | –                       | 6              | GLB Reg. Setup Time before Clock, 4 PT Bypass                            | 5.0  | –    | 6.5  | –    | 9.0  | –    | ns    |
| <b>t<sub>co1</sub></b>        | A                       | 7              | GLB Reg. Clock to Output Delay, ORP Bypass                               | –    | 4.0  | –    | 5.0  | –    | 6.5  | ns    |
| <b>t<sub>h1</sub></b>         | –                       | 8              | GLB Reg. Hold Time after Clock, 4 PT Bypass                              | 0.0  | –    | 0.0  | –    | 0.0  | –    | ns    |
| <b>t<sub>su2</sub></b>        | –                       | 9              | GLB Reg. Setup Time before Clock   | 6.0  | –    | 8.0  | –    | 11.0 | –    | ns    |
| <b>t<sub>co2</sub></b>        | –                       | 10             | GLB Reg. Clock to Output Delay   | –    | 4.5  | –    | 6.0  | –    | 8.0  | ns    |
| <b>t<sub>h2</sub></b>         | –                       | 11             | GLB Reg. Hold Time after Clock   | 0.0  | –    | 0.0  | –    | 0.0  | –    | ns    |
| <b>t<sub>r1</sub></b>         | A                       | 12             | Ext. Reset Pin to Output Delay   | –    | 10.0 | –    | 13.5 | –    | 17.0 | ns    |
| <b>t<sub>rw1</sub></b>        | –                       | 13             | Ext. Reset Pulse Duration  | 5.0  | –    | 6.5  | –    | 10.0 | –    | ns    |
| <b>t<sub>ptoen</sub></b>      | B                       | 14             | Product Term OE, Enable  | –    | 12.0 | –    | 15.0 | –    | 18.0 | ns    |
| <b>t<sub>ptodis</sub></b>     | C                       | 15             | Product Term OE, Disable   | –    | 12.0 | –    | 15.0 | –    | 18.0 | ns    |
| <b>t<sub>goen</sub></b>       | B                       | 16             | Global OE, Enable  | –    | 7.0  | –    | 9.0  | –    | 12.0 | ns    |
| <b>t<sub>goedis</sub></b>     | C                       | 17             | Global OE, Disable   | –    | 7.0  | –    | 9.0  | –    | 12.0 | ns    |
| <b>t<sub>wh</sub></b>         | –                       | 18             | External Synchronous Clock Pulse Duration, High                          | 4.0  | –    | 4.5  | –    | 5.0  | –    | ns    |
| <b>t<sub>wl</sub></b>         | –                       | 19             | External Synchronous Clock Pulse Duration, Low                           | 4.0  | –    | 4.5  | –    | 5.0  | –    | ns    |

Table 2 - 0030B/2064-130

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.

2. Refer to Timing Model in this data sheet for further details.

3. Standard 16-bit counter using GRP feedback.

4. Reference Switching Test Conditions section.

Select devices have been discontinued.  
See Ordering Information section for product status.

## Internal Timing Parameters<sup>1</sup>

Over Recommended Operating Conditions

| PARAMETER            | # <sup>2</sup> | DESCRIPTION   | -125 |      | -100 |      | -80  |      | UNITS |
|----------------------|----------------|---|------|------|------|------|------|------|-------|
|                      |                |   | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |       |
| Inputs               |                |   |      |      |      |      |      |      |       |
| t <sub>io</sub>      | 20             | Input Buffer Delay                                    | –    | 0.2  | –    | 0.5  | –    | 1.8  | ns    |
| t <sub>din</sub>     | 21             | Dedicated Input Delay                                 | –    | 1.5  | –    | 2.2  | –    | 4.4  | ns    |
| GRP                  |                |   |      |      |      |      |      |      |       |
| t <sub>grp</sub>     | 22             | GRP Delay   | –    | 1.3  | –    | 1.7  | –    | 2.6  | ns    |
| GLB                  |                |   |      |      |      |      |      |      |       |
| t <sub>4ptbp</sub>   | 23             | 4 Product Term Bypass Comb. Path Delay                | –    | 4.5  | –    | 5.8  | –    | 8.1  | ns    |
| t <sub>4ptbp</sub>   | 24             | 4 Product Term Bypass Reg. Path Delay                 | –    | 5.0  | –    | 5.8  | –    | 6.8  | ns    |
| t <sub>1ptxor</sub>  | 25             | 1 Product Term/XOR Path Delay                         | –    | 5.7  | –    | 6.8  | –    | 8.0  | ns    |
| t <sub>20ptxor</sub> | 26             | 20 Product Term/XOR Path Delay                        | –    | 6.0  | –    | 7.3  | –    | 8.8  | ns    |
| t <sub>xoradj</sub>  | 27             | XOR Adjacent Path Delay <sup>3</sup>                  | –    | 6.5  | –    | 8.0  | –    | 9.8  | ns    |
| t <sub>gbp</sub>     | 28             | GLB Register Bypass Delay                             | –    | 0.5  | –    | 0.5  | –    | 1.3  | ns    |
| t <sub>gsu</sub>     | 29             | GLB Register Setup Time before Clock                  | 0.8  | –    | 1.2  | –    | 1.4  | –    | ns    |
| t <sub>gh</sub>      | 30             | GLB Register Hold Time after Clock                    | 3.0  | –    | 4.0  | –    | 6.0  | –    | ns    |
| t <sub>gco</sub>     | 31             | GLB Register Clock to Output Delay                    | –    | 0.2  | –    | 0.3  | –    | 0.4  | ns    |
| t <sub>gro</sub>     | 32             | GLB Register Reset to Output Delay                    | –    | 1.1  | –    | 1.3  | –    | 1.6  | ns    |
| t <sub>ptre</sub>    | 33             | GLB Product Term Reset to Register Delay              | –    | 4.8  | –    | 6.1  | –    | 8.6  | ns    |
| t <sub>ptoe</sub>    | 34             | GLB Product Term Output Enable to I/O Cell Delay      | –    | 7.3  | –    | 8.6  | –    | 9.0  | ns    |
| t <sub>ptck</sub>    | 35             | GLB Product Term Clock Delay                          | 3.3  | 5.6  | 4.1  | 7.1  | 5.6  | 10.2 | ns    |
| ORP                  |                |   |      |      |      |      |      |      |       |
| t <sub>orp</sub>     | 36             | ORP Delay   | –    | 0.8  | –    | 1.4  | –    | 2.0  | ns    |
| t <sub>orpbp</sub>   | 37             | ORP Bypass Delay                                      | –    | 0.3  | –    | 0.4  | –    | 0.5  | ns    |
| Outputs              |                |   |      |      |      |      |      |      |       |
| t <sub>ob</sub>      | 38             | Output Buffer Delay                                   | –    | 1.2  | –    | 1.6  | –    | 2.0  | ns    |
| t <sub>sl</sub>      | 39             | Output Slew Limited Delay Adder                       | –    | 10.0 | –    | 10.0 | –    | 10.0 | ns    |
| t <sub>oen</sub>     | 40             | I/O Cell OE to Output Enabled                         | –    | 3.2  | –    | 4.2  | –    | 4.6  | ns    |
| t <sub>odis</sub>    | 41             | I/O Cell OE to Output Disabled                        | –    | 3.2  | –    | 4.2  | –    | 4.6  | ns    |
| t <sub>goe</sub>     | 42             | Global Output Enable                                  | –    | 3.8  | –    | 4.8  | –    | 7.4  | ns    |
| Clocks               |                |   |      |      |      |      |      |      |       |
| t <sub>gy0</sub>     | 43             | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 2.3  | 2.3  | 2.7  | 2.7  | 3.6  | 3.6  | ns    |
| t <sub>gy1/2</sub>   | 44             | Clock Delay, Y1 or Y2 to Global GLB Clock Line        | 2.3  | 2.3  | 2.7  | 2.7  | 3.6  | 3.6  | ns    |
| Global Reset         |                |   |      |      |      |      |      |      |       |
| t <sub>gr</sub>      | 45             | Global Reset to GLB                                   | –    | 6.9  | –    | 9.2  | –    | 11.4 | ns    |

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

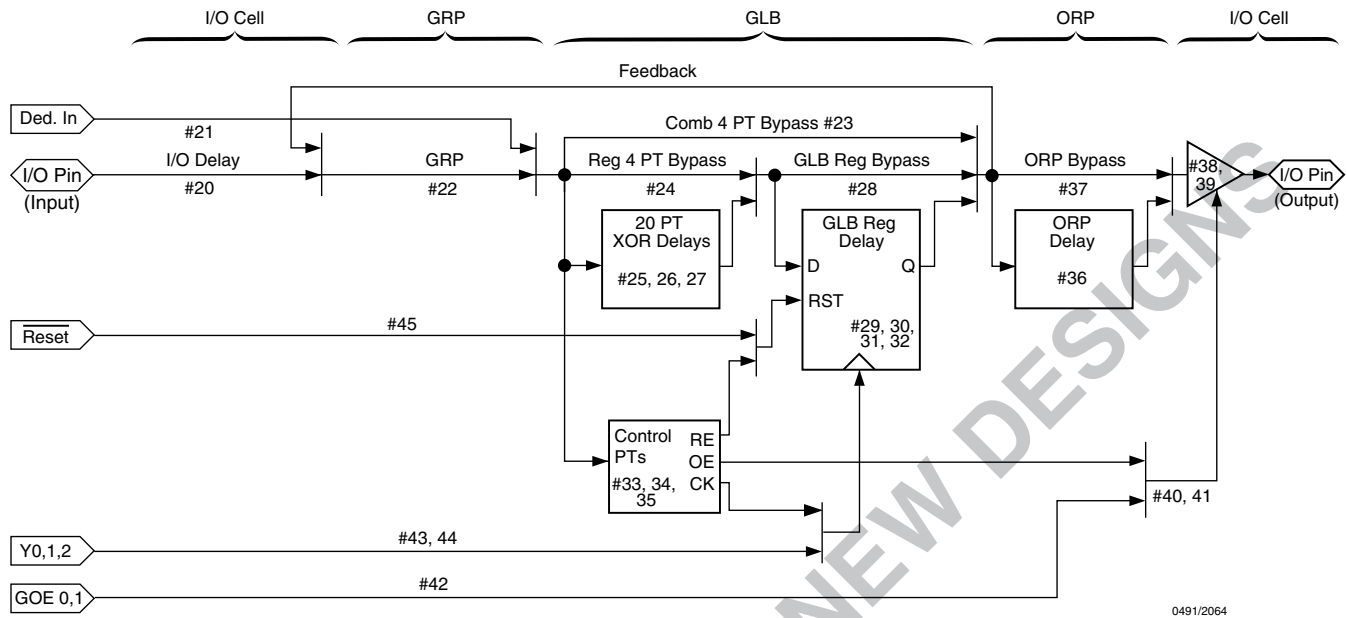
3. The XOR adjacent path can only be used by hard macros.

Table 2- 0036C/2064-130

Select devices have been discontinued.  
See Ordering Information section for product status.



**ispLSI 2064/A Timing Model**



**Derivations of  $t_{su}$ ,  $t_h$  and  $t_{co}$  from the Product Term Clock<sup>1</sup>**

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg su} - \text{Clock (min)} \\
 &= (t_{io} + t_{grp} + t_{20ptxor}) + (t_{gsu}) - (t_{io} + t_{grp} + t_{ptck(min)}) \\
 &= (\#20 + \#22 + \#26) + (\#29) - (\#20 + \#22 + \#35) \\
 3.5 \text{ ns} &= (0.2 + 1.3 + 6.0) + (0.8) - (0.2 + 1.3 + 3.3) \\
 t_h &= \text{Clock (max)} + \text{Reg h} - \text{Logic} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gh}) - (t_{io} + t_{grp} + t_{20ptxor}) \\
 &= (\#20 + \#22 + \#35) + (\#30) - (\#20 + \#22 + \#26) \\
 2.6 \text{ ns} &= (0.2 + 1.3 + 5.6) + (3.0) - (0.2 + 1.3 + 6.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg co} + \text{Output} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#22 + \#35) + (\#31) + (\#36 + \#38) \\
 9.4 \text{ ns} &= (0.2 + 1.3 + 5.6) + (0.2) + (0.8 + 1.2)
 \end{aligned}$$

Table 2- 0042A-2064

Note: Calculations are based upon timing specifications for the ispLSI 2064/A-125L.

Select devices have been discontinued.  
See Ordering Information section for product status.

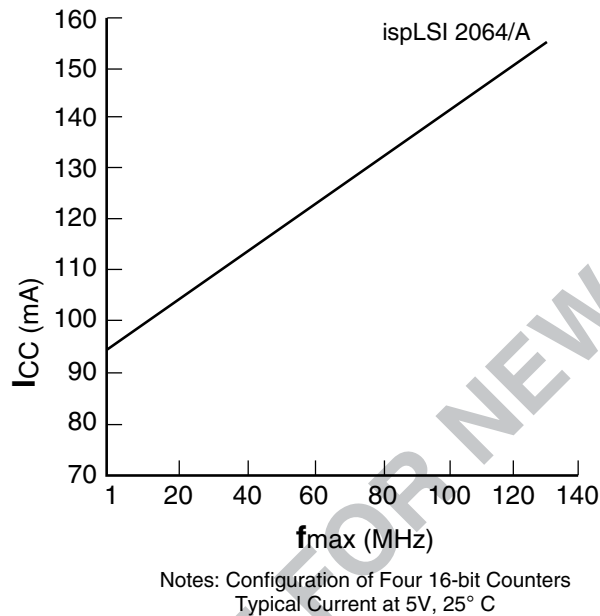


## Power Consumption

Power consumption in the ispLSI 2064 and 2064A devices depends on two primary factors: the speed at which the device is operating and the number of Product Terms

used. Figure 4 shows the relationship between power and operating speed.

**Figure 4. Typical Device Power Consumption vs fmax**



ICC can be estimated for the ispLSI 2064/A using the following equation:

$$I_{CC}(\text{mA}) = 38 + (\# \text{ of PTs} * 0.33) + (\# \text{ of nets} * \text{Max freq} * 0.007)$$

Where:

- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A/2064A

Select devices have been discontinued.  
See Ordering Information section for product status.

## Pin Description

| NAME  | PLCC PIN NUMBERS   | DESCRIPTION   |
|---|--|---|
| I/O 0 - I/O 3<br>I/O 4 - I/O 7<br>I/O 8 - I/O 11<br>I/O 12 - I/O 15<br>I/O 16 - I/O 19<br>I/O 20 - I/O 23<br>I/O 24 - I/O 27<br>I/O 28 - I/O 31<br>I/O 32 - I/O 35<br>I/O 36 - I/O 39<br>I/O 40 - I/O 43<br>I/O 44 - I/O 47<br>I/O 48 - I/O 51<br>I/O 52 - I/O 55<br>I/O 56 - I/O 59<br>I/O 60 - I/O 63 | 26, 27, 28, 29,<br>30, 31, 32, 33,<br>34, 35, 36, 37,<br>38, 39, 40, 41,<br>45, 46, 47, 48,<br>49, 50, 51, 52,<br>53, 54, 55, 56,<br>57, 58, 59, 60,<br>68, 69, 70, 71,<br>72, 73, 74, 75,<br>76, 77, 78, 79,<br>80, 81, 82, 83,<br>3, 4, 5, 6,<br>7, 8, 9, 10,<br>11, 12, 13, 14,<br>15, 16, 17, 18 | Input/Output Pins — These are the general purpose I/O pins used by the logic array.   |
| GOE 0, GOE 1  | 67, 84   | Global Output Enable input pins.  |
| Y0, Y1, Y2<br><br>$\overline{\text{RESET}}$   | 20, 66, 63<br><br>24   | Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs in the device.<br><br>Active Low (0) Reset pin which resets all registers in the device.  |
| $\overline{\text{ispEN}}$<br><br>SDI/ IN 0 <sup>2</sup><br><br>MODE/ IN 1 <sup>2</sup><br><br>SDO/ IN 2 <sup>2</sup><br><br>SCLK/ IN 3 <sup>2</sup>   | 23<br><br>25<br><br>42<br><br>44<br><br>61   | Input — Dedicated in-system programming enable pin. This pin is brought low to enable the programming mode. When low, the MODE, SDI, SDO and SCLK controls become active.<br><br>Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated pin input.<br><br>Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.<br><br>Output/Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.<br><br>Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin. |
| GND<br>VCC<br>NC <sup>1</sup>   | 1, 22, 43, 64<br>21, 65<br>2, 19, 62   | Ground (GND)<br>Vcc<br>No Connect   |

1. NC pins are not to be connected to any active signals, VCC or GND.

Table 2-0002A-08isp/2064

2. Pins have dual function capability.

Select devices have been discontinued.  
See Ordering Information section for product status.

## Pin Description

| NAME  | TQFP PIN NUMBERS   | DESCRIPTION   |
|---|--|---|
| I/O 0 - I/O 3<br>I/O 4 - I/O 7<br>I/O 8 - I/O 11<br>I/O 12 - I/O 15<br>I/O 16 - I/O 19<br>I/O 20 - I/O 23<br>I/O 24 - I/O 27<br>I/O 28 - I/O 31<br>I/O 32 - I/O 35<br>I/O 36 - I/O 39<br>I/O 40 - I/O 43<br>I/O 44 - I/O 47<br>I/O 48 - I/O 51<br>I/O 52 - I/O 55<br>I/O 56 - I/O 59<br>I/O 60 - I/O 63 | 17, 18, 19, 20,<br>21, 22, 23, 28,<br>29, 30, 31, 32,<br>33, 34, 35, 36,<br>40, 41, 42, 43,<br>44, 45, 46, 47,<br>48, 53, 54, 55,<br>56, 57, 58, 59,<br>67, 68, 69, 70,<br>71, 72, 73, 78,<br>79, 80, 81, 82,<br>83, 84, 85, 86,<br>90, 91, 92, 93,<br>94, 95, 96, 97,<br>98, 3, 4, 5,<br>6, 7, 8, 9 | Input/Output Pins - These are the general purpose I/O pins used by the logic array.   |
| GOE 0, GOE 1  | 66, 87   | Global Output Enable input pins.  |
| Y0, Y1, Y2<br><br>$\overline{\text{RESET}}$   | 11, 65, 62<br><br>15   | Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.<br><br>Active Low (0) Reset pin which resets all of the registers in the device.  |
| $\overline{\text{ispEN}}$<br><br>SDI/IN 0 <sup>2</sup><br><br>MODE/IN 1 <sup>2</sup><br><br>SDO/IN 2 <sup>2</sup><br><br>SCLK/IN 3 <sup>2</sup>   | 14<br><br>16<br><br>37<br><br>39<br><br>60   | Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active.<br><br>Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.<br><br>Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.<br><br>Output/Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.<br><br>Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin. |
| GND<br>VCC<br>NC <sup>1</sup>   | 13, 38, 63, 88<br>12, 64<br>1, 2, 10, 24,<br>25, 26, 27, 49,<br>50, 51, 52, 61,<br>74, 75, 76, 77,<br>89, 99, 100  | Ground (GND)<br><br>V <sub>CC</sub><br><br>No Connect.  |

1. NC pins are not to be connected to any active signals, VCC or GND.

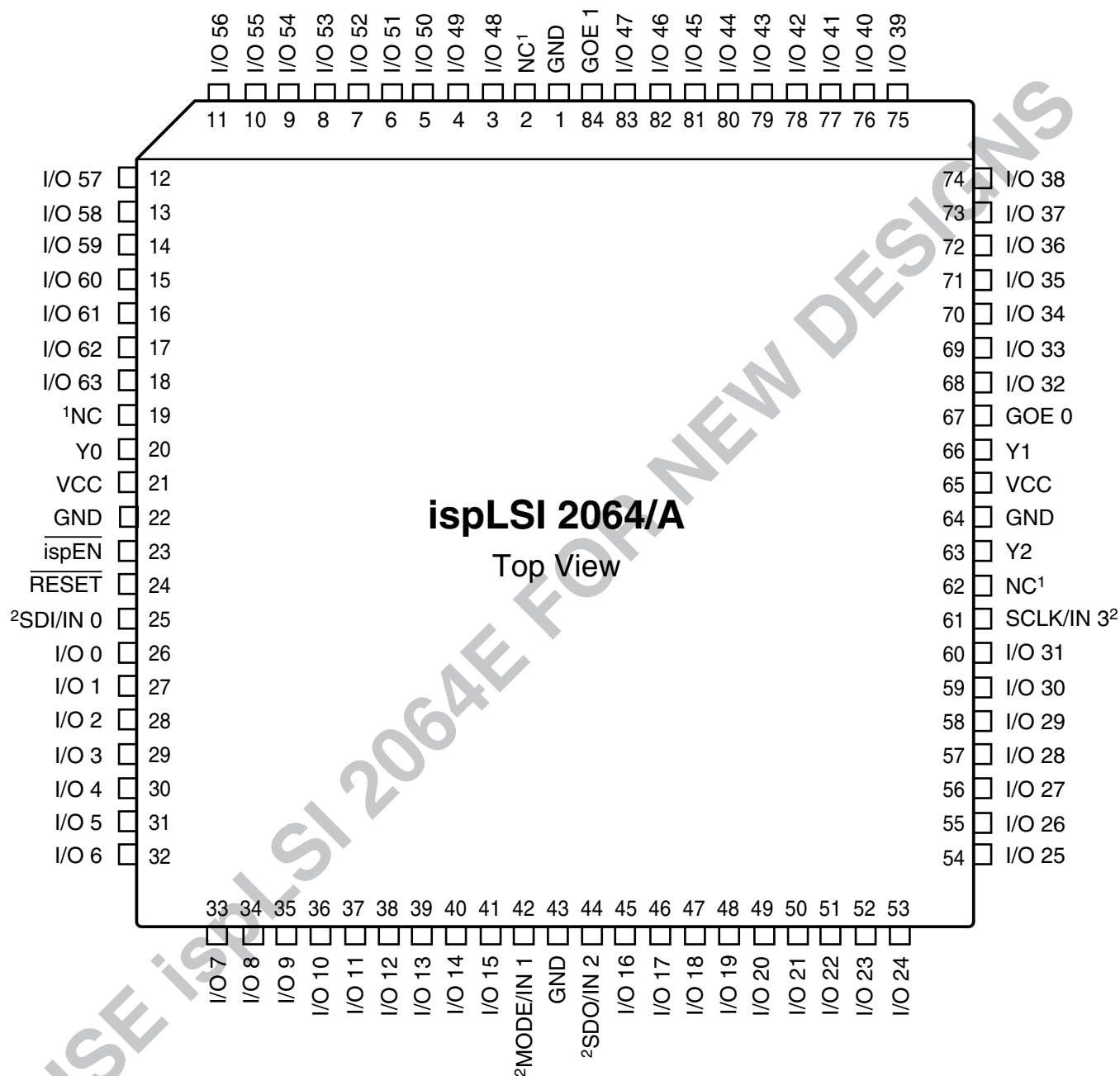
2. Pins have dual function capability.

Table 2-0002-2064b.eps

Select devices have been discontinued.  
See Ordering Information section for product status.

## Pin Configuration

ispLSI 2064/A 84-Pin PLCC Pinout Diagram

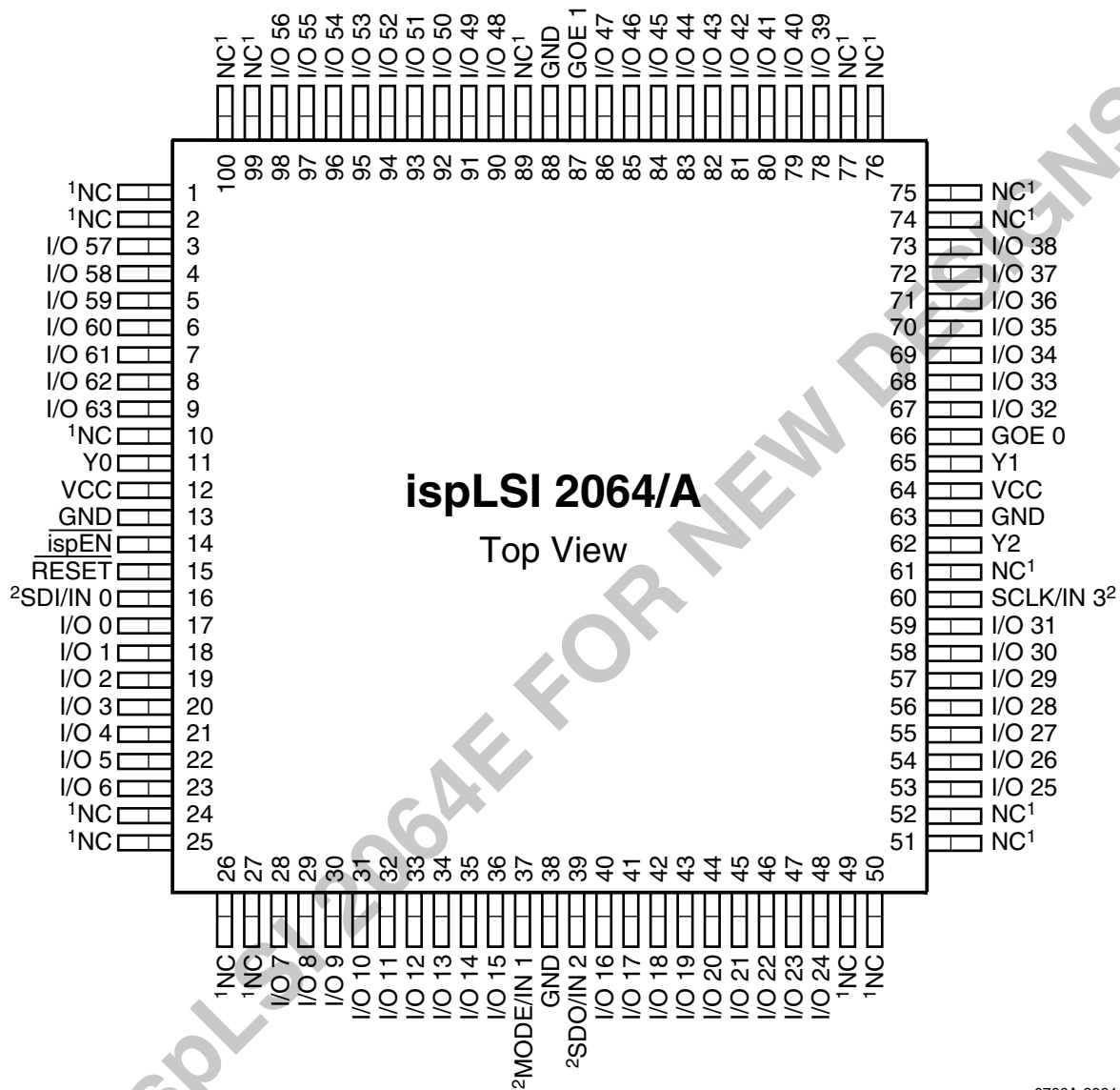


0123A/2064

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

## Pin Configuration

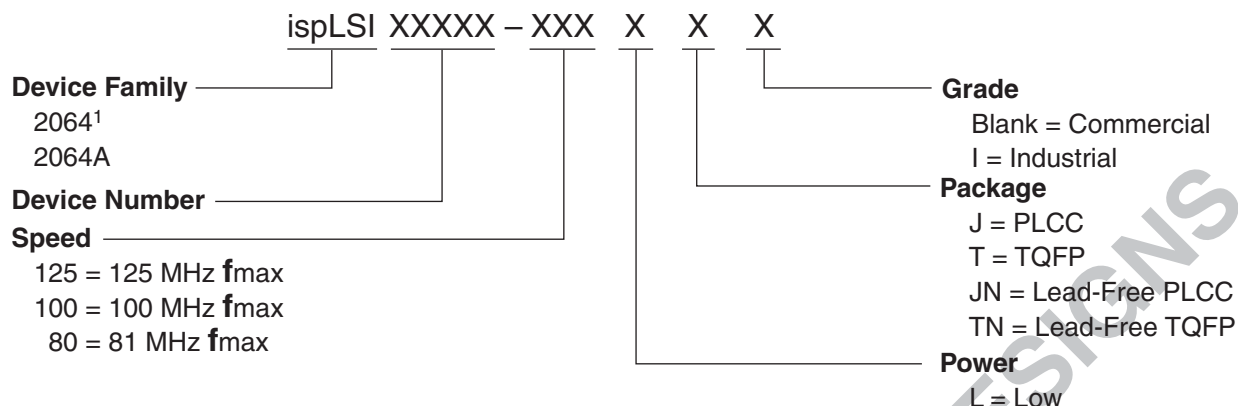
ispLSI 2064/A 100-Pin TQFP Pinout Diagram



0766A-2064-isp

Select devices have been discontinued.  
See Ordering Information section for product status.

## Part Number Description



1. Discontinued per PCN #02-06. Contact Rochester Electronics for available inventory.

## ispLSI 2064/A Ordering Information

### Conventional Packaging

#### COMMERCIAL

| FAMILY | $f_{max}$ (MHz) | tpd (ns) | ORDERING NUMBER                | PACKAGE      |
|--------|-----------------|----------|--------------------------------|--------------|
| ispLSI | 125             | 7.5      | ispLSI 2064A-125LJ84           | 84-Pin PLCC  |
|        | 125             | 7.5      | ispLSI 2064A-125LT100          | 100-Pin TQFP |
|        | 100             | 10       | ispLSI 2064A-100LJ84           | 84-Pin PLCC  |
|        | 100             | 10       | ispLSI 2064A-100LT100          | 100-Pin TQFP |
|        | 81              | 15       | ispLSI 2064A-80LJ84            | 84-Pin PLCC  |
|        | 81              | 15       | ispLSI 2064A-80LT100           | 100-Pin TQFP |
|        | 125             | 7.5      | ispLSI 2064-125LJ <sup>1</sup> | 84-Pin PLCC  |
|        | 125             | 7.5      | ispLSI 2064-125LT <sup>1</sup> | 100-Pin TQFP |
|        | 100             | 10       | ispLSI 2064-100LJ <sup>1</sup> | 84-Pin PLCC  |
|        | 100             | 10       | ispLSI 2064-100LT <sup>1</sup> | 100-Pin TQFP |
|        | 81              | 15       | ispLSI 2064-80LJ <sup>1</sup>  | 84-Pin PLCC  |
|        | 81              | 15       | ispLSI 2064-80LT <sup>1</sup>  | 100-Pin TQFP |

1. Discontinued per PCN #02-06. Contact Rochester Electronics for available inventory.

#### INDUSTRIAL

| FAMILY | $f_{max}$ (MHz) | tpd (ns) | ORDERING NUMBER                | PACKAGE      |
|--------|-----------------|----------|--------------------------------|--------------|
| ispLSI | 81              | 15       | ispLSI 2064A-80LJ84I           | 84-Pin PLCC  |
|        | 81              | 15       | ispLSI 2064A-80LT100I          | 100-Pin TQFP |
|        | 81              | 15       | ispLSI 2064-80LJI <sup>1</sup> | 84-Pin PLCC  |
|        | 81              | 15       | ispLSI 2064-80LTI <sup>1</sup> | 100-Pin TQFP |

1. Discontinued per PCN #02-06. Contact Rochester Electronics for available inventory.

Select devices have been discontinued.  
See Ordering Information section for product status.

## ispLSI 2064/A Ordering Information (Cont.)

### Lead-Free Packaging

#### COMMERCIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER                    | PACKAGE                |
|--------|------------|----------|------------------------------------|------------------------|
| ispLSI | 125        | 7.5      | ispLSI 2064A-125LJN84 <sup>1</sup> | Lead-Free 84-Pin PLCC  |
|        | 125        | 7.5      | ispLSI 2064A-125LTN100             | Lead-Free 100-Pin TQFP |
|        | 100        | 10       | ispLSI 2064A-100LJN84 <sup>1</sup> | Lead-Free 84-Pin PLCC  |
|        | 100        | 10       | ispLSI 2064A-100LTN100             | Lead-Free 100-Pin TQFP |
|        | 81         | 15       | ispLSI 2064A-80LJN84 <sup>1</sup>  | Lead-Free 84-Pin PLCC  |
|        | 81         | 15       | ispLSI 2064A-80LTN100              | Lead-Free 100-Pin TQFP |

1. 84-PLCC lead-free package is MSL4. Refer to "Handling Moisture Sensitive Packages" document on [www.latticesemi.com](http://www.latticesemi.com).

#### INDUSTRIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER                    | PACKAGE                |
|--------|------------|----------|------------------------------------|------------------------|
| ispLSI | 81         | 15       | ispLSI 2064A-80LJN84I <sup>1</sup> | Lead-Free 84-Pin PLCC  |
|        | 81         | 15       | ispLSI 2064A-80LTN100I             | Lead-Free 100-Pin TQFP |

1. 84-PLCC lead-free package is MSL4. Refer to "Handling Moisture Sensitive Packages" document on [www.latticesemi.com](http://www.latticesemi.com).

### Revision History

| Date        | Version | Change Summary                         |
|-------------|---------|--|
| —           | 09      | Previous Lattice release.              |
| August 2006 | 10      | Updated for lead-free package options. |

Select devices have been discontinued.  
See Ordering Information section for product status.