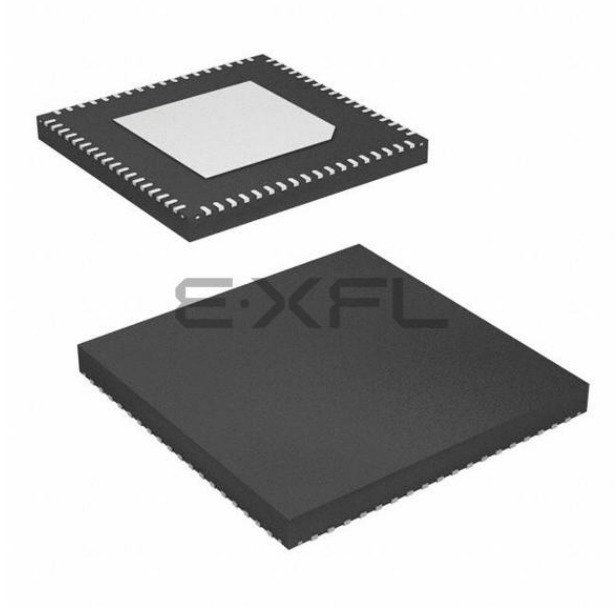

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	147.456MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	192kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	72-VFQFN Exposed Pad, CSP
Supplier Device Package	72-LFCSP-VQ (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1462wbcpz150

Auxiliary ADC

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, AVDD = 3.3 V ± 10%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit
RESOLUTION		10		Bits
FULL-SCALE ANALOG INPUT		AVDD		V
NONLINEARITY				
Integrated Nonlinearity (INL)	−2.5		+2.5	LSB
Differential Nonlinearity (DNL)	−2.5		+2.5	LSB
GAIN ERROR	−2.5		+2.5	LSB
INPUT IMPEDANCE		200		kΩ
SAMPLE RATE		f_{CORE}/6144		Hz

PDM Inputs

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%. Pulse density modulation (PDM) data is latched on both edges of the clock (see Figure 10).

Table 15.

Parameter	t_{MIN}	t_{MAX}	Unit	Description
t_{SETUP}	10		ns	Data setup time
t_{HOLD}	5		ns	Data hold time

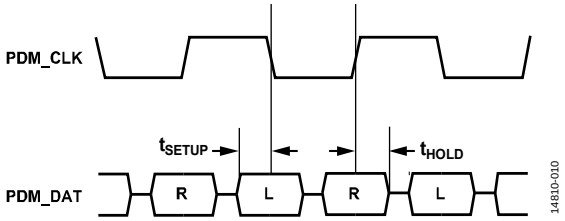


Figure 10. PDM Timing Diagram

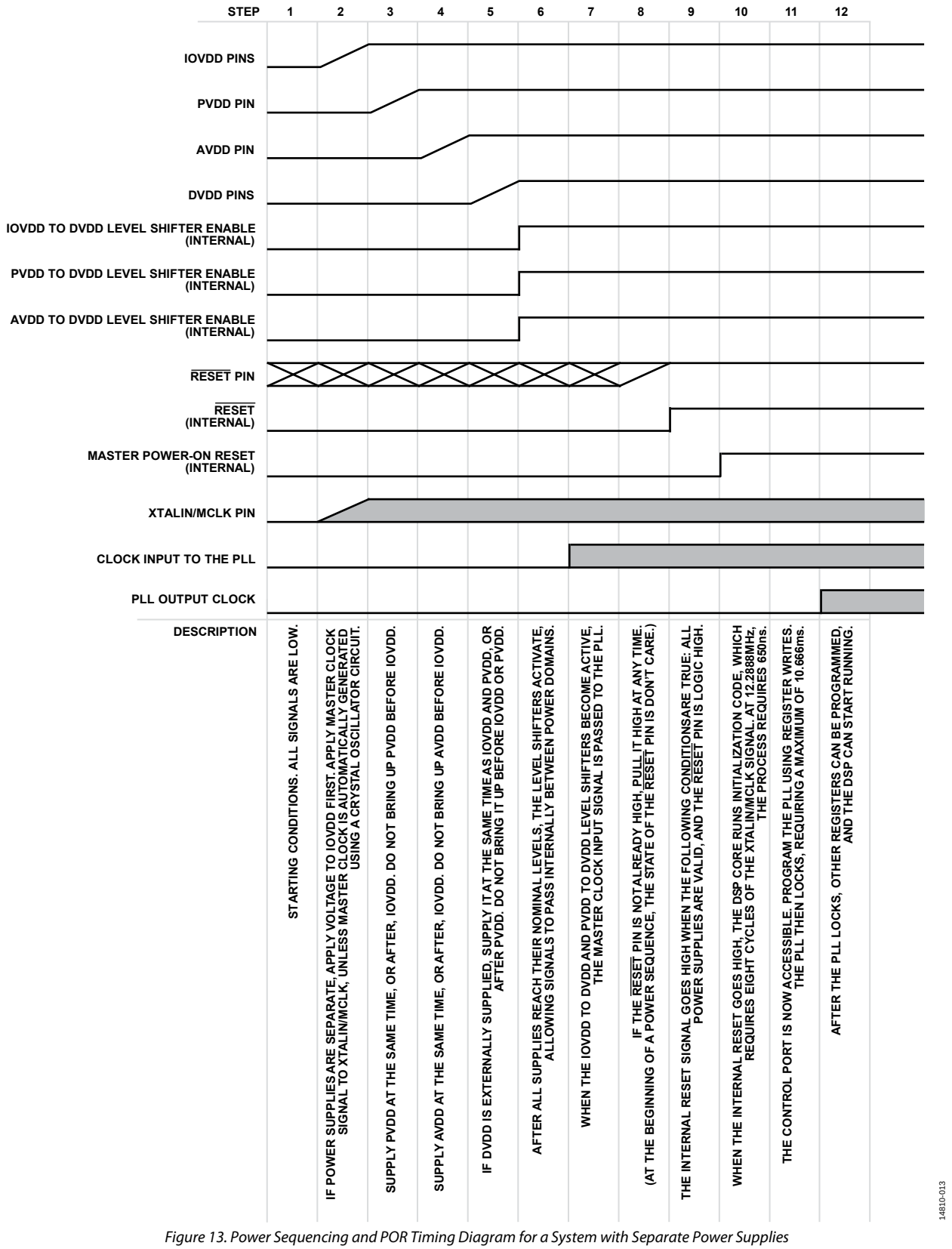


Figure 13. Power Sequencing and POR Timing Diagram for a System with Separate Power Supplies

SLAVE CONTROL PORTS

A total of four control ports are available: two slave ports and two master ports. The slave I²C port and slave SPI port allow an external master device to modify the contents of the memory and registers. The master I²C port and master SPI port allow the device to self boot and to send control messages to slave devices on the same bus.

Slave Control Port Overview

To program the DSP and configure the control registers, a slave port is available that can communicate using either the I²C or SPI protocols. Any external device that controls the ADAU1462/ADAU1466, including a hardware interface used with SigmaStudio for development or a microcontroller in a large running system, uses the slave control port to communicate with the DSP. This port is unrelated to the master communications port that also uses the I²C or SPI protocols. The master port enables applications without an external controller and can read from an external EEPROM to self boot and control external ICs.

The slave communications port defaults to I²C mode; however, it can be put into SPI mode by toggling SS (SS/ADDR0), the slave select pin, from high to low three times. The slave select pin must be held low for at least one master clock period (that is, one period of the clock on the XTALIN_MCLK input pin). Only the PLL configuration registers (0xF000 to 0xF004) are accessible before the PLL locks. For this reason, always write to the PLL registers first after the chip powers up. After the PLL locks, the remaining registers and the RAM become accessible. See the System Initialization Sequence section for more information.

SLAVE CONTROL PORT ADDRESSING

Unlike earlier SigmaDSP processors, the ADAU1462/ADAU1466 slave control port 16-bit addressing cannot provide direct access to the total amount of memory available to the DSP core on its wider internal busses. Full read/write access to all memory and addressable registers is possible, but it must be accessed as two pages of memory in the slave control port address space. Page 0 is referred to as lower memory and Page 1 as upper memory. The single-bit register SECONDPAGE_ENABLE (0xF899) selects the active page.

Within a page, all addresses are accessible using both single address mode and burst mode. The first byte (Byte 0) of a control port write contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the register location within the memory maps of the ADAU1462/ADAU1466. This subaddress must be two bytes long because the memory locations within the devices are directly addressable, and their sizes exceed the range of single byte addressing. The third byte to the end of the sequence contain the data, such as control port data, program data, or parameter data. The number of bytes written per word depends on the type of data. For more information, see the Burst Mode Writing and Reading section. The ADAU1462/ADAU1466 must have a valid master clock to write to the slave control port, with the exception of the PLL configuration registers, 0xF000 to 0xF004.

If large blocks of data must be downloaded, halt the output of the DSP core (using Register 0xF400, HIBERNATE), load new data, and then restart the device (using Register 0xF402, START_CORE). This process is most common during the booting sequence at startup or when loading a new program into RAM because the ADAU1462/ADAU1466 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks.

When updating a signal processing parameter while the DSP core is running, use the software safeload function. This function allows atomic writes to memory and prevents updates to parameters across the boundary of an audio frame, which can lead to an audio artifact such as a click or pop sound. For more information, see the Software Safeload section.

The slave control port supports either I²C or SPI, but not simultaneously. The function of each pin is described in Table 25 for the two modes.

Burst Mode Writing and Reading

Burst write and read modes are available for convenience when writing large amounts of data to contiguous registers. In these modes, the chip and memory addresses are written once, and then a large amount of data can follow uninterrupted. The subaddresses are automatically incremented at the word boundaries. This increment happens automatically after a single word write or read unless a stop condition is encountered (I²C mode) or the slave select is disabled and brought high (SPI mode). A burst write starts like a single word write, but, following the first data-word, the data-word for the next address can be written immediately without sending its 2-byte address. The control registers in the ADAU1462/ADAU1466 are two bytes wide, and the memories are four bytes wide. The auto-increment feature knows the word length at each subaddress; therefore, it is not necessary to manually specify the subaddress for each address in a burst write.

The subaddresses are automatically incremented by one address, following each read or write of a data-word, regardless of whether there is a valid register or RAM word at that address.

I²C Slave Port

The ADAU1462/ADAU1466 support a 2-wire serial (I²C compatible) microprocessor bus driving multiple peripherals. The maximum clock frequency on the I²C slave port is 400 kHz. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAU1462/ADAU1466 and the system I²C master controller. In I²C mode, the ADAU1462/ADAU1466 are always slaves on the bus, meaning that they cannot initiate a data transfer. Each slave device is recognized by a unique address. The address bit sequence and the format of the read/write byte is shown in Table 26. The address resides in the first seven bits of the I²C write. The two address bits that follow can be set to assign the I²C slave address of the device, as follows: Bit 1 can be set by pulling the SS/ADDR0 pin either to IOVDD (by setting it to 1) or to DGND (by setting it to 0); and Bit 2 can be set by pulling the MOSI/ADDR1 pin either to IOVDD (by setting it to 1) or to DGND (by setting it to 0). The LSB of the address (the R/$\overline{W}$ bit) either specifies a read or write operation. Logic Level 1 corresponds to a read operation; Logic Level 0 corresponds to a write operation.

Table 26 describes the sequence of eight bits that define the I²C device address byte.

Table 27 describes the relationship between the state of the address pins (0 represents logic low and 1 represents logic high) and the I²C slave address. Ensure that the address pins (SS/ADDR0 and MOSI/ADDR1) are hardwired in the design. Do not allow these pins to change states while the device is operating.

Place a 2 kΩ pull-up resistor on each line connected to the SDA and SCL pins. Ensure that the voltage on these signal lines does not exceed IOVDD (1.8 V − 5% to 3.3 V + 10%).

Addressing

Initially, each device on the I²C bus is in an idle state and monitors the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCL remains high. This start condition indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit), MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition.

The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral, whereas a Logic 1 means that the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer occurs until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high.

Figure 28 shows the timing of an I²C single word write operation, Figure 29 shows the timing of an I²C burst mode write operation, and Figure 30 shows an I²C burst mode read operation.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the slave I²C port of the ADAU1462/ADAU1466 immediately jumps to the idle condition. During a given SCL high period, issue only one start condition and one stop condition, or a single stop condition followed by a single start condition. If the user issues an invalid subaddress, the ADAU1462/ADAU1466 do not issue an acknowledge and return to the idle condition.

Note the following conditions:

- Do not issue an autoincrement (burst) write command that exceeds the highest subaddress in the memory.
- Do not issue an autoincrement (burst) write command that writes to subaddresses that are not defined in the Global RAM and Control Register Map section.

Table 26. Address Bit Sequence

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	ADDR1 (set by the MOSI/ADDR1 pin)	ADDR0 (set by the SS/ADDR0 pin)	R/$\overline{W}$

Table 27. I²C Slave Addresses

MOSI/ADDR1	SS/ADDR0	Read/$\overline{Write}$[1]	Slave Address (Eight Bits, Including R/$\overline{W}$ Bit)	Slave Address (Seven Bits, Excluding R/$\overline{W}$ Bit)
0	0	0	0x70	0x38
0	0	1	0x71	0x38
0	1	0	0x72	0x39
0	1	1	0x73	0x39
1	0	0	0x74	0x3A
1	0	1	0x75	0x3A
1	1	0	0x76	0x3B
1	1	1	0x77	0x3B

[1] 0 means write, 1 means read.

PLL Lock Register

Address: 0xF004, Reset: 0x0000, Name: PLL_LOCK

This register contains a flag that represents the lock status of the PLL. Lock status has four prerequisites: a stable input clock is being routed to the PLL, the related PLL registers (Register 0xF000 (PLL_CTRL0), Register 0xF001 (PLL_CTRL1), and Register 0xF002 (PLL_CLK_SRC)) are set appropriately, the PLL is enabled (Register 0xF003 (PLL_ENABLE), Bit 0 (PLL_ENABLE) = 0b1), and the PLL has had adequate time to adjust its feedback path and provide a stable output clock to the rest of the device. The amount of time required to achieve lock to a new input clock signal varies based on system conditions, so Bit 0 (PLL_LOCK) provides a clear indication of when lock has been achieved.

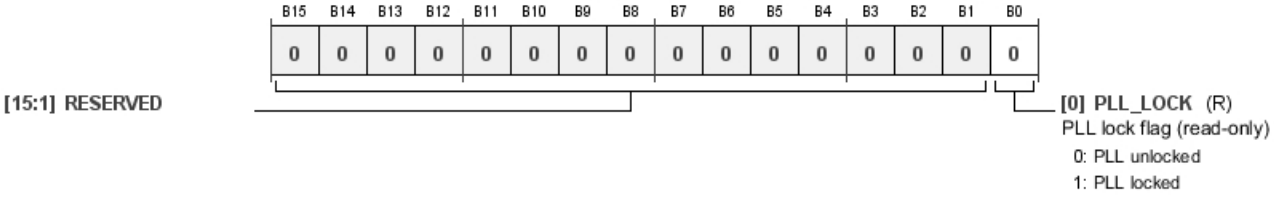


Table 63. Bit Descriptions for PLL_LOCK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PLL_LOCK		PLL lock flag (read only).	0x0	R
		0	PLL unlocked		
		1	PLL locked		

Analog PLL Watchdog Control Register

Address: 0xF006, Reset: 0x0001, Name: PLL_WATCHDOG

The PLL watchdog is a feature that monitors the PLL and automatically resets it in the event that it reaches an unstable condition. The PLL resets itself and automatically attempts to lock to the incoming clock signal again, with the same settings as before. This functionality requires no interaction on the part of the user. Ensure that the PLL watchdog is enabled at all times.

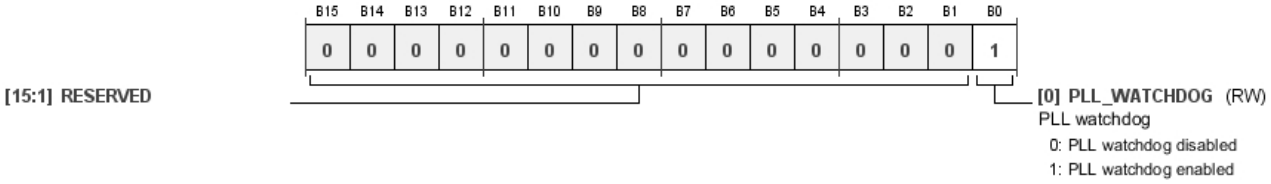


Table 65. Bit Descriptions for PLL_WATCHDOG

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PLL_WATCHDOG		PLL watchdog.	0x1	RW
		0	PLL watchdog disabled		
		1	PLL watchdog enabled		

CLOCK GENERATOR REGISTERS

Denominator (M) for Clock Generator 1 Register

Address: 0xF020, Reset: 0x0006, Name: CLK_GEN1_M

This register contains the denominator (M) for Clock Generator 1.

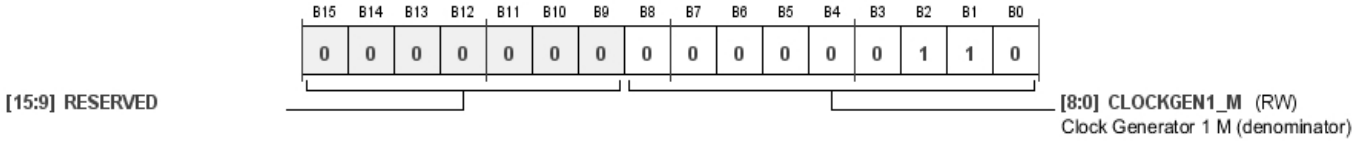


Table 66. Bit Descriptions for CLK_GEN1_M

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	RESERVED			0x0	RW
[8:0]	CLOCKGEN1_M		Clock Generator 1 M (denominator). Format is binary integer.	0x006	RW

Numerator (N) for Clock Generator 1 Register

Address: 0xF021, Reset: 0x0001, Name: CLK_GEN1_N

This register contains the numerator (N) for Clock Generator 1.

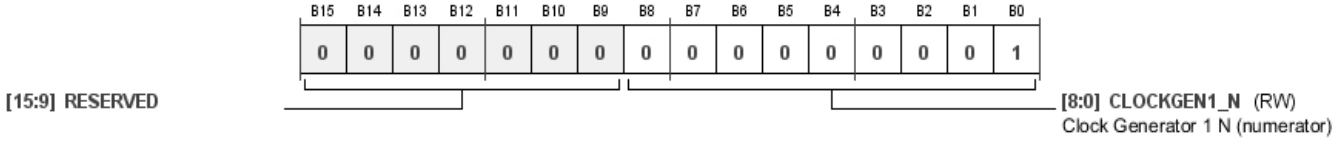


Table 67. Bit Descriptions for CLK_GEN1_N

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	RESERVED			0x0	RW
[8:0]	CLOCKGEN1_N		Clock Generator 1 N (numerator). Format is binary integer.	0x001	RW

Denominator (M) for Clock Generator 2 Register

Address: 0xF022, Reset: 0x0009, Name: CLK_GEN2_M

This register contains the denominator (M) for Clock Generator 2.

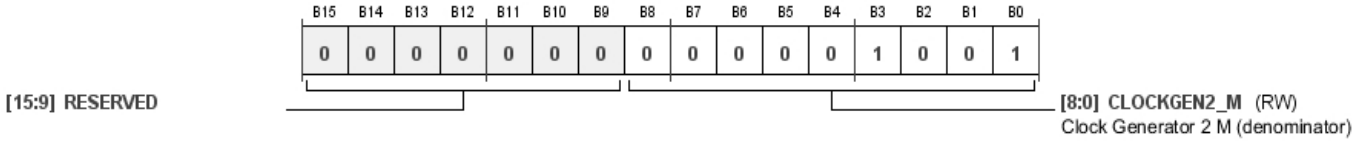


Table 68. Bit Descriptions for CLK_GEN2_M

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	RESERVED			0x0	RW
[8:0]	CLOCKGEN2_M		Clock Generator 2 M (denominator). Format is binary integer.	0x009	RW

Table 72. Bit Descriptions for CLK_GEN3_SRC

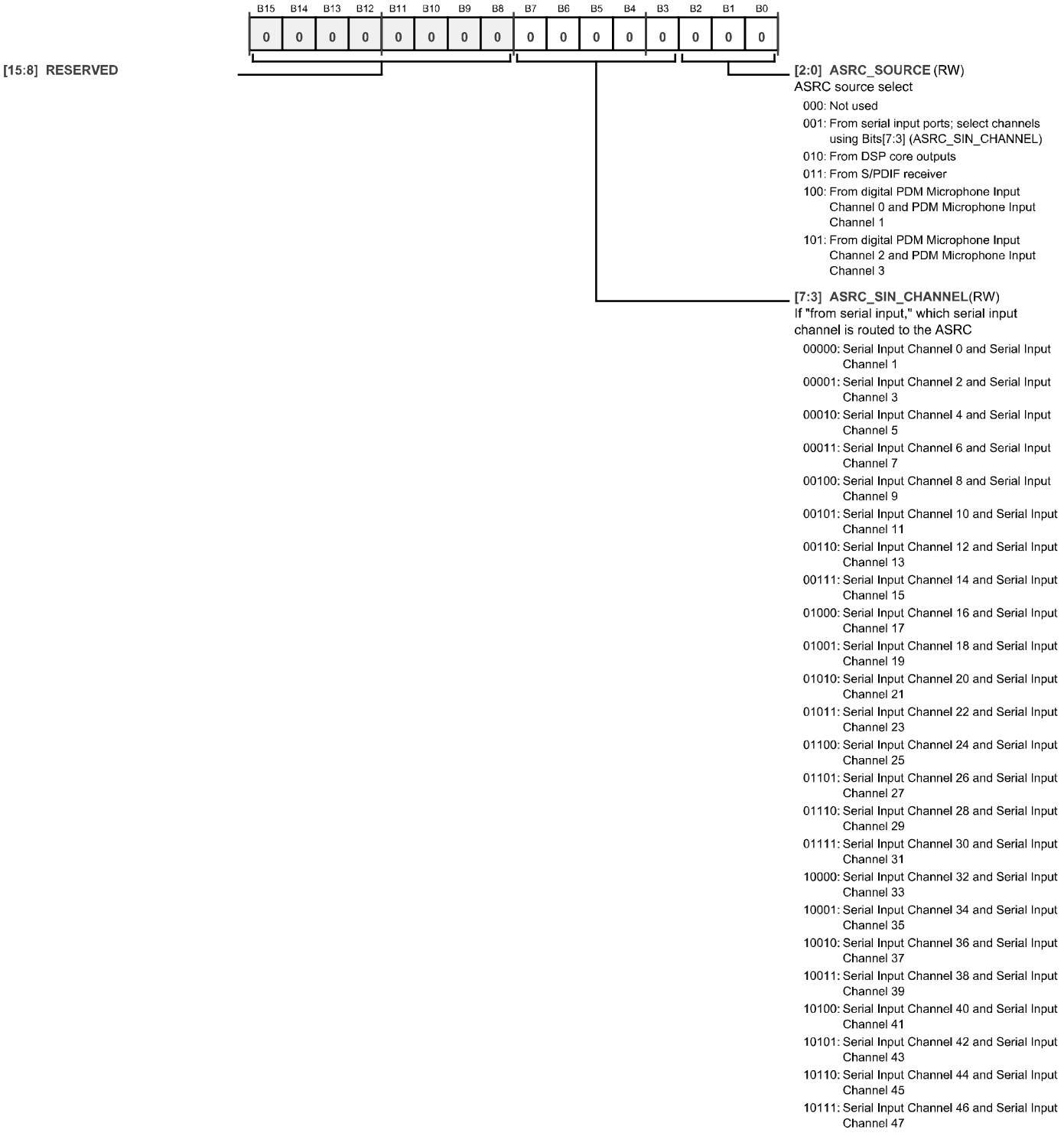
Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	CLK_GEN3_SRC		Reference source for Clock Generator 3. This bit selects the reference of Clock Generator 3. If set to use an external reference clock, Bits[3:0] define the source pin. Otherwise, the PLL output is used as the reference clock. When an external reference clock is used for Clock Generator 3, the resulting base output frequency of Clock Generator 3 is the frequency of the input reference clock multiplied by the Clock Generator 3 numerator, divided by 1024. For example: if Bit 4 (CLK_GEN3_SRC) = 0b1 (an external reference clock is used); Bits[3:0] (FREF_PIN) = 0b1110 (the input signal of the S/PDIF receiver is used as the reference source); the sample rate of the S/PDIF input signal = 48 kHz; and the numerator of Clock Generator 3 = 2048; the resulting base output sample rate of Clock Generator 3 is 48 kHz × 2048/1024 = 96 kHz.	0x0	RW
		0	Reference signal provided by PLL output; multiply the frequency of that signal by N and divide it by M.		
		1	Reference signal provided by the signal input to the hardware pin defined by Bits[3:0] (FREF_PIN); multiply the frequency of that signal by N (and then divide by 1024) to get the resulting sample rate. M is ignored.		
[3:0]	FREF_PIN		Input reference for Clock Generator 3. If Clock Generator 3 is set up to lock to an external reference clock (Bit 4 (CLK_GEN3_SRC) = 0b1), these bits allow the user to specify which pin is receiving the reference clock. The signal input to the corresponding pin must be a 50% duty cycle square wave clock representing the reference sample rate.	0xE	RW
		0000	Input reference source is SS_M/MP0		
		0001	Input reference source is MOSI_M/MP1		
		0010	Input reference source is SCL_M/SCLK_M/MP2		
		0011	Input reference source is SDA_M/MISO_M/MP3		
		0100	Input reference source is LRCLK_OUT0/MP4		
		0101	Input reference source is LRCLK_OUT1/MP5		
		0110	Input reference source is MP6		
		0111	Input reference source is MP7		
		1000	Input reference source is LRCLK_OUT2/MP8		
		1001	Input reference source is LRCLK_OUT3/MP9		
		1010	Input reference source is LRCLK_IN0/MP10		
		1011	Input reference source is LRCLK_IN1/MP11		
		1100	Input reference source is LRCLK_IN2/MP12		
		1101	Input reference source is LRCLK_IN3/MP13		
		1110	Input reference source is S/PDIF receiver (recovered frame clock)		

AUDIO SIGNAL ROUTING REGISTERS

ASRC Input Selector Register

Address: 0xF100 to Address 0xF107 (Increments of 0x1), Reset: 0x0000, Name: ASRC_INPUTx

These eight registers configure the input signal to the corresponding eight stereo ASRCs on the ADAU1466 and ADAU1462. ASRC_INPUT0 configures ASRC Channel 0 and ASRC Channel 1, ASRC_INPUT1 configures ASRC Channel 2 and ASRC Channel 3, and so on. Valid input signals to the ASRCs include Serial Input Channel 0 to Serial Input Channel 47, the PDM Microphone Input Channel 0 to PDM Microphone Input Channel 3, and the S/PDIF Receiver Channel 0 to S/PDIF Receiver Channel 1.



Bits	Bit Name	Settings	Description	Reset	Access
[2:0]	SOUT_SOURCE		Audio data source for these serial audio output channels. If these bits are set to 0b001, the corresponding output channels output a copy of the data from the corresponding input channels. For example, if Address 0xF180, Bits[2:0] are set to 0b001, Serial Input Channel 0 and Serial Input Channel 1 copy to Serial Output Channel 0 and Serial Output Channel 1, respectively. If these bits are set to 0b010, DSP Output Channel 0 and DSP Output Channel 1 copy to Serial Output Channel 0 and Serial Output Channel 1, respectively. If these bits are set to 0b011, Bits[5:3] (SOUT_ASRC_SELECT) must be configured to select the desired ASRC output.	0x0	RW
		000	Disabled; these output channels are not used		
		001	Direct copy of data from corresponding serial input channels		
		010	Data from corresponding DSP core output channels		
		011	From ASRC (select channel using Bits[5:3], SOUT_ASRC_SELECT)		
		100	Digital PDM Microphone Input Channel 0 and Digital PDM Microphone Input Channel 1		
		101	Digital PDM Microphone Input Channel 2 and Digital PDM Microphone Input Channel 3		

S/PDIF Transmitter Data Selector Register

Address: 0xF1C0, Reset: 0x0000, Name: SPDIFTX_INPUT

This register configures which data source feeds the S/PDIF transmitter on the ADAU1466 and ADAU1462. Data can originate from the S/PDIF outputs of the DSP core or directly from the S/PDIF receiver.

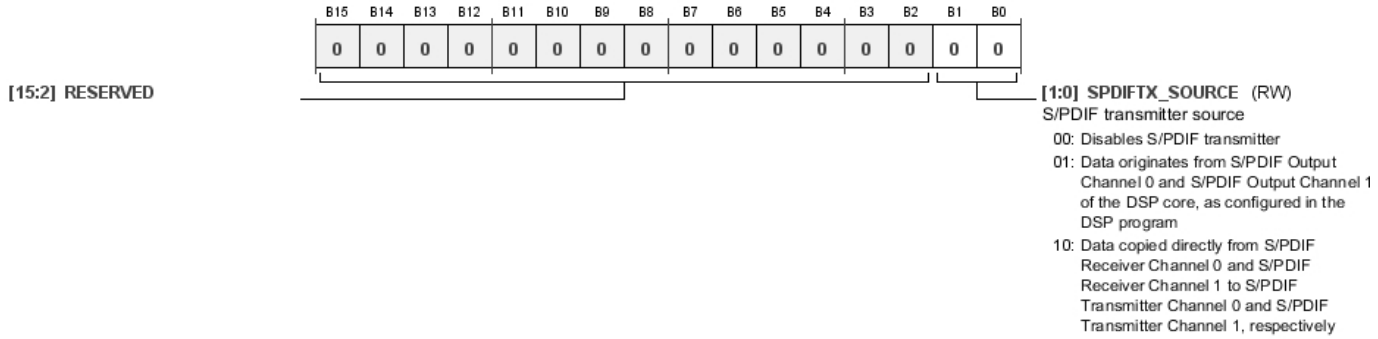


Table 79. Bit Descriptions for SPDIFTX_INPUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:2]	RESERVED			0x0	RW
[1:0]	SPDIFTX_SOURCE		S/PDIF transmitter source.	0x0	RW
		00	Disables S/PDIF transmitter		
		01	Data originates from S/PDIF Output Channel 0 and S/PDIF Output Channel 1 of the DSP core, as configured in the DSP program		
		10	Data copied directly from S/PDIF Receiver Channel 0 and S/PDIF Receiver Channel 1 to S/PDIF Transmitter Channel 0 and S/PDIF Transmitter Channel 1, respectively		

Bits	Bit Name	Settings	Description	Reset	Access
[4:3]	DATA_FMT		MSB position. These bits set the positioning of the data in the frame on the corresponding serial port.	0x0	RW
		00	I²S (delay data by one BCLK cycle)		
		01	Left justified (delay data by zero BCLK cycles)		
		10	Right justified for 24-bit data (delay data by 8 BCLK cycles)		
		11	Right justified for 16-bit data (delay data by 16 BCLK cycles)		
[2:0]	TDM_MODE		Channels per frame and BCLK cycles per channel. These bits set the number of channels per frame and the number of bit clock cycles per frame on the corresponding serial port.	0x0	RW
		000	2 channels, 32 bit clock cycles per channel, 64 bit clock cycles per frame		
		001	4 channels, 32 bit clock cycles per channel, 128 bit clock cycles per frame		
		010	8 channels, 32 bit clock cycles per channel, 256 bit clock cycles per frame		
		011	16 channels, 32 bit clock cycles per channel, 512 bit clock cycles per frame		
		100	4 channels, 16 bit clock cycles per channel, 64 bit clock cycles per frame		
		101	2 channels, 16 bit clock cycles per channel, 32 bit clock cycles per frame		

Serial Port Control 1 Register

Address: 0xF201 to 0xF21D (Increments of 0x4), Reset: 0x0002, Name: SERIAL_BYTE_x_1

These eight registers configure several settings for the corresponding serial input and serial output ports. Clock generator, sample rate, and behavior during inactive channels are configured with these registers. On the input side, Register 0xF201 (SERIAL_BYTE_0_1) corresponds to SDATA_IN0; Register 0xF205 (SERIAL_BYTE_1_1) corresponds to SDATA_IN1; Register 0xF209 (SERIAL_BYTE_2_1) corresponds to SDATA_IN2; and Register 0xF20D (SERIAL_BYTE_3_1) corresponds to SDATA_IN3. On the output side, Register 0xF211 (SERIAL_BYTE_4_1) corresponds to SDATA_OUT0; Register 0xF215 (SERIAL_BYTE_5_1) corresponds to SDATA_OUT1; Register 0xF219 (SERIAL_BYTE_6_1) corresponds to SDATA_OUT2; and Register 0xF21D (SERIAL_BYTE_7_1) corresponds to SDATA_OUT3.

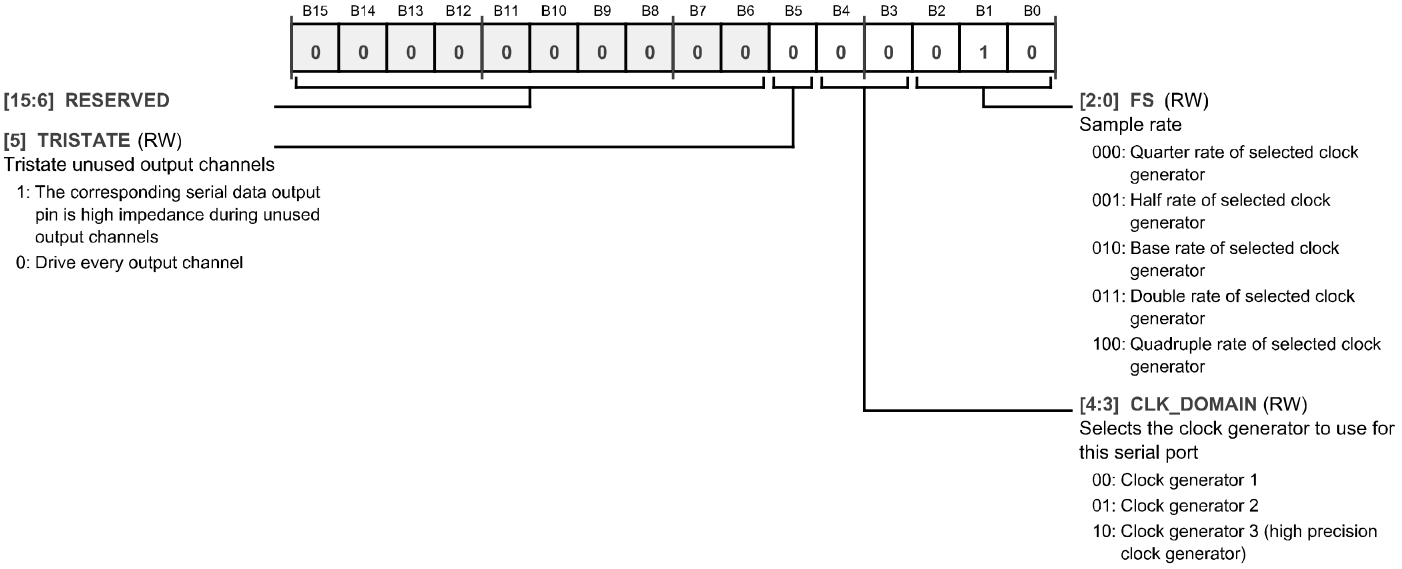


Table 81. Bit Descriptions for SERIAL_BYTE_x_1

Bits	Bit Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x000	RW
5	TRISTATE		Tristate unused output channels. This bit has no effect on serial input ports.	0x0	RW
		1	The corresponding serial data output pin is high impedance during unused output channels		
		0	Drive every output channel		

Core Status Register

Address: 0xF405, Reset: 0x0000, Name: CORE_STATUS

This read only register allows the user to check the status of the DSP core. To manually modify the core status, use Register 0xF400 (HIBERNATE), Register 0xF402 (START_CORE), and Register 0xF403 (KILL_CORE).

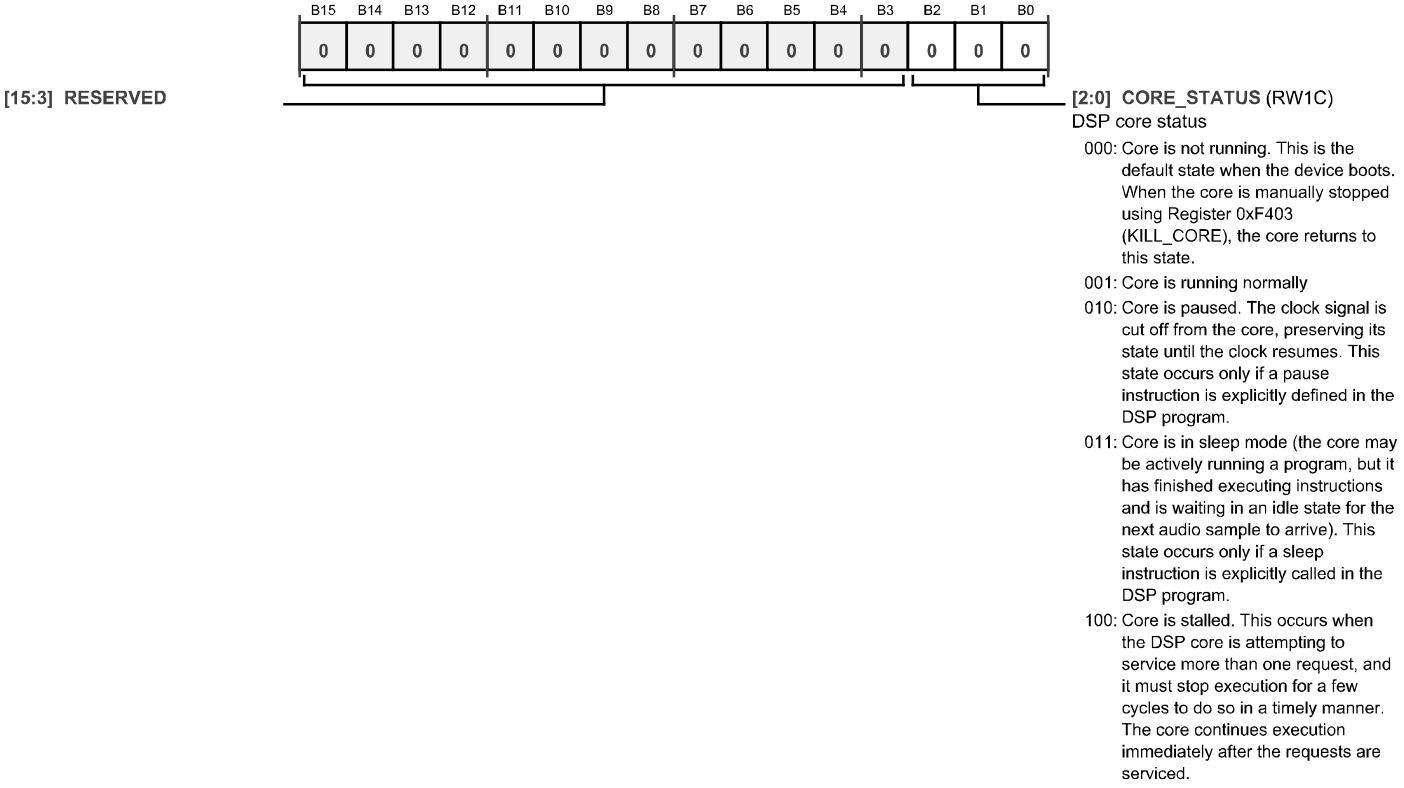


Table 89. Bit Descriptions for CORE_STATUS

Bits	Bit Name	Settings	Description	Reset	Access
[15:3]	RESERVED			0x0	RW
[2:0]	CORE_STATUS		DSP core status. These bits display the status of the DSP core at the moment the value is read.	0x0	RW
		000	Core is not running. This is the default state when the device boots. When the core is manually stopped using Register 0xF403 (KILL_CORE), the core returns to this state.		
		001	Core is running normally.		
		010	Core is paused. The clock signal is cut off from the core, preserving its state until the clock resumes. This state occurs only if a pause instruction is explicitly defined in the DSP program.		
		011	Core is in sleep mode (the core may be actively running a program, but it has finished executing instructions and is waiting in an idle state for the next audio sample to arrive). This state occurs only if a sleep instruction is explicitly called in the DSP program.		
		100	Core is stalled. This occurs when the DSP core is attempting to service more than one request, and it must stop execution for a few cycles to do so in a timely manner. The core continues execution immediately after the requests are serviced.		

Bits	Bit Name	Settings	Description	Reset	Access
5	DM0_BANK1_MASK		DM0 Bank 1 mask.	0x0	RW
		0	Report DM0_BANK1 parity mask errors		
		1	Do not report DM0_BANK1 parity mask errors		
4	DM0_BANK0_MASK		DM0 Bank 0 mask.	0x0	RW
		0	Report DM0_BANK0 parity mask errors		
		1	Do not report DM0_BANK0 parity mask errors		
3	PM1_MASK		PM1 parity mask.	0x0	RW
		0	Report PM1 parity mask errors		
		1	Do not report PM1 parity mask errors		
2	PM0_MASK		PM0 parity mask.	0x0	RW
		0	Report PM0 parity mask errors		
		1	Do not report PM0 parity mask errors		
1	ASRC1_MASK		ASRC 1 parity mask.	0x1	RW
		0	Report ASRC 1 parity mask errors		
		1	Do not report ASRC 1 parity mask errors		
0	ASRC0_MASK		ASRC 0 parity mask.	0x1	RW
		0	Report ASRC 0 parity mask errors		
		1	Do not report ASRC 0 parity mask errors		

Panic Mask 0 Register

Address: 0xF423, Reset: 0x0000, Name: PANIC_SOFTWARE_MASK

The panic manager checks and reports software errors. Register 0xF423 (PANIC_SOFTWARE_MASK) allows the user to configure whether software errors are reported to the panic manager or ignored.

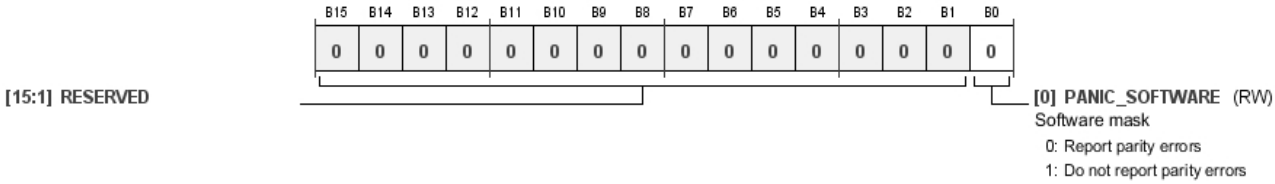


Table 92. Bit Descriptions for PANIC_SOFTWARE_MASK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PANIC_SOFTWARE		Software mask.	0x0	RW
		0	Report parity errors		
		1	Do not report parity errors		

Panic Parity Error PM Bank [1:0] Register

Address: 0xF470, Reset: 0x0000, Name: PANIC_CODE5

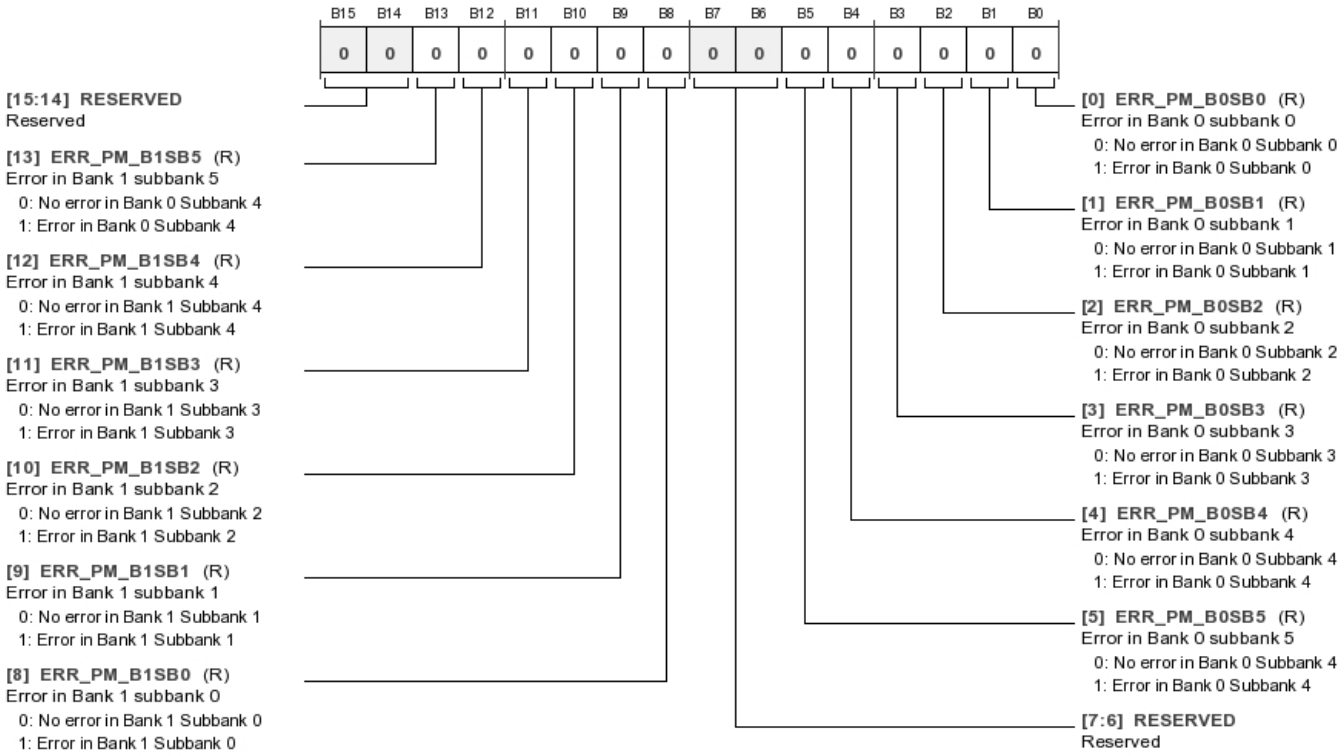


Table 121. Bit Descriptions for PANIC_CODE5

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	RESERVED		Reserved.	0x0	RW
13	ERR_PM_B1SB5		Error in Bank 1 Subbank 5.	0x0	R
		0	No error in Bank 0 Subbank 4		
		1	Error in Bank 0 Subbank 4		
12	ERR_PM_B1SB4		Error in Bank 1 Subbank 4.	0x0	R
		0	No error in Bank 1 Subbank 4		
		1	Error in Bank 1 Subbank 4		
11	ERR_PM_B1SB3		Error in Bank 1 Subbank 3.	0x0	R
		0	No error in Bank 1 Subbank 3		
		1	Error in Bank 1 Subbank 3		
10	ERR_PM_B1SB2		Error in Bank 1 Subbank 2.	0x0	R
		0	No error in Bank 1 Subbank 2		
		1	Error in Bank 1 Subbank 2		
9	ERR_PM_B1SB1		Error in Bank 1 Subbank 1.	0x0	R
		0	No error in Bank 1 Subbank 1		
		1	Error in Bank 1 Subbank 1		
8	ERR_PM_B1SB0		Error in Bank 1 Subbank 0.	0x0	R
		0	No error in Bank 1 Subbank 0		
		1	Error in Bank 1 Subbank 0		
[7:6]	RESERVED		Reserved.	0x0	RW
5	ERR_PM_B0SB5		Error in Bank 0 Subbank 5.	0x0	R
		0	No error in Bank 0 Subbank 4		
		1	Error in Bank 0 Subbank 4		

Digital PDM Microphone Control Register

Address: 0xF560 to 0xF561 (Increments of 0x1), Reset: 0x4000, Name: DMIC_CTRLx

These registers configure the digital PDM microphone interface. Two registers are used to control up to four PDM microphones: Register 0xF560 (DMIC_CTRL0) configures PDM Microphone Channel 0 and PDM Microphone Channel 1, and Register 0xF561 (DMIC_CTRL1) configures PDM Microphone Channel 2 and PDM Microphone Channel 3.

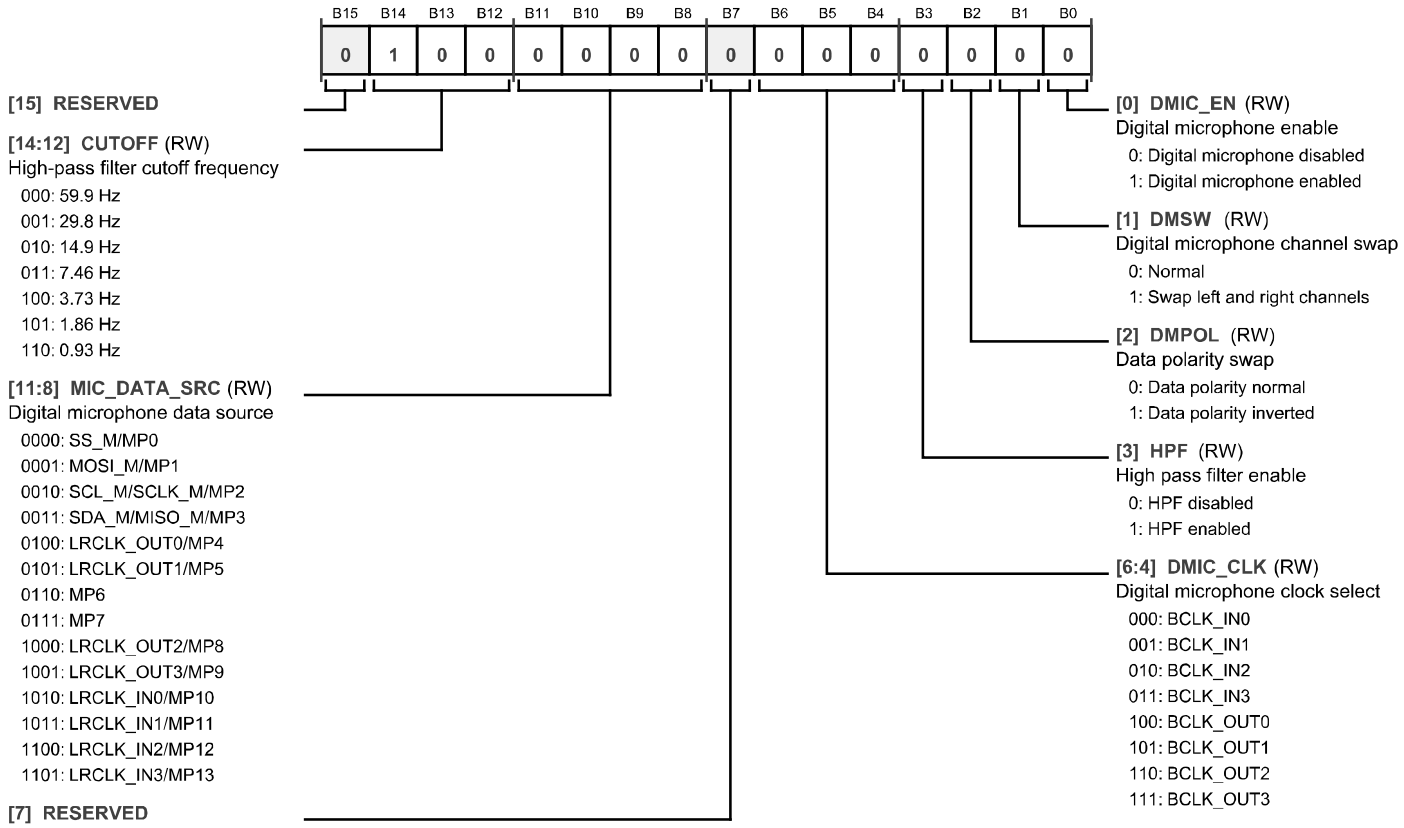


Table 125. Bit Descriptions for DMIC_CTRLx

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED			0x0	RW
[14:12]	CUTOFF		High-pass filter cutoff frequency. These bits configure the cutoff frequency of an optional high-pass filter designed to remove dc components from the microphone data signal(s). To use these bits, Bit 3 (HPF), must be enabled.	0x4	RW
		000	59.9 Hz		
		001	29.8 Hz		
		010	14.9 Hz		
		011	7.46 Hz		
		100	3.73 Hz		
		101	1.86 Hz		
		110	0.93 Hz		

S/PDIF Transmitter Validity Bits (Left) Register

Address: 0xF6E0 to 0xF6EB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_VB_LEFT_x

These 12 registers allow the 192 validity bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1466 and ADAU1462 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

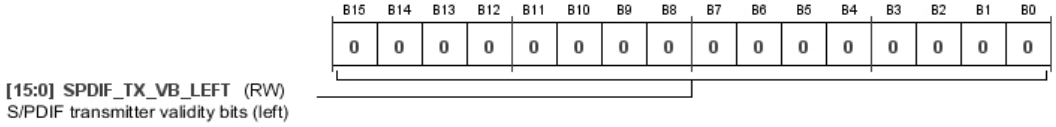


Table 155. Bit Descriptions for SPDIF_TX_VB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_VB_LEFT		S/PDIF transmitter validity bits (left).	0x0000	RW

S/PDIF Transmitter Validity Bits (Right) Register

Address: 0xF6F0 to 0xF6FB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_VB_RIGHT_x

These 12 registers allow the 192 validity bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1466 and ADAU1462 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

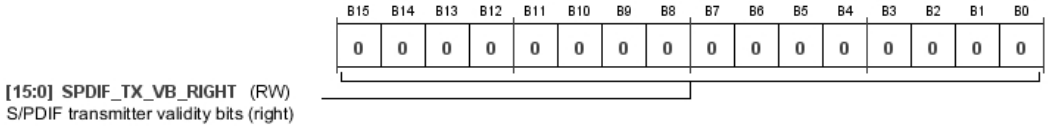


Table 156. Bit Descriptions for SPDIF_TX_VB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_VB_RIGHT		S/PDIF transmitter validity bits (right).	0x0000	RW

S/PDIF Transmitter Parity Bits (Left) Register

Address: 0xF700 to Address 0xF70B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_PB_LEFT_x

These 12 registers allow the 192 parity bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1466 and ADAU1462 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

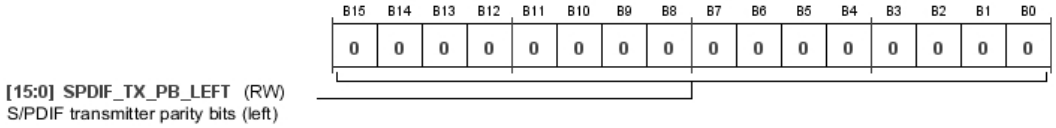


Table 157. Bit Descriptions for SPDIF_TX_PB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_PB_LEFT		S/PDIF transmitter parity bits (left).	0x0000	RW

MP6 Pin Drive Strength and Slew Rate Register

Address: 0xF7A1, Reset: 0x0018, Name: MP6_PIN

This register configures the drive strength, slew rate, and pull resistors for the MP6 pin.

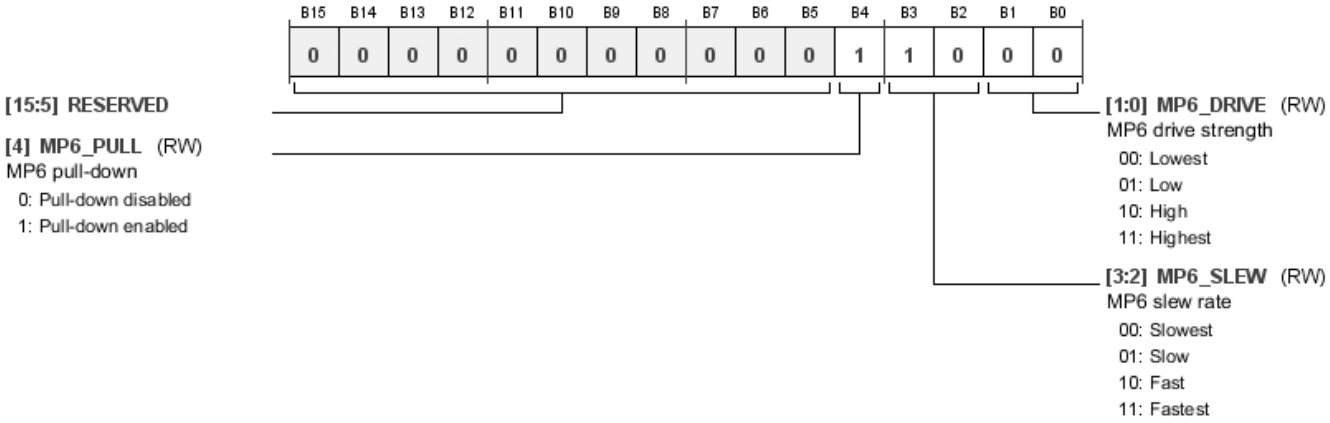


Table 174. Bit Descriptions for MP6_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	MP6_PULL		MP6 pull-down.	0x1	RW
		0	Pull-down disabled		
		1	Pull-down enabled		
[3:2]	MP6_SLEW		MP6 slew rate.	0x2	RW
		00	Slowest		
		01	Slow		
		10	Fast		
		11	Fastest		
[1:0]	MP6_DRIVE		MP6 drive strength.	0x0	RW
		00	Lowest		
		01	Low		
		10	High		
		11	Highest		

MP7 Pin Drive Strength and Slew Rate Register

Address: 0xF7A2, Reset: 0x0018, Name: MP7_PIN

This register configures the drive strength, slew rate, and pull resistors for the MP7 pin.

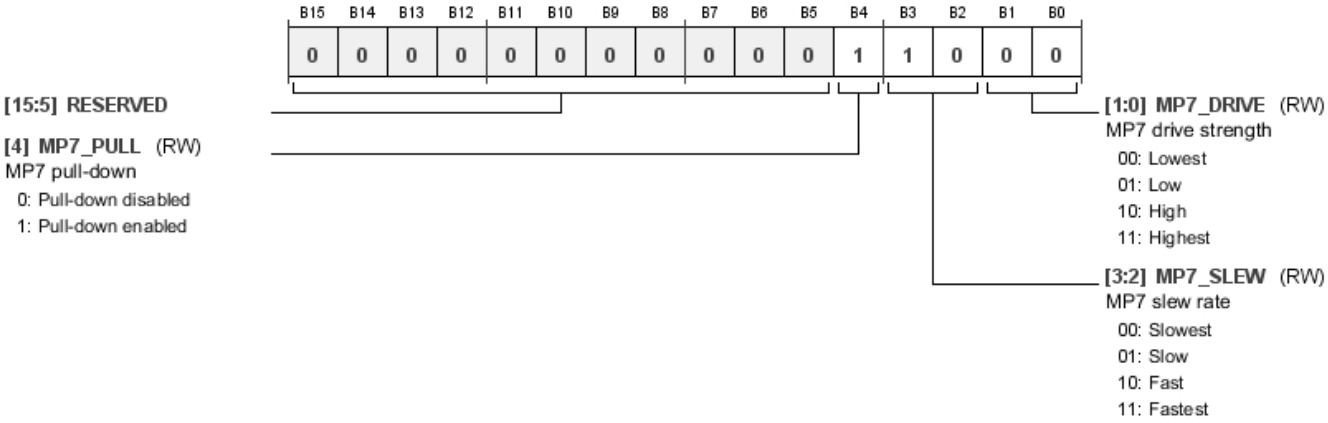


Table 175. Bit Descriptions for MP7_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	MP7_PULL		MP7 pull-down.	0x1	RW
		0	Pull-down disabled		
		1	Pull-down enabled		
[3:2]	MP7_SLEW		MP7 slew rate.	0x2	RW
		00	Slowest		
		01	Slow		
		10	Fast		
		11	Fastest		
[1:0]	MP7_DRIVE		MP7 drive strength.	0x0	RW
		00	Lowest		
		01	Low		
		10	High		
		11	Highest		

EXAMPLE PCB LAYOUT

Several external components, such as capacitors, resistors, and a transistor, are required for proper operation of the device. An example of the connection and layout of these components is shown in Figure 91. Thick black lines represent traces, gray rectangles represent components, and white circles with a thick black ring represent thermal via connections to power or ground planes. If a 1.2 V supply is available in the system, the transistor circuit (including the associated 1 kΩ resistor) can be removed, and 1.2 V can be connected directly to the DVDD power net, with the VDRIVE pin left floating.

The analog (AVDD), PLL (PVDD), and interface (IOVDD) supply pins each have local 100 nF bypass capacitors to provide high frequency return currents with a short path to ground.

The digital (DVDD) supply pins each have up to three local bypass capacitors, as follows:

- The 10 nF bypass capacitor, placed closest to the pin, acts as a return path for very high frequency currents resulting from the nominal 294.912 MHz operating frequency of the DSP core.
- The 100 nF bypass capacitor acts as a return path for high frequency currents from the DSP and other digital circuitry.
- The 1 µF bypass capacitor is required to provide a local current supply for sudden spikes in current that occur at the beginning of each audio frame when the DSP core switches from idle mode to operating mode.

Of these three bypass capacitors, the most important is the 100 nF bypass capacitor, which is required for proper power supply bypassing. The 10 nF and 1 µF capacitors can optionally be used to improve the EMI/EMC performance of the system.

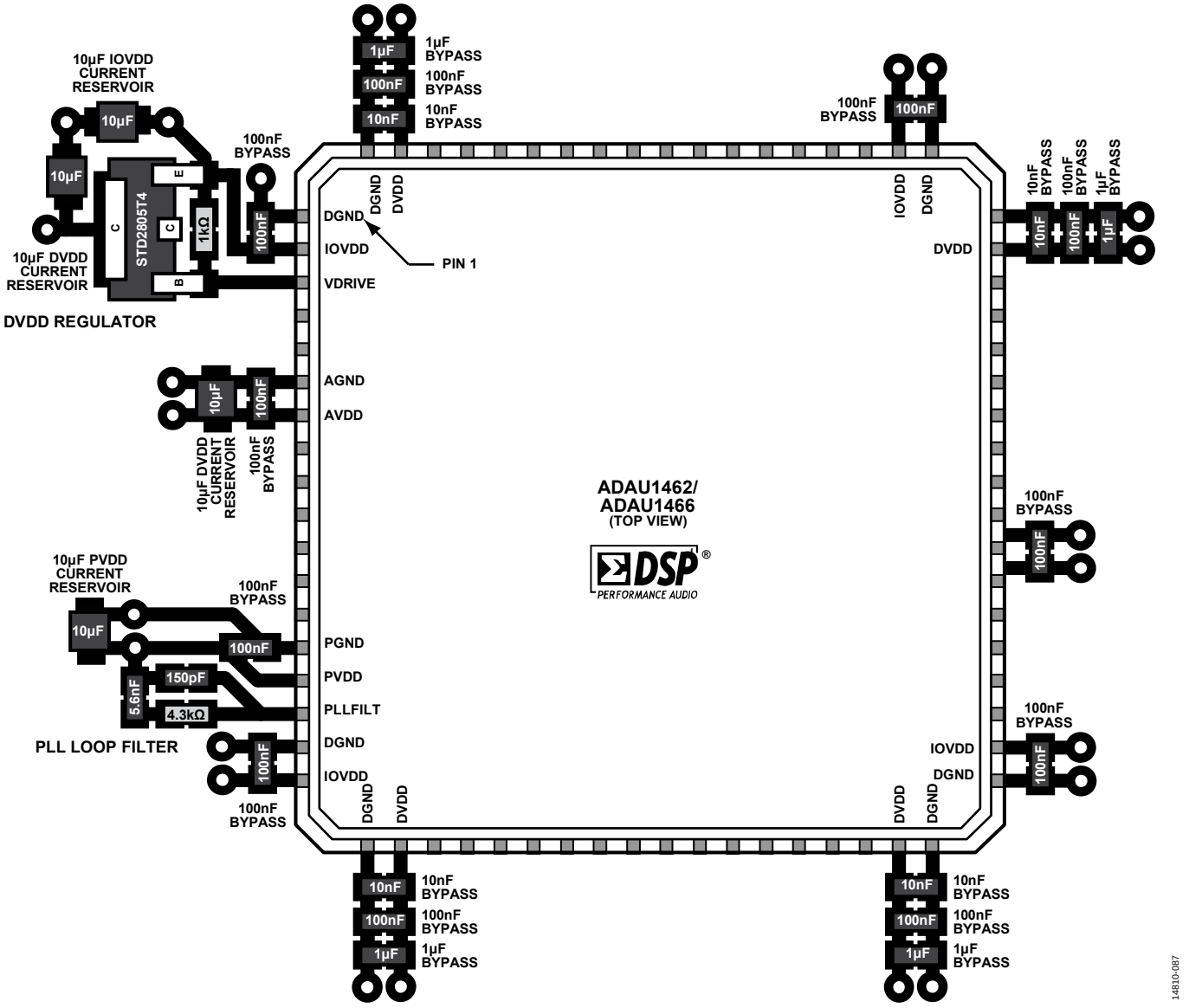


Figure 91. Supporting Component Placement and Layout