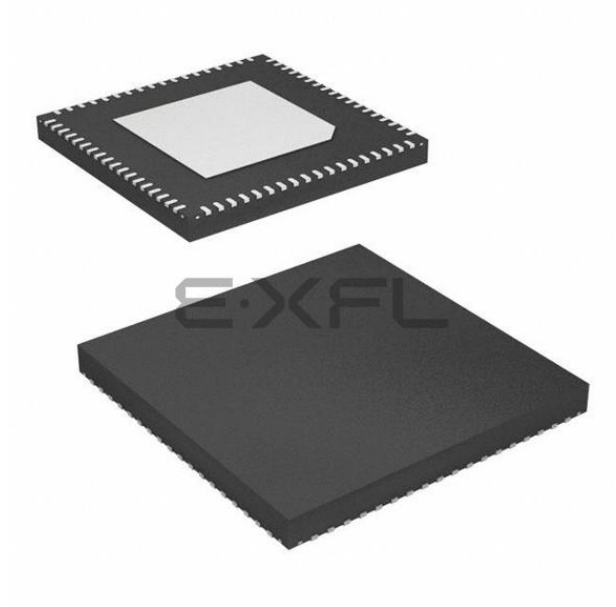

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Sigma |
| Interface | I²C, SPI |
| Clock Rate | 294.912MHz |
| Non-Volatile Memory | ROM (64kB) |
| On-Chip RAM | 192kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.20V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 72-VFQFN Exposed Pad, CSP |
| Supplier Device Package | 72-LFCSP-VQ (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adau1462wbcpz300rl |

## REVISION HISTORY

**3/2018—Rev. B to Rev. C**

Changes to Table 1 ....4
Changes to Table 2 ....5
Changes to Table 3 ....6
Added Endnote 1, Table 6 ....9
Deleted Endnote 1, Table 9 ....11
Changes to S/PDIF Transmitter and Receiver Section and Table 10 ....11
Deleted S/PDIF Receiver Section and Table 11; Renumbered Sequentially ....11
Added Table 11; Renumbered Sequentially ....12
Added I²C Interface—Master Section ....13
Changes to Table 20 ....29
Changes to Table 21 ....30
Changes to SigmaDSP Core Section ....80
Changes to Ordering Guide ....202

**10/2017—Rev. A to Rev. B**

Changes to Table 1 ....4
Changes to Table 2 ....5
Changes to Table 3 ....6
Changes to Table 6 ....9
Changes to Table 21 ....29
Changes to PLL Filter Section and Table 22 ....30
Changes to Clock Generators Section and Figure 18 ....31
Changes to Figure 19 ....32
Changes to Figure 26 ....37
Changes to Figure 27 ....38
Changes to SigmaDSP Core Section ....80
Changes to Table 58 ....89
Changes to Figure 82 ....90
Changes to Figure 83 ....91
Changes to Ordering Guide ....202

**9/2017—Rev. 0 to Rev. A**

Change to Supply Current Analog Current (AVDD) Parameter, Table 2 ....4
Change to Supply Current PLL Current (PVDD) Parameter and Supply Current Analog Current (AVDD) Parameter, Table 3 ....5
Added Endnote 2 to Ordering Guide ....201

**8/2017—Revision 0: Initial Version**

# SPECIFICATIONS

AVDD = 3.3 V ± 10%, DVDD = 1.2 V ± 5%, PVDD = 3.3 V ± 10%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, $T_A$ = 25°C, master clock input = 12.288 MHz, core clock ($f_{CORE}$) = 294.912 MHz, I/O pins set to low drive setting, unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| POWER | | | | | |
| Supply Voltage | | | | | |
| Analog Voltage (AVDD) | 2.97 | 3.3 | 3.63 | V | Supply for analog circuitry, including auxiliary ADC |
| Digital Voltage (DVDD) | 1.14 | 1.2 | 1.26 | V | Supply for digital circuitry, including the DSP core, ASRCs, and signal routing |
| PLL Voltage (PVDD) | 2.97 | 3.3 | 3.63 | V | Supply for PLL circuitry |
| I/O Supply Voltage (IOVDD) | 1.71 | 3.3 | 3.63 | V | Supply for input/output circuitry, including pads and level shifters |
| Supply Current | | | | | |
| Analog Current (AVDD) | 1.36 | 1.66 | 2 | mA | |
| Idle State | 1.00 | 1.10 | 40 | µA | Power applied, chip not programmed |
| Reset State | 1.00 | 1.10 | 40 | µA | Power applied, $\overline{\text{RESET}}$ held low |
| PLL Current (PVDD) | 8.3 | 10.1 | 12.9 | mA | 12.288 MHz MCLK with default PLL settings |
| Idle State | 18.3 | 18.7 | 40 | µA | Power applied, PLL not configured |
| Reset State | 18.3 | 18.7 | 40 | µA | Power applied, $\overline{\text{RESET}}$ held low |
| I/O Current (IOVDD) | | | | | Dependent on the number of active serial ports, clock pins, and characteristics of external loads |
| Operation State | | 53 | | mA | IOVDD = 3.3 V; all serial ports are clock masters |
| | | 22 | | mA | IOVDD = 1.8 V; all serial ports are clock masters |
| Power-Down State | | 4.1 | 4.2 | mA | IOVDD = 1.8 V − 5% to 3.3 V + 10% |
| Digital Current (DVDD) | | | | | |
| ADAU1466 Operation State | | | | | |
| Maximum Program | | 233 | 495 | mA | |
| Typical Program | | 220 | | mA | Test program includes 16-channel I/O, 10-band equalizer (EQ) per channel, all ASRCs active |
| Minimal Program | | 213 | | mA | Test program includes 2-channel I/O, 10-band EQ per channel |
| ADAU1462 Operation State | | | | | |
| $f_{CORE}$ = 294.912 MHz | | | | | |
| Maximum Program | | 233 | 495 | mA | |
| Typical Program | | 220 | | mA | Test program includes 16-channel I/O, 10-band EQ per channel, all ASRCs active |
| Minimal Program | | 213 | | mA | Test program includes 2-channel I/O, 10-band EQ per channel |
| $f_{CORE}$ = 147.456 MHz | | | | | |
| Maximum Program | | 170 | 455 | mA | |
| Typical Program | | 135 | | mA | Test program includes 16-channel I/O, 10-band EQ per channel |
| Minimal Program | | 110 | | mA | Test program includes 2-channel I/O, 10-band EQ per channel |
| Idle State | 18.3 | 18.7 | 19.9 | mA | Power applied, DSP not enabled |
| Reset State | 18.3 | 18.7 | 19.9 | mA | Power applied, $\overline{\text{RESET}}$ held low |
| ASYNCHRONOUS SAMPLE RATE CONVERTERS | | | | | |
| Dynamic Range | | 139 | | dB | A-weighted, 20 Hz to 20 kHz |
| I/O Sample Rate | 6 | | 192 | kHz | |
| I/O Sample Rate Ratio | 1:8 | | 7.75:1 | | |
| Total Harmonic Distortion + Noise (THD + N) | | | −120 | dB | |
| CRYSTAL OSCILLATOR | | | | | |
| Transconductance | 8.3 | 10.6 | 13.4 | mS | |
| REGULATOR | | | | | |
| DVDD Voltage | 1.14 | 1.2 | | V | Regulator maintains typical output voltage up to a maximum 800 mA load; IOVDD = 1.8 V − 5% to 3.3 V + 10% |

| Pin No. | Mnemonic | Internal Pull Resistor | Description |
|---|---|---|---|
| 51 | BCLK_OUT3 | Configurable | Bit Clock, Serial Output Port 3. This pin is bidirectional, with the direction depending on whether Serial Output Port 3 is a master or slave. Disconnect this pin when not in use. |
| 52 | SDATA_OUT3 | Configurable | Serial Data Output Port 3 (Channel 40 to Channel 47). Capable of 2-channel, 4-channel, 8-channel, and flexible TDM modes. Disconnect this pin when not in use. |
| 53 | DVDD | None | Digital Supply. Must be 1.2 V ± 5%. This pin can be supplied externally or by using the internal regulator and external pass transistor. Bypass Pin 53 with decoupling capacitors to Pin 54 (DGND). See the Power Supply Bypass Capacitors and Grounding sections. |
| 54 | DGND | None | Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections. |
| 55 | DGND | None | Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections. |
| 56 | IOVDD | None | Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this pin with decoupling capacitors to Pin 55 (DGND). See the Power Supply Bypass Capacitors and Grounding sections. |
| 57 | BCLK_IN0 | Configurable | Bit Clock, Serial Input Port 0. This pin is bidirectional, with the direction depending on whether Serial Input Port 0 is a master or slave. Disconnect this pin when not in use. |
| 58 | LRCLK_IN0/ MP10 | Configurable | Frame Clock, Serial Input Port 0 (LRCLK_IN0)/Multipurpose, General-Purpose Input/Output (MP10). This pin is bidirectional, with the direction depending on whether Serial Input Port 0 is a master or slave. Disconnect this pin when not in use. |
| 59 | SDATA_IN0 | Configurable | Serial Data Input Port 0 (Channel 0 to Channel 15). Capable of 2-channel, 4-channel, 8-channel, or 16-channel mode. Disconnect this pin when not in use. |
| 60 | BCLK_IN1 | Configurable | Bit Clock, Serial Input Port 1. This pin is bidirectional, with the direction depending on whether the Serial Input Port 1 is a master or slave. Disconnect this pin when not in use. |
| 61 | LRCLK_IN1/ MP11 | Configurable | Frame Clock, Serial Input Port 1 (LRCLK_IN1)/Multipurpose, General-Purpose Input/Output (MP11). This pin is bidirectional, with the direction depending on whether the Serial Input Port 1 is a master or slave. Disconnect this pin when not in use. |
| 62 | SDATA_IN1 | Configurable | Serial Data Input Port 1 (Channels 16 to Channel 31). Capable of 2-channel, 4-channel, 8-channel, or 16-channel mode. Disconnect this pin when not in use. |
| 63 | THD_M | None | Thermal Diode Negative (−) Input. Connect this pin to the D− pin of an external temperature sensor IC. Disconnect this pin when not in use. |
| 64 | THD_P | None | Thermal Diode Positive (+) Input. Connect this pin to the D+ pin of an external temperature sensor IC. Disconnect this pin when not in use. |
| 65 | BCLK_IN2 | Configurable | Bit Clock, Serial Input Port 2. This pin is bidirectional, with the direction depending on whether the Serial Input Port 2 is a master or slave. Disconnect this pin when not in use. |
| 66 | LRCLK_IN2/ MP12 | Configurable | Frame Clock, Input Serial Port 2 (LRCLK_IN2)/Multipurpose, General-Purpose Input/Output (MP12). This pin is bidirectional, with the direction depending on whether Serial Input Port 2 is a master or slave. Disconnect this pin when not in use. |
| 67 | SDATA_IN2 | Configurable | Serial Data Input Port 2 (Channel 32 to Channel 39). Capable of 2-channel, 4-channel, 8-channel, or flexible TDM mode. Disconnect this pin when not in use. |
| 68 | BCLK_IN3 | Configurable | Bit Clock, Input Serial Port 3. This pin is bidirectional, with the direction depending on whether Input Serial Port 3 is a master or slave. Disconnect this pin when not in use. |
| 69 | LRCLK_IN3/ MP13 | Configurable | Frame Clock, Serial Input Port 3 (LRCLK_IN3)/Multipurpose, General-Purpose Input/Output (MP13). This pin is bidirectional, with the direction depending on whether Serial Input Port 3 is a master or slave. Disconnect this pin when not in use. |
| 70 | SDATA_IN3 | Configurable | Serial Data Input Port 3 (Channel 40 to Channel 47). Capable of 2-channel, 4-channel, 8-channel, or flexible TDM mode. Disconnect this pin when not in use. |
| 71 | DVDD | None | Digital Supply. Must be 1.2 V ± 5%. This pin can be supplied externally or by using the internal regulator and external pass transistor. Bypass with decoupling capacitors to Pin 72 (DGND). |
| 72 | DGND | None | Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections. |
| EP | Exposed Pad | None | The exposed pad must be grounded by soldering it to a copper square of equivalent size on the PCB. Identical copper squares must exist on all layers of the board, connected by vias, and they must be connected to a dedicated copper ground layer within the PCB. See Exposed Pad PCB Design, Figure 87, and Figure 88. |

### System Initialization Sequence

Before the IC can process the audio in the DSP, the following initialization sequence must be completed.

1. If possible, apply the required voltage to all four power supply domains (IOVDD, AVDD, PVDD, and DVDD) simultaneously. If simultaneous application is not possible, supply IOVDD first to prevent damage or reduced operating lifetime. If using the on-board regulator, AVDD and PVDD can be supplied in any order, and DVDD is then generated automatically. If not using the on-board regulator, AVDD, PVDD, and DVDD can be supplied in any order following IOVDD.
2. Start providing a master clock signal to the XTALIN/MCLK pin, or, if using the crystal oscillator, let the crystal oscillator start generating a master clock signal. The master clock signal must be valid when the DVDD supply stabilizes.
3. If the SELFBOOT pin is pulled high, a self boot sequence initiates on the master control port. Wait until the self boot operation is complete.
4. If SPI slave control mode is desired, toggle the SS/ADDR0 pin three times. Ensure that each toggle lasts at least the duration of one cycle of the master clock being input to the XTALIN/MCLK pin. When the SS/ADDR0 line rises for the third time, the slave control port is then in SPI mode.
5. Execute the register and memory write sequence that is required to configure the device in the proper operating mode.

Table 19 contains an example series of register writes used to configure the system at startup. The contents of the data column may vary depending on the system configuration. The configuration that is listed in Table 19 represents the default initialization sequence for project files generated in SigmaStudio.

### Recommended Program/Parameter Loading Procedure

When writing large amounts of data to the program or parameter RAM in direct write mode (such as when downloading the initial contents of the RAMs from an external memory), use the hibernate register (Address 0xF400) to disable the processor core, thus preventing unpleasant noises from appearing at the audio output. When small amounts of data are transmitted during real-time operation of the DSP (such as when updating individual parameters), the software safeload mechanism can be used (see the Software Safeload section).

### *Master Clock, PLL, and Clock Generators Registers*

An overview of the registers related to the master clock, PLL, and clock generators is listed in Table 22. For a more detailed description, see the PLL Configuration Registers section and the Clock Generator Registers section.

**Table 22. Master Clock, PLL, and Clock Generator Registers**

| Address | Register | Description |
|---|---|---|
| 0xF000 | PLL_CTRL0 | PLL feedback divider |
| 0xF001 | PLL_CTRL1 | PLL prescale divider |
| 0xF002 | PLL_CLK_SRC | PLL clock source |
| 0xF003 | PLL_ENABLE | PLL enable |
| 0xF004 | PLL_LOCK | PLL lock |
| 0xF005 | MCLK_OUT | CLKOUT control |
| 0xF006 | PLL_WATCHDOG | Analog PLL watchdog control |
| 0xF020 | CLK_GEN1_M | Denominator (M) for Clock Generator 1 |
| 0xF021 | CLK_GEN1_N | Numerator (N) for Clock Generator 1 |
| 0xF022 | CLK_GEN2_M | Denominator (M) for Clock Generator 2 |
| 0xF023 | CLK_GEN2_N | Numerator (N) for Clock Generator 2 |
| 0xF024 | CLK_GEN3_M | Denominator (M) for Clock Generator 3 |
| 0xF025 | CLK_GEN3_N | Numerator (N) for Clock Generator 3 |
| 0xF026 | CLK_GEN3_SRC | Input source for Clock Generator 3 |
| 0xF027 | CLK_GEN3_LOCK | Lock bit for Clock Generator 3 input reference |

## POWER SUPPLIES, VOLTAGE REGULATOR, AND HARDWARE RESET

### *Power Supplies*

The ADAU1462/ADAU1466 are supplied by four power supplies: IOVDD, DVDD, AVDD, and PVDD.

- IOVDD (input/output supply) sets the reference voltage for all digital input and output pins. It can be any value ranging from 1.8 V − 5% to 3.3 V + 10%. To use the I²C/SPI control ports or any of the digital input or output pins, the IOVDD supply must be present.
- DVDD (digital supply) powers the DSP core and supporting digital logic circuitry. It must be 1.2 V ± 5%.
- AVDD (analog supply) powers the analog auxiliary ADC circuitry. It must be supplied even if the auxiliary ADCs are not in use.
- PVDD (PLL supply) powers the PLL and acts as a reference for the voltage controlled oscillator (VCO). It must be supplied even if the PLL is not in use.

**Table 23. Power Supply Details**

| Supply | Voltage | Externally Supplied? | Description |
|---|---|---|---|
| IOVDD (Input/ Output) | 1.8 V − 5% to 3.3 V + 10% | Yes | |
| DVDD (Digital) | 1.2 V ± 5% | Optional | Can be derived from IOVDD using an internal LDO regulator |
| AVDD (Analog) | 3.3 V ± 10% | Yes | |
| PVDD (PLL) | 3.3 V ± 10% | Yes | |

### *Voltage Regulator*

The ADAU1462/ADAU1466 include a linear regulator that can generate the 1.2 V supply required by the DSP core and other internal digital circuitry from an external supply. Source the linear regulator from the I/O supply (IOVDD), which can range from 1.8 V − 5% to 3.3 V + 10%. A simplified block diagram of the internal structure of the regulator is shown in Figure 22.

For proper operation, the linear regulator requires several external components. A PNP bipolar junction transistor, such as the ON Semiconductor NSS1C300ET4G, acts as an external pass device to bring the higher IOVDD voltage down to the lower DVDD voltage, thus externally dissipating the power of the IC package. Ensure that the current gain of the transistor (β) is 200 or greater and that the transistor is able to dissipate at least 1 W in the worst case. Place a 1 kΩ resistor between the transistor emitter and base to help stabilize the regulator for varying loads. This resistor placement also guarantees that current is always flowing into the VDRIVE pin, even for minimal regulator loads. Figure 21 shows the connection of the external components.

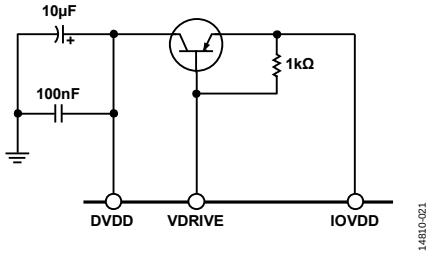


*Figure 21. External Components Required for Voltage Regulator Circuit*

If an external supply is provided to DVDD, ground the VDRIVE pin. The regulator continues to draw a small amount of current (approximately 100 µA) from the IOVDD supply. Do not use the regulator to provide a voltage supply to external ICs. There are no control registers associated with the regulator.

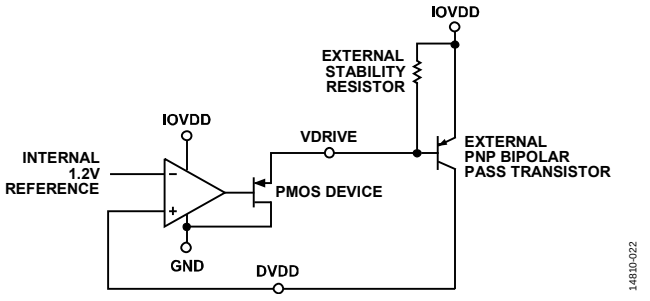


*Figure 22. Simplified Block Diagram of Regulator Internal Structure, Including External Components*

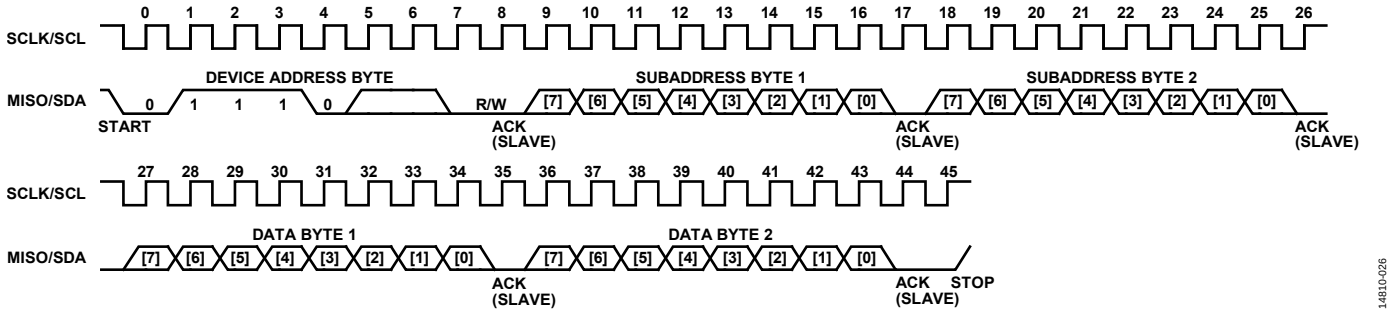


Figure 28. I²C Slave Single Word Write Operation (Two Bytes)

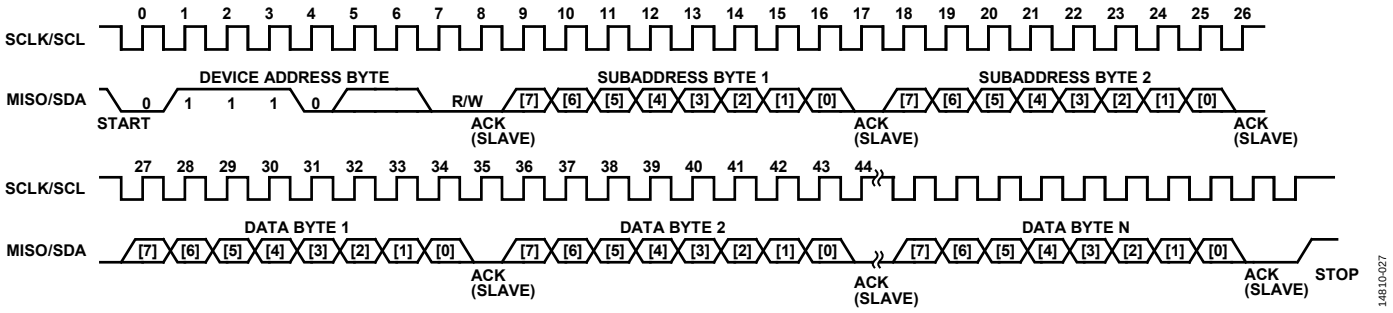


Figure 29. I²C Slave Burst Mode Write Operation (N Bytes)

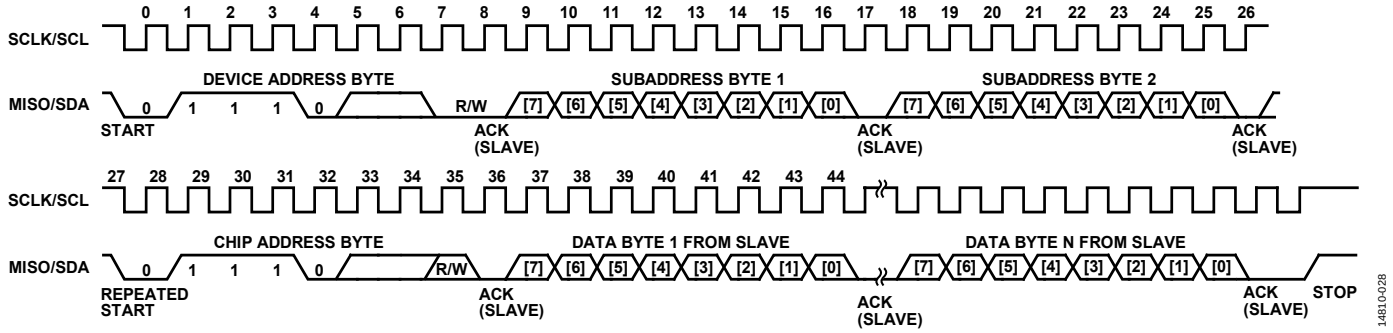


Figure 30. I²C Slave Burst Mode Read Operation (N Bytes)

### I²C Read and Write Operations

Figure 31 shows the format of a single word write operation. Every ninth clock pulse, the ADAU1462/ADAU1466 issue an acknowledge by pulling SDA low.

Figure 32 shows the simplified format of a burst mode write sequence. This figure shows an example of a write to sequential single byte registers. The ADAU1462/ADAU1466 increment the subaddress register after every byte because the requested subaddress corresponds to a register or memory area with a 1-byte word length.

Figure 33 shows the format of a single word read operation. The first R/$\overline{W}$ bit is 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the ADAU1462/ADAU1466 acknowledge the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ bit set to 1 (read). The start command causes the SDA pin of the device to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the device.

Figure 34 shows the format of a burst mode read sequence. This figure shows an example of a read from sequential single byte registers. The ADAU1462/ADAU1466 increment the subaddress register after every byte because the requested subaddress corresponds to a register or memory area with a 1-byte word length. The ADAU1462/ADAU1466 always decode the subaddress and set the auto-increment circuit such that the address increments after the appropriate number of bytes.

Figure 31 to Figure 34 use the following abbreviations:

- S means start bit.
- P means stop bit.
- AM means acknowledge by master.
- AS means acknowledge by slave.

### *Serial Audio Inputs to DSP Core*

The 48 serial input channels are mapped to four audio input cells in SigmaStudio. Each input cell corresponds to one of the serial input pins (see Table 32).

Depending on whether the serial port is configured in 2-channel, 4-channel, 8-channel, or 16-channel mode, the available channels in SigmaStudio change. The channel count for each serial port is configured in the SERIAL_BYTE_x_0 registers, Bits[2:0] (TDM_MODE), at Address 0xF200 to Address 0xF21C (in increments of 0x4).

Figure 44 shows how the input pins map to the input cells in SigmaStudio, including their graphical appearance in the software.

**Table 32. Serial Input Pin Mapping to SigmaStudio Input Cells**

| Serial Input Pin | Channels in SigmaStudio |
|---|---|
| SDATA_IN0 | 0 to 15 |
| SDATA_IN1 | 16 to 31 |
| SDATA_IN2 | 32 to 39 |
| SDATA_IN3 | 40 to 47 |

**Table 33. Detailed Serial Input Mapping to SigmaStudio Input Channels**

| Serial Input Pin | Position in I²S Stream (2-Channel) | Position in TDM4 Stream | Position in TDM8 Stream | Position in TDM16 Stream | Input Channel in SigmaStudio |
|---|---|---|---|---|---|
| SDATA_IN0 | Left | 0 | 0 | 0 | 0 |
| SDATA_IN0 | Right | 1 | 1 | 1 | 1 |
| SDATA_IN0 | Not applicable | 2 | 2 | 2 | 2 |
| SDATA_IN0 | Not applicable | 3 | 3 | 3 | 3 |
| SDATA_IN0 | Not applicable | Not applicable | 4 | 4 | 4 |
| SDATA_IN0 | Not applicable | Not applicable | 5 | 5 | 5 |
| SDATA_IN0 | Not applicable | Not applicable | 6 | 6 | 6 |
| SDATA_IN0 | Not applicable | Not applicable | 7 | 7 | 7 |
| SDATA_IN0 | Not applicable | Not applicable | Not applicable | 8 | 8 |
| SDATA_IN0 | Not applicable | Not applicable | Not applicable | 9 | 9 |
| SDATA_IN0 | Not applicable | Not applicable | Not applicable | 10 | 10 |
| SDATA_IN0 | Not applicable | Not applicable | Not applicable | 11 | 11 |
| SDATA_IN0 | Not applicable | Not applicable | Not applicable | 12 | 12 |
| SDATA_IN0 | Not applicable | Not applicable | Not applicable | 13 | 13 |
| SDATA_IN0 | Not applicable | Not applicable | Not applicable | 14 | 14 |
| SDATA_IN0 | Not applicable | Not applicable | Not applicable | 15 | 15 |
| SDATA_IN1 | Left | 0 | 0 | 0 | 16 |
| SDATA_IN1 | Right | 1 | 1 | 1 | 17 |
| SDATA_IN1 | Not applicable | 2 | 2 | 2 | 18 |
| SDATA_IN1 | Not applicable | 3 | 3 | 3 | 19 |
| SDATA_IN1 | Not applicable | Not applicable | 4 | 4 | 20 |
| SDATA_IN1 | Not applicable | Not applicable | 5 | 5 | 21 |
| SDATA_IN1 | Not applicable | Not applicable | 6 | 6 | 22 |
| SDATA_IN1 | Not applicable | Not applicable | 7 | 7 | 23 |
| SDATA_IN1 | Not applicable | Not applicable | Not applicable | 8 | 24 |
| SDATA_IN1 | Not applicable | Not applicable | Not applicable | 9 | 25 |
| SDATA_IN1 | Not applicable | Not applicable | Not applicable | 10 | 26 |
| SDATA_IN1 | Not applicable | Not applicable | Not applicable | 11 | 27 |
| SDATA_IN1 | Not applicable | Not applicable | Not applicable | 12 | 28 |
| SDATA_IN1 | Not applicable | Not applicable | Not applicable | 13 | 29 |
| SDATA_IN1 | Not applicable | Not applicable | Not applicable | 14 | 30 |
| SDATA_IN1 | Not applicable | Not applicable | Not applicable | 15 | 31 |
| SDATA_IN2 | Left | 0 | 0 | 0 | 32 |
| SDATA_IN2 | Right | 1 | 1 | 1 | 33 |
| SDATA_IN2 | Not applicable | 2 | 2 | 2 | 34 |
| SDATA_IN2 | Not applicable | 3 | 3 | 3 | 35 |
| SDATA_IN2 | Not applicable | Not applicable | 4 | 4 | 36 |
| SDATA_IN2 | Not applicable | Not applicable | 5 | 5 | 37 |
| SDATA_IN2 | Not applicable | Not applicable | 6 | 6 | 38 |
| SDATA_IN2 | Not applicable | Not applicable | 7 | 7 | 39 |

## SERIAL DATA INPUT/OUTPUT

There are four serial data input pins (SDATA_IN3 to SDATA_IN0) and four serial data output pins (SDATA_OUT3 to SDATA_OUT0). Each pin is capable of 2-channel, 4-channel, or 8-channel mode. In addition, SDATA_IN0, SDATA_IN1, SDATA_OUT0, and SDATA_OUT1 are capable of 16-channel mode.

The serial ports have a very flexible configuration scheme that allows completely independent and orthogonal configuration of clock pin assignment, clock waveform type, clock polarity, channel count, position of the data bits within the stream, audio word length, slave or master operation, and sample rate. A detailed description of all possible serial port settings is included in the Serial Port Configuration Registers section.

The physical serial data input and output pins are connected to functional blocks called serial ports, which deal with handling the audio data and clocks as they pass in and out of the device. Table 39 describes this relationship.

**Table 39. Relationship Between Hardware Serial Data Pins and Serial Input/Output Ports**

| Serial Data Pin | Serial Port |
|---|---|
| SDATA_IN0 | Serial Input Port 0 |
| SDATA_IN1 | Serial Input Port 1 |
| SDATA_IN2 | Serial Input Port 2 |
| SDATA_IN3 | Serial Input Port 3 |
| SDATA_OUT0 | Serial Output Port 0 |
| SDATA_OUT1 | Serial Output Port 1 |
| SDATA_OUT2 | Serial Output Port 2 |
| SDATA_OUT3 | Serial Output Port 3 |

There are 48 channels of serial audio data inputs and 48 channels of serial audio data outputs. The 48 audio input channels and 48 audio output channels are distributed among the four serial data input pins and the four serial data output pins. This distribution is described in Table 40.

The maximum sample rate for the serial audio data on the serial ports is 192 kHz. The minimum sample rate is 6 kHz.

SDATA_IN2, SDATA_IN3, SDATA_OUT2, and SDATA_OUT3 are capable of operating in a special mode called flexible TDM mode, which allows custom byte addressable configuration, where the data for each channel is located in the serial data stream. Flexible TDM mode is not a standard audio interface. Use it only in cases where a customized serial data format is desired. See the Flexible TDM Interface section for more information.

### *Serial Audio Data Format*

The serial data input and output ports are designed to work with audio data that is encoded in a linear PCM format, based on the common I²S standard. Audio data-words can be 16, 24, or 32 bits in length. The serial ports can handle TDM formats with channel counts ranging from two channels to 16 channels on a single data line.

Almost every aspect of the serial audio data format can be configured using the SERIAL_BYTE_x_0 and SERIAL_BYTE_x_1 registers, and every setting can be configured independently. As a result, there are more than 70,000 valid configurations for each serial audio port.

### *Serial Audio Data Timing Diagrams*

Because it is impractical to show timing diagrams for each possible combination, timing diagrams for the more common configurations are shown in Figure 61 to Figure 66. Explanatory text accompanies each figure.

**Table 40. Relationship Between Data Pin, Audio Channels, Clock Pins, and TDM Options**

| Serial Data Pin | Channel Numbering | Corresponding Clock Pins in Master Mode | Maximum TDM Channels | Flexible TDM Mode |
|---|---|---|---|---|
| SDATA_IN0 | Channel 0 to Channel 15 | BCLK_IN0, LRCLK_IN0 | 16 channels | No |
| SDATA_IN1 | Channel 16 to Channel 31 | BCLK_IN1, LRCLK_IN1 | 16 channels | No |
| SDATA_IN2 | Channel 32 to Channel 39 | BCLK_IN2, LRCLK_IN2 | 8 channels | Yes |
| SDATA_IN3 | Channel 40 to Channel 47 | BCLK_IN3, LRCLK_IN3 | 8 channels | Yes |
| SDATA_OUT0 | Channel 0 to Channel 15 | BCLK_OUT0, LRCLK_OUT0 | 16 channels | No |
| SDATA_OUT1 | Channel 16 to Channel 31 | BCLK_OUT1, LRCLK_OUT1 | 16 channels | No |
| SDATA_OUT2 | Channel 32 to Channel 39 | BCLK_OUT2, LRCLK_OUT2 | 8 channels | Yes |
| SDATA_OUT3 | Channel 40 to Channel 47 | BCLK_OUT3, LRCLK_OUT3 | 8 channels | Yes |

### *Serial Clock Domains*

There are four input clock domains and four output clock domains. A clock domain consists of a pair of LRCLK_OUTx and LRCLK_INx (frame clock) and BCLK_OUTx and BCLK_INx (bit clock) pins, which are used to synchronize the transmission of audio data to and from the device. There are eight total clock domains. Four of them are input domains and four of them are output domains. In master mode (refer to the SERIAL_BYTE_x_0 registers, Register 0xF200 to Register 0xF21C, Bits[15:13] (LRCLK_SRC) = 0b100 and Bits[12:10] (BCLK_SRC) = 0b100), each clock domain corresponds to exactly one serial data pin, one frame clock pin, and one bit clock pin.

Any serial data input can be clocked by any input clock domains when it is configured in slave mode (refer to the SERIAL_BYTE_x_0 registers, Bits[15:13] (LRCLK_SRC), which can be set to 0b000, 0b001, 0b010, or 0b011; and Bits[12:10] (BCLK_SRC), which can be set to 0b000, 0b001, 0b010, or 0b011). Any serial data output can be clocked by any output clock domain when it is configured in slave mode (see the SERIAL_BYTE_x_0 registers, Bits[15:13] (LRCLK_SRC), which can be set to 0b000, 0b001, 0b010, or 0b011; and Bits[12:10] (BCLK_SRC), which can be set to 0b000, 0b001, 0b010, or 0b011).

**Table 41. Relationship Between Serial Data Pins and Clock Pins in Master or Slave Mode**

| Serial Data Pin | Corresponding Clock Pins in Master Mode | Corresponding Clock Pins in Slave Mode |
|---|---|---|
| SDATA_IN0 | BCLK_IN0, LRCLK_IN0 (LRCLK_IN0/MP10) | BCLK_IN0, LRCLK_IN0 or<br>BCLK_IN1, LRCLK_IN1 or<br>BCLK_IN2, LRCLK_IN2 or<br>BCLK_IN3, LRCLK_IN3 |
| SDATA_IN1 | BCLK_IN1, LRCLK_IN1 (LRCLK_IN1/MP11) | BCLK_IN0, LRCLK_IN0 or<br>BCLK_IN1, LRCLK_IN1 or<br>BCLK_IN2, LRCLK_IN2 or<br>BCLK_IN3, LRCLK_IN3 |
| SDATA_IN2 | BCLK_IN2, LRCLK_IN2 (LRCLK_IN2/MP12) | BCLK_IN0, LRCLK_IN0 or<br>BCLK_IN1, LRCLK_IN1 or<br>BCLK_IN2, LRCLK_IN2 or<br>BCLK_IN3, LRCLK_IN3 |
| SDATA_IN3 | BCLK_IN3, LRCLK_IN3 (LRCLK_IN3/MP13) | BCLK_IN0, LRCLK_IN0 or<br>BCLK_IN1, LRCLK_IN1 or<br>BCLK_IN2, LRCLK_IN2 or<br>BCLK_IN3, LRCLK_IN3 |
| SDATA_OUT0 | BCLK_OUT0, LRCLK_OUT0 (LRCLK_OUT0/MP4) | BCLK_OUT0, LRCLK_OUT0 or<br>BCLK_OUT1, LRCLK_OUT1 or<br>BCLK_OUT2, LRCLK_OUT2 or<br>BCLK_OUT3, LRCLK_OUT3 |
| SDATA_OUT1 | BCLK_OUT1, LRCLK_OUT1 (LRCLK_OUT1/MP5) | BCLK_OUT0, LRCLK_OUT0 or<br>BCLK_OUT1, LRCLK_OUT1 or<br>BCLK_OUT2, LRCLK_OUT2 or<br>BCLK_OUT3, LRCLK_OUT3 |
| SDATA_OUT2 | BCLK_OUT2, LRCLK_OUT2 (LRCLK_OUT2/MP8) | BCLK_OUT0, LRCLK_OUT0 or<br>BCLK_OUT1, LRCLK_OUT1 or<br>BCLK_OUT2, LRCLK_OUT2 or<br>BCLK_OUT3, LRCLK_OUT3 |
| SDATA_OUT3 | BCLK_OUT3, LRCLK_OUT3 (LRCLK_OUT3/MP9) | BCLK_OUT0, LRCLK_OUT0 or<br>BCLK_OUT1, LRCLK_OUT1 or<br>BCLK_OUT2, LRCLK_OUT2 or<br>BCLK_OUT3, LRCLK_OUT3 |

### *Flexible TDM Registers*

An overview of the registers related to the flexible TDM interface is shown in Table 45. For a more detailed description, see the Flexible TDM Interface Registers section.

**Table 45. Flexible TDM Registers**

| Address | Register | Description |
|---|---|---|
| 0xF300 | FTDM_IN0 | FTDM mapping for the serial inputs (Channel 32, Bits[31:24]) |
| 0xF301 | FTDM_IN1 | FTDM mapping for the serial inputs (Channel 32, Bits[23:16]) |
| 0xF302 | FTDM_IN2 | FTDM mapping for the serial inputs (Channel 32, Bits[15:8]) |
| 0xF303 | FTDM_IN3 | FTDM mapping for the serial inputs (Channel 32, Bits[7:0]) |
| 0xF304 | FTDM_IN4 | FTDM mapping for the serial inputs (Channel 33, Bits[31:24]) |
| 0xF305 | FTDM_IN5 | FTDM mapping for the serial inputs (Channel 33, Bits[23:16]) |
| 0xF306 | FTDM_IN6 | FTDM mapping for the serial inputs (Channel 33, Bits[15:8]) |
| 0xF307 | FTDM_IN7 | FTDM mapping for the serial inputs Channel 33, Bits[7:0]) |
| 0xF308 | FTDM_IN8 | FTDM mapping for the serial inputs (Channel 34, Bits[31:24]) |
| 0xF309 | FTDM_IN9 | FTDM mapping for the serial inputs (Channel 34, Bits[23:16]) |
| 0xF30A | FTDM_IN10 | FTDM mapping for the serial inputs (Channel 34, Bits[15:8]) |
| 0xF30B | FTDM_IN11 | FTDM mapping for the serial inputs (Channel 34, Bits[7:0]) |
| 0xF30C | FTDM_IN12 | FTDM mapping for the serial inputs (Channel 35, Bits[31:24]) |
| 0xF30D | FTDM_IN13 | FTDM mapping for the serial inputs (Channel 35, Bits[23:16]) |
| 0xF30E | FTDM_IN14 | FTDM mapping for the serial inputs (Channel 35, Bits[15:8]) |
| 0xF30F | FTDM_IN15 | FTDM mapping for the serial inputs (Channel 35, Bits[7:0]) |
| 0xF310 | FTDM_IN16 | FTDM mapping for the serial inputs (Channel 36, Bits[31:24]) |
| 0xF311 | FTDM_IN17 | FTDM mapping for the serial inputs (Channel 36, Bits[23:16]) |
| 0xF312 | FTDM_IN18 | FTDM mapping for the serial inputs (Channel 36, Bits[15:8]) |
| 0xF313 | FTDM_IN19 | FTDM mapping for the serial inputs (Channel 36, Bits[7:0]) |
| 0xF314 | FTDM_IN20 | FTDM mapping for the serial inputs (Channel 37, Bits[31:24]) |
| 0xF315 | FTDM_IN21 | FTDM mapping for the serial inputs (Channel 37, Bits[23:16]) |
| 0xF316 | FTDM_IN22 | FTDM mapping for the serial inputs (Channel 37, Bits[15:8]) |
| 0xF317 | FTDM_IN23 | FTDM mapping for the serial inputs (Channel 37, Bits[7:0]) |
| 0xF318 | FTDM_IN24 | FTDM mapping for the serial inputs (Channel 38, Bits[31:24]) |
| 0xF319 | FTDM_IN25 | FTDM mapping for the serial inputs (Channel 38, Bits[23:16]) |
| 0xF31A | FTDM_IN26 | FTDM mapping for the serial inputs (Channel 38, Bits[15:8]) |
| 0xF31B | FTDM_IN27 | FTDM mapping for the serial inputs (Channel 38, Bits[7:0]) |
| 0xF31C | FTDM_IN28 | FTDM mapping for the serial inputs (Channel 39, Bits[31:24]) |
| 0xF31D | FTDM_IN29 | FTDM mapping for the serial inputs (Channel 39, Bits[23:16]) |
| 0xF31E | FTDM_IN30 | FTDM mapping for the serial inputs (Channel 39, Bits[15:8]) |
| 0xF31F | FTDM_IN31 | FTDM mapping for the serial inputs (Channel 39, Bits[7:0]) |
| 0xF320 | FTDM_IN32 | FTDM mapping for the serial inputs (Channel 40, Bits[31:24]) |
| 0xF321 | FTDM_IN33 | FTDM mapping for the serial inputs (Channel 40, Bits[23:16]) |
| 0xF322 | FTDM_IN34 | FTDM mapping for the serial inputs (Channel 40, Bits[15:8]) |
| 0xF323 | FTDM_IN35 | FTDM mapping for the serial inputs (Channel 40, Bits[7:0]) |
| 0xF324 | FTDM_IN36 | FTDM mapping for the serial inputs (Channel 41, Bits[31:24]) |
| 0xF325 | FTDM_IN37 | FTDM mapping for the serial inputs (Channel 41, Bits[23:16]) |
| 0xF326 | FTDM_IN38 | FTDM mapping for the serial inputs (Channel 41, Bits[15:8]) |
| 0xF327 | FTDM_IN39 | FTDM mapping for the serial inputs (Channel 41, Bits[7:0]) |
| 0xF328 | FTDM_IN40 | FTDM mapping for the serial inputs (Channel 42, Bits[31:24]) |
| 0xF329 | FTDM_IN41 | FTDM mapping for the serial inputs (Channel 42, Bits[23:16]) |
| 0xF32A | FTDM_IN42 | FTDM mapping for the serial inputs (Channel 42, Bits[15:8]) |
| 0xF32B | FTDM_IN43 | FTDM mapping for the serial inputs (Channel 42, Bits[7:0]) |
| 0xF32C | FTDM_IN44 | FTDM mapping for the serial inputs (Channel 43, Bits[31:24]) |
| 0xF32D | FTDM_IN45 | FTDM mapping for the serial inputs (Channel 43, Bits[23:16]) |
| 0xF32E | FTDM_IN46 | FTDM mapping for the serial inputs (Channel 43, Bits[15:8]) |
| 0xF32F | FTDM_IN47 | FTDM mapping for the serial inputs (Channel 43, Bits[7:0]) |

| Address | Register | Description |
|---|---|---|
| 0xF330 | FTDM_IN48 | FTDM mapping for the serial inputs (Channel 44, Bits[31:24]) |
| 0xF331 | FTDM_IN49 | FTDM mapping for the serial inputs (Channel 44, Bits[23:16]) |
| 0xF332 | FTDM_IN50 | FTDM mapping for the serial inputs (Channel 44, Bits[15:8]) |
| 0xF333 | FTDM_IN51 | FTDM mapping for the serial inputs (Channel 44, Bits[7:0]) |
| 0xF334 | FTDM_IN52 | FTDM mapping for the serial inputs (Channel 45, Bits[31:24]) |
| 0xF335 | FTDM_IN53 | FTDM mapping for the serial inputs (Channel 45, Bits[23:16]) |
| 0xF336 | FTDM_IN54 | FTDM mapping for the serial inputs (Channel 45, Bits[15:8]) |
| 0xF337 | FTDM_IN55 | FTDM mapping for the serial inputs (Channel 45, Bits[7:0]) |
| 0xF338 | FTDM_IN56 | FTDM mapping for the serial inputs (Channel 46, Bits[31:24]) |
| 0xF339 | FTDM_IN57 | FTDM mapping for the serial inputs (Channel 46, Bits[23:16]) |
| 0xF33A | FTDM_IN58 | FTDM mapping for the serial inputs (Channel 46, Bits[15:8]) |
| 0xF33B | FTDM_IN59 | FTDM mapping for the serial inputs (Channel 46, Bits[7:0]) |
| 0xF33C | FTDM_IN60 | FTDM mapping for the serial inputs (Channel 47, Bits[31:24]) |
| 0xF33D | FTDM_IN61 | FTDM mapping for the serial inputs (Channel 47, Bits[23:16]) |
| 0xF33E | FTDM_IN62 | FTDM mapping for the serial inputs (Channel 47, Bits[15:8]) |
| 0xF33F | FTDM_IN63 | FTDM mapping for the serial inputs (Channel 47, Bits[7:0]) |
| 0xF380 | FTDM_OUT0 | FTDM mapping for the serial outputs (Port 2, Channel 0, Bits[31:24]) |
| 0xF381 | FTDM_OUT1 | FTDM mapping for the serial outputs (Port 2, Channel 0, Bits[23:16]) |
| 0xF382 | FTDM_OUT2 | FTDM mapping for the serial outputs (Port 2, Channel 0, Bits[15:8]) |
| 0xF383 | FTDM_OUT3 | FTDM mapping for the serial outputs (Port 2, Channel 0, Bits[7:0]) |
| 0xF384 | FTDM_OUT4 | FTDM mapping for the serial outputs (Port 2, Channel 1, Bits[31:24]) |
| 0xF385 | FTDM_OUT5 | FTDM mapping for the serial outputs (Port 2, Channel 1, Bits[23:16]) |
| 0xF386 | FTDM_OUT6 | FTDM mapping for the serial outputs (Port 2, Channel 1, Bits[15:8]) |
| 0xF387 | FTDM_OUT7 | FTDM mapping for the serial outputs (Port 2, Channel 1, Bits[7:0]) |
| 0xF388 | FTDM_OUT8 | FTDM mapping for the serial outputs (Port 2, Channel 2, Bits[31:24]) |
| 0xF389 | FTDM_OUT9 | FTDM mapping for the serial outputs (Port 2, Channel 2, Bits[23:16]) |
| 0xF38A | FTDM_OUT10 | FTDM mapping for the serial outputs (Port 2, Channel 2, Bits[15:8]) |
| 0xF38B | FTDM_OUT11 | FTDM mapping for the serial outputs (Port 2, Channel 2, Bits[7:0]) |
| 0xF38C | FTDM_OUT12 | FTDM mapping for the serial outputs (Port 2, Channel 3, Bits[31:24]) |
| 0xF38D | FTDM_OUT13 | FTDM mapping for the serial outputs (Port 2, Channel 3, Bits[23:16]) |
| 0xF38E | FTDM_OUT14 | FTDM mapping for the serial outputs (Port 2, Channel 3, Bits[15:8]) |
| 0xF38F | FTDM_OUT15 | FTDM mapping for the serial outputs (Port 2, Channel 3, Bits[7:0]) |
| 0xF390 | FTDM_OUT16 | FTDM mapping for the serial outputs (Port 2, Channel 4, Bits[31:24]) |
| 0xF391 | FTDM_OUT17 | FTDM mapping for the serial outputs (Port 2, Channel 4, Bits[23:16]) |
| 0xF392 | FTDM_OUT18 | FTDM mapping for the serial outputs (Port 2, Channel 4, Bits[15:8]) |
| 0xF393 | FTDM_OUT19 | FTDM mapping for the serial outputs (Port 2, Channel 4, Bits[7:0]) |
| 0xF394 | FTDM_OUT20 | FTDM mapping for the serial outputs (Port 2, Channel 5, Bits[31:24]) |
| 0xF395 | FTDM_OUT21 | FTDM mapping for the serial outputs (Port 2, Channel 5, Bits[23:16]) |
| 0xF396 | FTDM_OUT22 | FTDM mapping for the serial outputs (Port 2, Channel 5, Bits[15:8]) |
| 0xF397 | FTDM_OUT23 | FTDM mapping for the serial outputs (Port 2, Channel 5, Bits[7:0]) |
| 0xF398 | FTDM_OUT24 | FTDM mapping for the serial outputs (Port 2, Channel 6, Bits[31:24]) |
| 0xF399 | FTDM_OUT25 | FTDM mapping for the serial outputs (Port 2, Channel 6, Bits[23:16]) |
| 0xF39A | FTDM_OUT26 | FTDM mapping for the serial outputs (Port 2, Channel 6, Bits[15:8]) |
| 0xF39B | FTDM_OUT27 | FTDM mapping for the serial outputs (Port 2, Channel 6, Bits[7:0]) |
| 0xF39C | FTDM_OUT28 | FTDM mapping for the serial outputs (Port 2, Channel 7, Bits[31:24]) |
| 0xF39D | FTDM_OUT29 | FTDM mapping for the serial outputs (Port 2, Channel 7, Bits[23:16]) |
| 0xF39E | FTDM_OUT30 | FTDM mapping for the serial outputs (Port 2, Channel 7, Bits[15:8]) |
| 0xF39F | FTDM_OUT31 | FTDM mapping for the serial outputs (Port 2, Channel 7, Bits[7:0]) |
| 0xF3A0 | FTDM_OUT32 | FTDM mapping for the serial outputs (Port 3, Channel 0, Bits[31:24]) |
| 0xF3A1 | FTDM_OUT33 | FTDM mapping for the serial outputs (Port 3, Channel 0, Bits[23:16]) |
| 0xF3A2 | FTDM_OUT34 | FTDM mapping for the serial outputs (Port 3, Channel 0, Bits[15:8]) |
| 0xF3A3 | FTDM_OUT35 | FTDM mapping for the serial outputs (Port 3, Channel 0, Bits[7:0]) |
| 0xF3A4 | FTDM_OUT36 | FTDM mapping for the serial outputs (Port 3, Channel 1, Bits[31:24]) |

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0xF380 ... 0xF3BF | FTDM_OUTx | [15:8] | RESERVED | | | | | | | | 0x0000 | RW |
| | | [7:0] | SLOT_ ENABLE_OUT | REVERSE_ OUT_BYTE | SERIAL_ OUT_SEL | CHANNEL_OUT_POS | | | BYTE_OUT_POS | | | |
| 0xF400 | HIBERNATE | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | HIBERNATE | | |
| 0xF401 | START_PULSE | [15:8] | RESERVED[10:3] | | | | | | | | 0x0002 | RW |
| | | [7:0] | RESERVED[2:0] | | | START_PULSE | | | | | | |
| 0xF402 | START_CORE | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | START_CORE | | |
| 0xF403 | KILL_CORE | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | KILL_CORE | | |
| 0xF404 | START_ADDRESS | [15:8] | START_ADDRESS[15:8] | | | | | | | | 0x0000 | RW |
| | | [7:0] | START_ADDRESS[7:0] | | | | | | | | | |
| 0xF405 | CORE_STATUS | [15:8] | RESERVED[12:5] | | | | | | | | 0x0000 | R |
| | | [7:0] | RESERVED[4:0] | | | | | CORE_STATUS | | | | |
| 0xF420 | DEBUG_MODE | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | DEBUG_MODE | | |
| 0xF421 | PANIC_CLEAR | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | PANIC_CLEAR | | |
| 0xF422 | PANIC_PARITY_MASK | [15:8] | RESERVED | | | | DM1_BANK3_ MASK | DM1_BANK2_ MASK | DM1_BANK1_ MASK | DM1_BANK0_ MASK | 0x0003 | RW |
| | | [7:0] | DM0_BANK3_ MASK | DM0_BANK2_ MASK | DM0_BANK1_ MASK | DM0_BANK0_ MASK | PM1_MASK | PM0_MASK | ASRC1_MASK | ASRC0_MASK | | |
| 0xF423 | PANIC_SOFTWARE_ MASK | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | PANIC_ SOFTWARE | | |
| 0xF424 | PANIC_WD_MASK | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | PANIC_WD | | |
| 0xF425 | PANIC_STACK_MASK | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | PANIC_STACK | | |
| 0xF426 | PANIC_LOOP_MASK | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | RW |
| | | [7:0] | RESERVED[6:0] | | | | | | | PANIC_LOOP | | |
| 0xF427 | PANIC_FLAG | [15:8] | RESERVED[14:7] | | | | | | | | 0x0000 | R |
| | | [7:0] | RESERVED[6:0] | | | | | | | PANIC_FLAG | | |
| 0xF428 | PANIC_CODE | [15:8] | ERR_SOFT | ERR_LOOP | ERR_STACK | ERR_ WATCHDOG | ERR_DM1B3 | ERR_DM1B2 | ERR_DM1B1 | ERR_DM1B0 | 0x0000 | R |
| | | [7:0] | ERR_DM0B3 | ERR_DM0B2 | ERR_DM0B1 | ERR_DM0B0 | ERR_PM1 | ERR_PM0 | ERR_ASRC1 | ERR_ASRC0 | | |
| 0xF429 | DECODE_OP0 | [15:8] | DECODE_OP0[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_OP0[7:0] | | | | | | | | | |
| 0xF42A | DECODE_OP1 | [15:8] | DECODE_OP1[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_OP1[7:0] | | | | | | | | | |
| 0xF42B | DECODE_OP2 | [15:8] | DECODE_OP2[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_OP2[7:0] | | | | | | | | | |
| 0xF42C | DECODE_OP3 | [15:8] | DECODE_OP3[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_OP3[7:0] | | | | | | | | | |
| 0xF42D | EXECUTE_OP0 | [15:8] | DECODE_EX0[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_EX0[7:0] | | | | | | | | | |
| 0xF42E | EXECUTE_OP1 | [15:8] | DECODE_EX1[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_EX1[7:0] | | | | | | | | | |
| 0xF42F | EXECUTE_OP2 | [15:8] | DECODE_EX2[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_EX2[7:0] | | | | | | | | | |
| 0xF430 | EXECUTE_OP3 | [15:8] | DECODE_EX3[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_EX3[7:0] | | | | | | | | | |
| 0xF431 | DECODE_COUNT | [15:8] | DECODE_COUNT[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | DECODE_COUNT[7:0] | | | | | | | | | |
| 0xF432 | EXECUTE_COUNT | [15:8] | EXECUTE_COUNT[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | EXECUTE_COUNT[7:0] | | | | | | | | | |
| 0xF433 | SOFTWARE_VALUE_0 | [15:8] | SOFTWARE_VALUE_0[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | SOFTWARE_VALUE_0[7:0] | | | | | | | | | |
| 0xF434 | SOFTWARE_VALUE_1 | [15:8] | SOFTWARE_VALUE_1[15:8] | | | | | | | | 0x0000 | R |
| | | [7:0] | SOFTWARE_VALUE_1[7:0] | | | | | | | | | |
| 0xF443 | WATCHDOG_ MAXCOUNT | [15:8] | RESERVED | | | WD_MAXCOUNT[12:8] | | | | | 0x0000 | RW |
| | | [7:0] | WD_MAXCOUNT[7:0] | | | | | | | | | |

### *Power Enable 1 Register*

**Address: 0xF051, Reset: 0x0000, Name: POWER_ENABLE1**

For the purpose of power savings, this register allows the PDM microphone interfaces, S/PDIF interfaces, and auxiliary ADCs to be disabled when not in use. When these functional blocks are disabled, the current draw on the corresponding supply pins decreases.

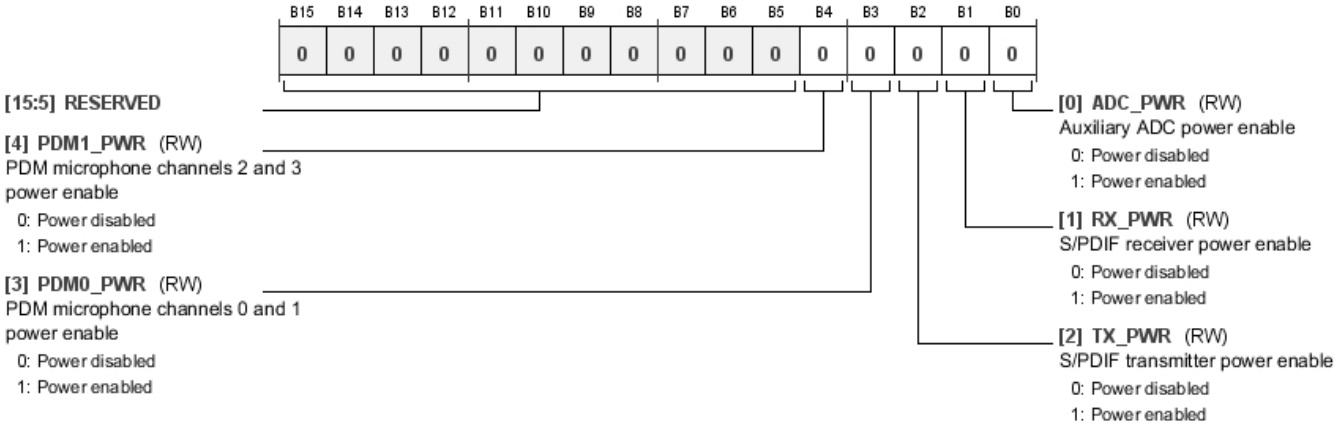


**Table 75. Bit Descriptions for POWER_ENABLE1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:5] | RESERVED | | | 0x0 | RW |
| 4 | PDM1_PWR | | PDM Microphone Channel 2 and PDM Microphone Channel 3 power enable. When this bit is disabled, PDM Microphone Channel 2 and PDM Microphone Channel 3 and their associated circuitry are disabled, and their data values cease to update. | 0x0 | RW |
| | | 0 | Power disabled | | |
| | | 1 | Power enabled | | |
| 3 | PDM0_PWR | | PDM Microphone Channel 0 and PDM Microphone Channel 1 power enable. When this bit is disabled, PDM Microphone Channel 0 and PDM Microphone Channel 1 and their associated circuitry are disabled, and their data values cease to update. | 0x0 | RW |
| | | 0 | Power disabled | | |
| | | 1 | Power enabled | | |
| 2 | TX_PWR | | S/PDIF transmitter power enable. This bit disables the S/PDIF transmitter circuit. Clock and data ceases to output from the S/PDIF transmitter pin, and the output is held at logic low as long as this bit is disabled. | 0x0 | RW |
| | | 0 | Power disabled | | |
| | | 1 | Power enabled | | |
| 1 | RX_PWR | | S/PDIF receiver power enable. This bit disables the S/PDIF receiver circuit. Clock and data recovery from the S/PDIF input stream ceases until this bit is reenabled. | 0x0 | RW |
| | | 0 | Power disabled | | |
| | | 1 | Power enabled | | |
| 0 | ADC_PWR | | Auxiliary ADC power enable. When this bit is disabled, the auxiliary ADCs are powered down, their outputs cease to update, and they hold their last value. | 0x0 | RW |
| | | 0 | Power disabled | | |
| | | 1 | Power enabled | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 8 | DM1_BANK3_SUBBANK0_MASK | | Bank 3 Subbank 0 mask. | 0x0 | RW |
| | | 0 | Report Bank 3 Subbank 0 parity errors | | |
| | | 1 | Ignore Bank 3 Subbank 0 parity errors | | |
| [7:5] | RESERVED | | Reserved. | 0x0 | RW |
| 4 | DM1_BANK2_SUBBANK4_MASK | | Bank 2 Subbank 4 mask. | 0x0 | RW |
| | | 0 | Report Bank 2 Subbank 4 parity errors | | |
| | | 1 | Ignore Bank 2 Subbank 4 parity errors | | |
| 3 | DM1_BANK2_SUBBANK3_MASK | | Bank 2 Subbank 3 mask. | 0x0 | RW |
| | | 0 | Report Bank 2 Subbank 3 parity errors | | |
| | | 1 | Ignore Bank 2 Subbank 3 parity errors | | |
| 2 | DM1_BANK2_SUBBANK2_MASK | | Bank 2 Subbank 2 mask. | 0x0 | RW |
| | | 0 | Report Bank 2 Subbank 2 parity errors | | |
| | | 1 | Ignore Bank 2 Subbank 2 parity errors | | |
| 1 | DM1_BANK2_SUBBANK1_MASK | | Bank 2 Subbank 1 mask. | 0x0 | RW |
| | | 0 | Report Bank 2 Subbank 1 parity errors | | |
| | | 1 | Ignore Bank 2 Subbank 1 parity errors | | |
| 0 | DM1_BANK2_SUBBANK0_MASK | | Bank 2 Subbank 0 mask. | 0x0 | RW |
| | | 0 | Report Bank 2 Subbank 0 parity errors | | |
| | | 1 | Ignore Bank 2 Subbank 0 parity errors | | |

### *Panic Mask Parity PM Bank [1:0] Register*

**Address: 0xF46B, Reset: 0x0000, Name: PANIC_PARITY_MASK5**

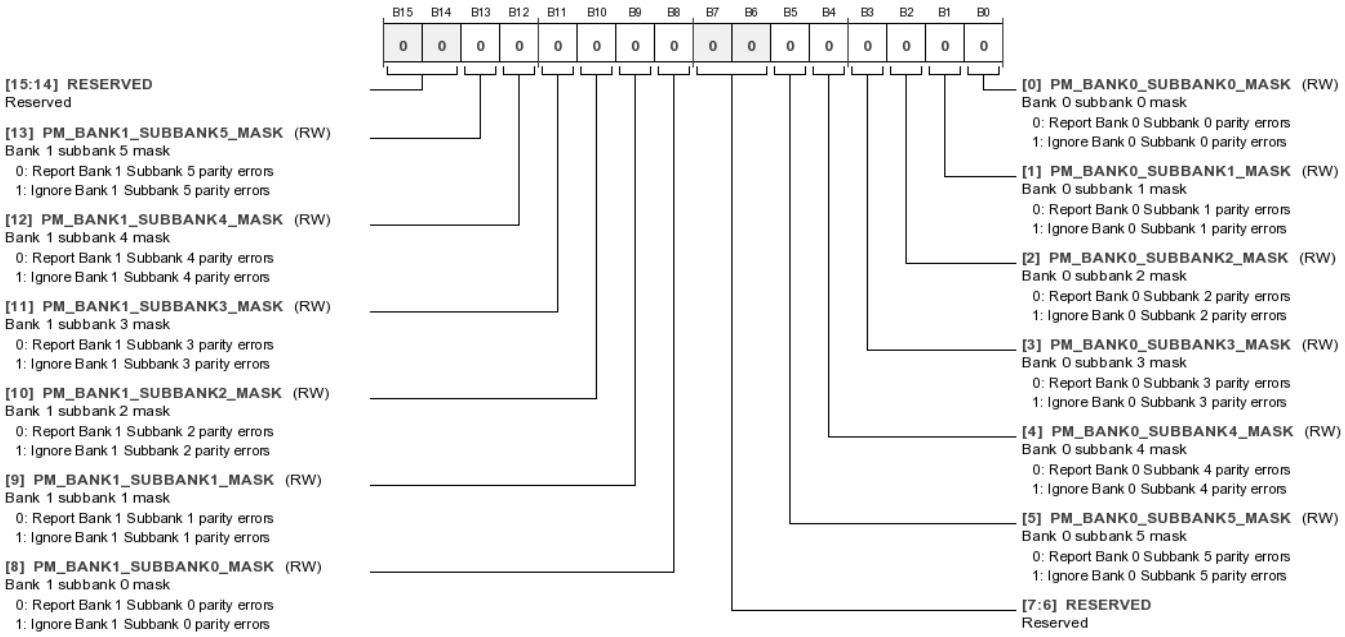


**Table 116. Bit Descriptions for PANIC_PARITY_MASK5**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:14] | RESERVED | | Reserved. | 0x0 | RW |
| 13 | PM_BANK1_SUBBANK5_MASK | | Bank 1 Subbank 5 mask. | 0x0 | RW |
| | | 0 | Report Bank 1 Subbank 5 parity errors | | |
| | | 1 | Ignore Bank 1 Subbank 5 parity errors | | |
| 12 | PM_BANK1_SUBBANK4_MASK | | Bank 1 Subbank 4 mask. | 0x0 | RW |
| | | 0 | Report Bank 1 Subbank 4 parity errors | | |
| | | 1 | Ignore Bank 1 Subbank 4 parity errors | | |

## S/PDIF INTERFACE REGISTERS

### *S/PDIF Receiver Lock Bit Detection Register*

**Address: 0xF600, Reset: 0x0000, Name: SPDIF_LOCK_DET**

This register contains a flag that monitors the S/PDIF receiver and provides a way to check the validity of the input signal.

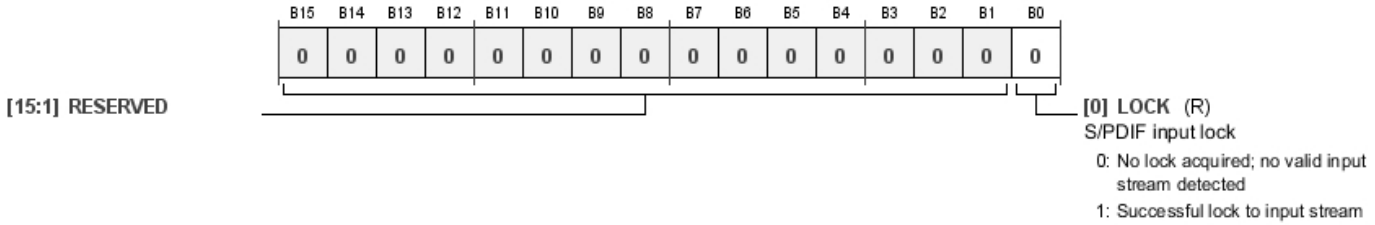


**Table 132. Bit Descriptions for SPDIF_LOCK_DET**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:1] | RESERVED | | | 0x0 | RW |
| 0 | LOCK | | S/PDIF input lock. | 0x0 | R |
| | | 0 | No lock acquired; no valid input stream detected | | |
| | | 1 | Successful lock to input stream | | |

### *S/PDIF Receiver Control Register*

**Address: 0xF601, Reset: 0x0000, Name: SPDIF_RX_CTRL**

This register provides controls that govern the behavior of the S/PDIF receiver on the ADAU1466 and ADAU1462.

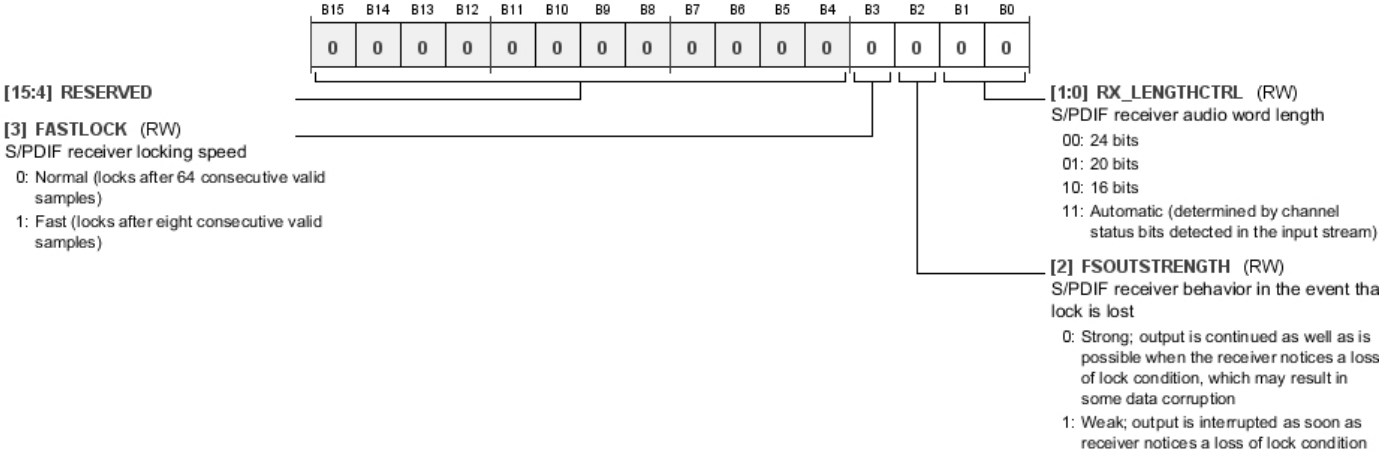


**Table 133. Bit Descriptions for SPDIF_RX_CTRL**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:4] | RESERVED | | | 0x0 | RW |
| 3 | FASTLOCK | | S/PDIF receiver locking speed. | 0x0 | RW |
| | | 0 | Normal (locks after 64 consecutive valid samples) | | |
| | | 1 | Fast (locks after eight consecutive valid samples) | | |
| 2 | FSOUTSTRENGTH | | S/PDIF receiver behavior in the event that lock is lost. FSOUTSTRENGTH applies to the output of the recovered frame clock from the S/PDIF receiver. | 0x0 | RW |
| | | 0 | Strong; output is continued as well as is possible when the receiver notices a loss of lock condition, which may result in some data corruption | | |
| | | 1 | Weak; output is interrupted as soon as receiver notices a loss of lock condition | | |
| [1:0] | RX_LENGTHCTRL | | S/PDIF receiver audio word length. | 0x0 | RW |
| | | 00 | 24 bits | | |
| | | 01 | 20 bits | | |
| | | 10 | 16 bits | | |
| | | 11 | Automatic (determined by channel status bits detected in the input stream) | | |

### *BCLK Output Pins Drive Strength and Slew Rate Register*

**Address: 0xF784 to 0xF787 (Increments of 0x1), Reset: 0x0018, Name: BCLK_OUTx_PIN**

These registers configure the drive strength, slew rate, and pull resistors for the BCLK_OUTx pins. Register 0xF784 corresponds to BCLK_OUT0, Register 0xF785 corresponds to BCLK_OUT1, Register 0xF786 corresponds to BCLK_OUT2, and Register 0xF787 corresponds to BCLK_OUT3.

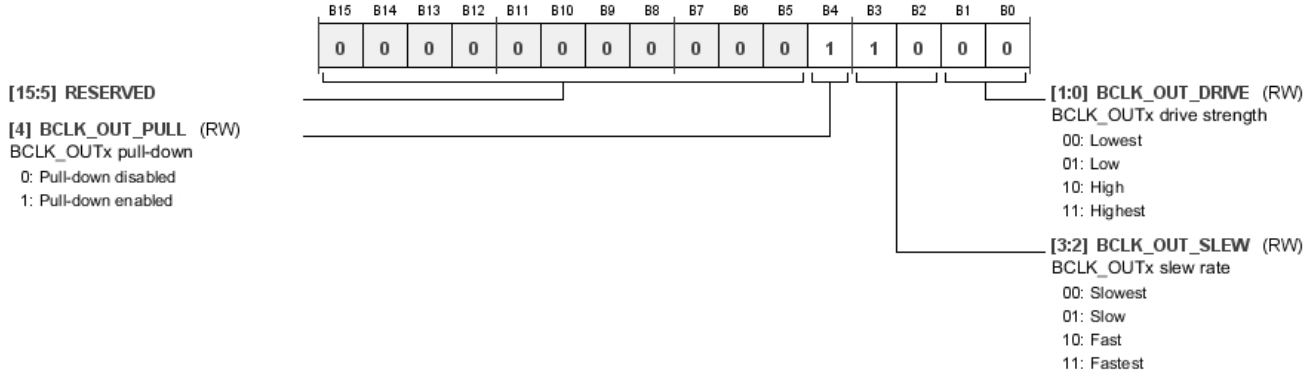


**Table 160. Bit Descriptions for BCLK_OUTx_PIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:5] | RESERVED | | | 0x0 | RW |
| 4 | BCLK_OUT_PULL | | BCLK_OUTx pull-down. | 0x1 | RW |
| | | 0 | Pull-down disabled | | |
| | | 1 | Pull-down enabled | | |
| [3:2] | BCLK_OUT_SLEW | | BCLK_OUTx slew rate. | 0x2 | RW |
| | | 00 | Slowest | | |
| | | 01 | Slow | | |
| | | 10 | Fast | | |
| | | 11 | Fastest | | |
| [1:0] | BCLK_OUT_DRIVE | | BCLK_OUTx drive strength. | 0x0 | RW |
| | | 00 | Lowest | | |
| | | 01 | Low | | |
| | | 10 | High | | |
| | | 11 | Highest | | |

### *LRCLK Input Pins Drive Strength and Slew Rate Register*

**Address: 0xF788 to 0xF78B (Increments of 0x1), Reset: 0x0018, Name: LRCLK_INx_PIN**

These registers configure the drive strength, slew rate, and pull resistors for the LRCLK_INx pins. Register 0xF788 corresponds to LRCLK_IN0/MP10, Register 0xF789 corresponds to LRCLK_IN1/MP11, Register 0xF78A corresponds to LRCLK_IN2/MP12, and Register 0xF78B corresponds to LRCLK_IN3/MP13.

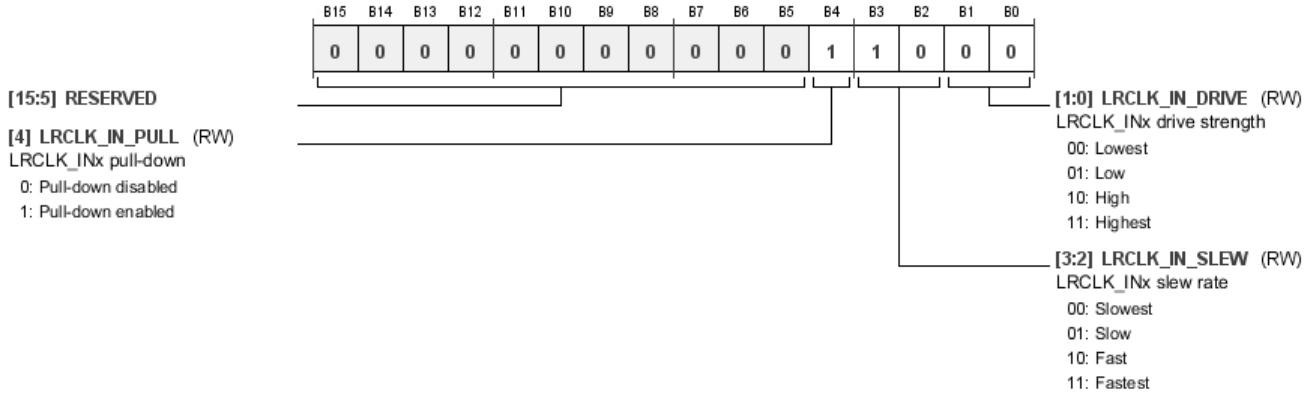


**Table 161. Bit Descriptions for LRCLK_INx_PIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:5] | RESERVED | | | 0x0 | RW |
| 4 | LRCLK_IN_PULL | | LRCLK_INx pull-down. | 0x1 | RW |
| | | 0 | Pull-down disabled | | |
| | | 1 | Pull-down enabled | | |
| [3:2] | LRCLK_IN_SLEW | | LRCLK_INx slew rate. | 0x2 | RW |
| | | 00 | Slowest | | |
| | | 01 | Slow | | |
| | | 10 | Fast | | |
| | | 11 | Fastest | | |
| [1:0] | LRCLK_IN_DRIVE | | LRCLK_INx drive strength. | 0x0 | RW |
| | | 00 | Lowest | | |
| | | 01 | Low | | |
| | | 10 | High | | |
| | | 11 | Highest | | |

### *MISO/SDA Pin Drive Strength and Slew Rate Register*

**Address: 0xF79A, Reset: 0x0008, Name: MISO_SDA_PIN**

This register configures the drive strength, slew rate, and pull resistors for the MISO/SDA pin.

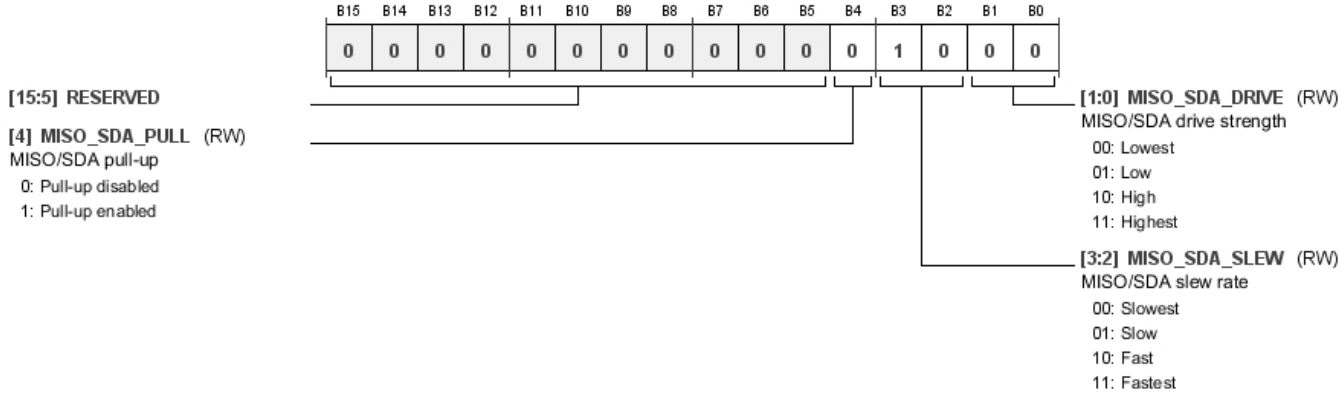


**Table 167. Bit Descriptions for MISO_SDA_PIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:5] | RESERVED | | | 0x0 | RW |
| 4 | MISO_SDA_PULL | | MISO/SDA pull-up. | 0x0 | RW |
| | | 0 | Pull-up disabled | | |
| | | 1 | Pull-up enabled | | |
| [3:2] | MISO_SDA_SLEW | | MISO/SDA slew rate. | 0x2 | RW |
| | | 00 | Slowest | | |
| | | 01 | Slow | | |
| | | 10 | Fast | | |
| | | 11 | Fastest | | |
| [1:0] | MISO_SDA_DRIVE | | MISO/SDA drive strength. | 0x0 | RW |
| | | 00 | Lowest | | |
| | | 01 | Low | | |
| | | 10 | High | | |
| | | 11 | Highest | | |

### *SS/ADDR0 Pin Drive Strength and Slew Rate Register*

**Address: 0xF79B, Reset: 0x0018, Name: SS_PIN**

This register configures the drive strength, slew rate, and pull resistors for the SS/ADDR0 pin.

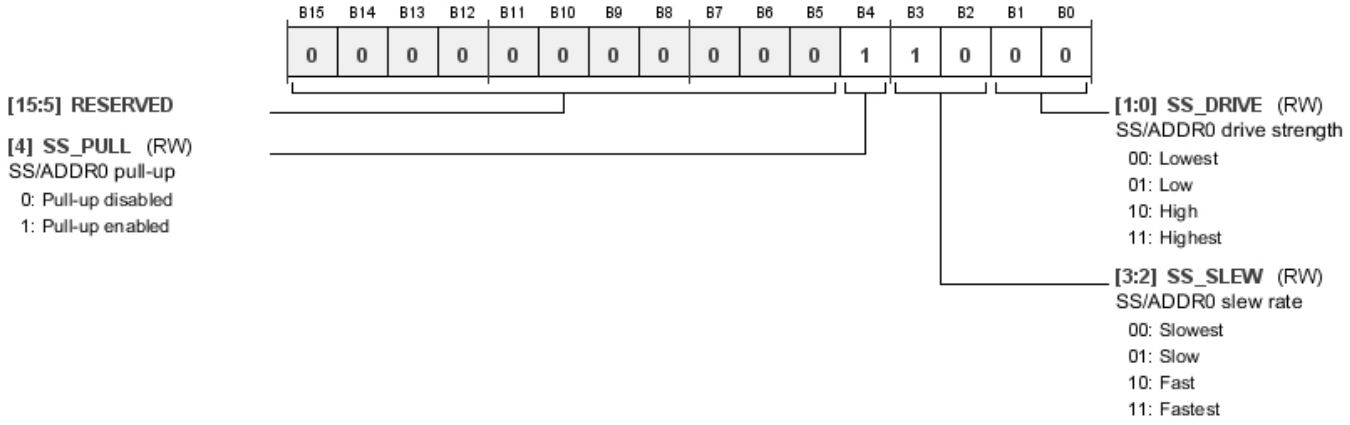


**Table 168. Bit Descriptions for SS_PIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:5] | RESERVED | | | 0x0 | RW |
| 4 | SS_PULL | | SS/ADDR0 pull-up. | 0x1 | RW |
| | | 0 | Pull-up disabled | | |
| | | 1 | Pull-up enabled | | |
| [3:2] | SS_SLEW | | SS/ADDR0 slew rate. | 0x2 | RW |
| | | 00 | Slowest | | |
| | | 01 | Slow | | |
| | | 10 | Fast | | |
| | | 11 | Fastest | | |
| [1:0] | SS_DRIVE | | SS/ADDR0 drive strength. | 0x0 | RW |
| | | 00 | Lowest | | |
| | | 01 | Low | | |
| | | 10 | High | | |
| | | 11 | Highest | | |

### *CLKOUT Pin Drive Strength and Slew Rate Register*

**Address: 0xF7A3, Reset: 0x0008, Name: CLKOUT_PIN**

This register configures the drive strength, slew rate, and pull resistors for the CLKOUT pin.

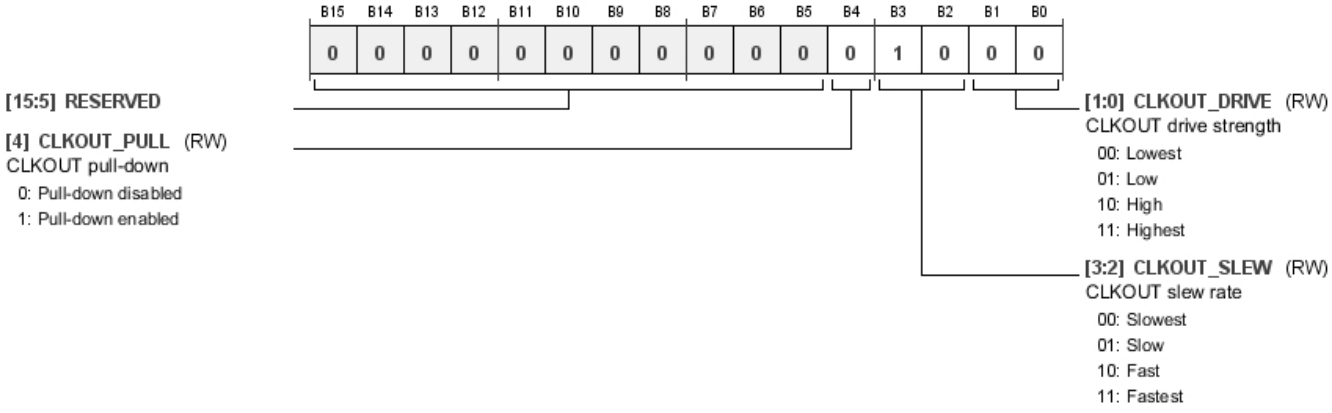


**Table 176. Bit Descriptions for CLKOUT_PIN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [15:5] | RESERVED | | | 0x0 | RW |
| 4 | CLKOUT_PULL | | CLKOUT pull-down. | 0x0 | RW |
| | | 0 | Pull-down disabled | | |
| | | 1 | Pull-down enabled | | |
| [3:2] | CLKOUT_SLEW | | CLKOUT slew rate. | 0x2 | RW |
| | | 00 | Slowest | | |
| | | 01 | Slow | | |
| | | 10 | Fast | | |
| | | 11 | Fastest | | |
| [1:0] | CLKOUT_DRIVE | | CLKOUT drive strength. | 0x0 | RW |
| | | 00 | Lowest | | |
| | | 01 | Low | | |
| | | 10 | High | | |
| | | 11 | Highest | | |