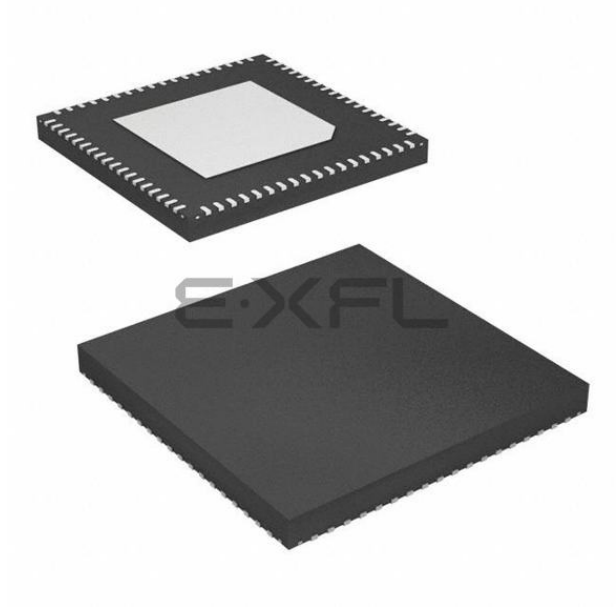

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	294.912MHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	320kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	72-VFQFN Exposed Pad, CSP
Supplier Device Package	72-LFCSP-VQ (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1466wbcpz300rl

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ELECTRICAL CHARACTERISTICS

Digital Input/Output

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT					
Input Voltage					Excluding SPDIFIN, which is not a standard digital input
IOVDD = 3.3 V					
High Level (V_{IH})	1.71		3.3	V	
Low Level (V_{IL})	0		1.71	V	
IOVDD = 1.8 V					
High Level (V_{IH})	0.92		1.8	V	
Low Level (V_{IL})	0		0.89	V	
Input Leakage					
High Level (I_{IH})			2	µA	Digital input pins with pull-up resistor
			14	µA	Digital input pins with pull-down resistor
			2	µA	Digital input pins with no pull resistor
			8	µA	MCLK
			120	µA	SPDIFIN
Low Level (I_{IL}) at 0 V	−14			µA	Digital input pins with pull-up resistor
	−2			µA	Digital input pins with pull-down resistor
	−2			µA	Digital input pins with no pull resistor
	−8			µA	MCLK
	−120			µA	SPDIFIN
Input Capacitance (C_I)		2		pF	Guaranteed by design
DIGITAL OUTPUT					
Output Voltage					
IOVDD = 3.3 V					
High Level (V_{OH})	3.09		3.3	V	I_{OH} = 1 mA
Low Level (V_{OL})	0		0.26	V	I_{OL} = 1 mA
IOVDD = 1.8 V					
High Level (V_{OH})	1.45		1.8		
Low Level (V_{OL})	0		0.33		
Digital Output Pins, Output Drive					The digital output pins are driving low impedance PCB traces to a high impedance digital input buffer
IOVDD = 1.8 V					
Drive Strength Setting					
Lowest			1	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
Low			2	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
High			3	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
Highest			5	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
IOVDD = 3.3 V					
Drive Strength Setting					
Lowest			2	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
Low			5	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
High			10	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
Highest			15	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly

I²C Interface—Slave

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, default drive strength (f_{SCL}) = 400 kHz.

Table 11.

Parameter	Min	Max	Unit	Description
f_{SCL}		1000	kHz	SCL clock frequency
t_{SCLH}	0.26		µs	SCL pulse width high
t_{SCLL}	0.5		µs	SCL pulse width low
t_{SCS}	0.26		µs	Start and repeated start condition setup time
t_{SCH}	0.26		µs	Start condition hold time
t_{DS}	50		ns	Data setup time
t_{DH}		0.45	µs	Data hold time
t_{SCLR}		120	ns	SCL rise time
t_{SCLF}		120	ns	SCL fall time
t_{SDR}		120	ns	SDA rise time
t_{SDF}		120	ns	SDA fall time
t_{BFT}	0.5		µs	Bus free time between stop and start
t_{SUSTO}	0.26		µs	Stop condition setup time

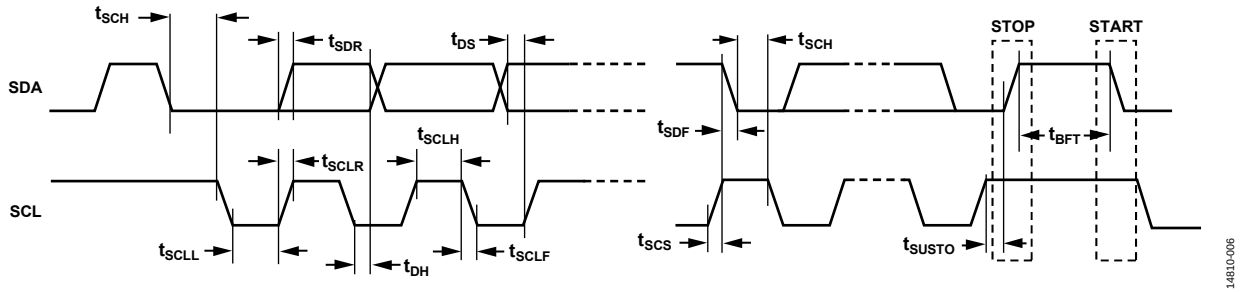
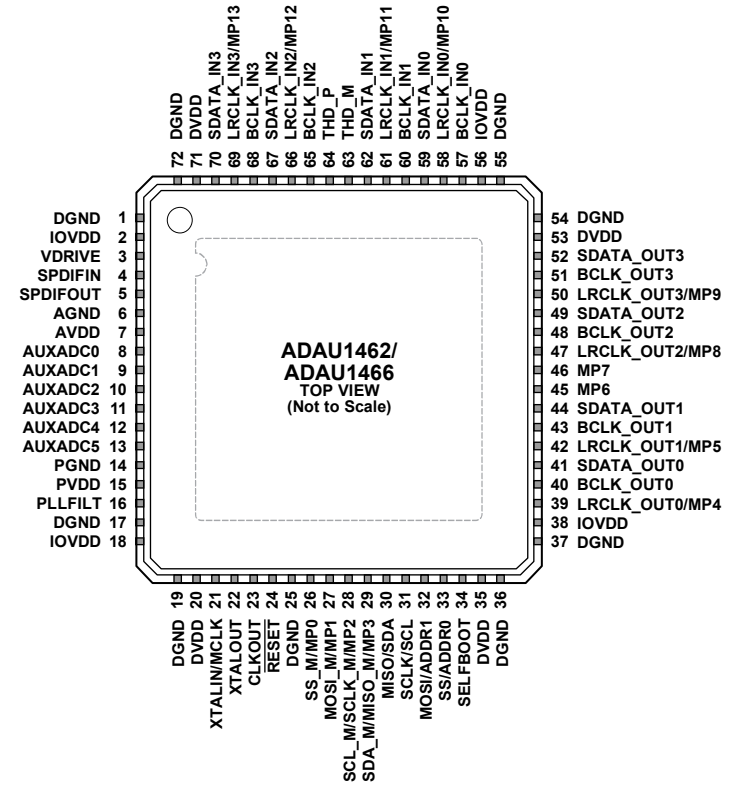


Figure 6. I²C Slave Port Timing Specifications

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE GROUNDED BY SOLDERING IT TO A COPPER SQUARE OF EQUIVALENT SIZE ON THE PCB. IDENTICAL COPPER SQUARES MUST EXIST ON ALL LAYERS OF THE BOARD, CONNECTED BY VIAS, AND THEY MUST BE CONNECTED TO A DEDICATED COPPER GROUND LAYER WITHIN THE PCB.

Figure 11. Pin Configuration

Table 18. Pin Function Descriptions

Pin No.	Mnemonic	Internal Pull Resistor	Description
1	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
2	IOVDD	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this pin with decoupling capacitors to Pin 1 (DGND). See the Power Supply Bypass Capacitors and Grounding sections.
3	VDRIVE	None	PNP Bipolar Junction Transistor-Base Drive Bias Pin for the Digital Supply Regulator. Connect VDRIVE to the base of an external PNP pass transistor (ON Semi NSS1C300ET4G is recommended). If an external supply is provided directly to DVDD, connect the VDRIVE pin to ground.
4	SPDIFIN	None	Input to the Integrated Sony/Philips Digital Interconnect Format Receiver. Disconnect this pin when not in use. This pin is internally biased to IOVDD/2.
5	SPDIFOUT	Configurable	Output from the Integrated Sony/Philips Digital Interface Format Transmitter. Disconnect this pin when not in use. This pin is internally biased to IOVDD/2.
6	AGND	None	Analog Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
7	AVDD	None	Analog (Auxiliary ADC) Supply. Must be 3.3 V ± 10%. Bypass this pin with decoupling capacitors to Pin 6 (AGND). See the Power Supply Bypass Capacitors and Grounding sections.
8	AUXADC0	None	Auxiliary ADC Input Channel 0. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.
9	AUXADC1	None	Auxiliary ADC Input Channel 1. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.
10	AUXADC2	None	Auxiliary ADC Input Channel 2. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.

INITIALIZATION

Power-Up Sequence

The first step in the initialization sequence is to power up the device. First, apply voltage to the power pins. All the power pins can be supplied simultaneously. If the power pins are not supplied simultaneously, supply IOVDD first because the internal ESD protection diodes are referenced to the IOVDD voltage. AVDD, DVDD, and PVDD can be supplied at the same time as IOVDD or after, but they must not be supplied prior to IOVDD. The order in which AVDD, DVDD, and PVDD are supplied does not matter.

DVDD, the power supply for the internal digital logic, can be regulated and supplied directly or it can by generated from IOVDD using an internal voltage regulator. When the internal regulator is not used and DVDD is directly supplied, no special sequence is required when providing the proper voltages to AVDD, DVDD, and PVDD.

When the internal regulator is used, DVDD is derived from IOVDD in combination with an external pass transistor, after AVDD, IOVDD, and PVDD are supplied. See the Power Supplies section for more information.

Each power supply domain has its own internal power-on reset (POR) circuits (also known as power OK circuits) to ensure that the level shifters attached to each power domain can be initialized properly. AVDD and PVDD must reach their nominal level before the auxiliary ADC and PLL can be used, respectively.

However, the AVDD and PVDD supplies have no role in the rest of the power-up sequence. After the AVDD power reaches its nominal threshold, the regulator becomes active and begins to charge up the DVDD supply. The DVDD supply also has a POR circuit to ensure that the level shifters initialize during power-up.

The POR signals are combined into three global level shifter resets that properly initialize the signal crossings between each separate power domain and DVDD.

The digital circuits remain in reset until the IOVDD to DVDD level shifter reset is released. At that point, the digital circuits exit reset.

When a crystal is in use, the crystal oscillator circuit must provide a stable master clock to the XTALIN/MCLK pin by the time the PVDD supply reaches its nominal level. The XTALIN/MCLK pin is restricted from passing into the PLL circuitry until the DVDD POR signal becomes active and the PVDD to DVDD level shifter is initialized.

When all four POR circuits signal that the power-on conditions are met, a reset synchronizer circuit releases the internal digital circuitry from reset, provided that the following conditions are met:

- A valid MCLK signal is provided to the digital circuitry and the PLL.
- The $\overline{\text{RESET}}$ pin is high.

When the internal digital circuitry becomes active, the DSP core runs eight lines of initialization code stored in read-only memory (ROM), requiring eight cycles of the MCLK signal. For a 12.288 MHz MCLK input, this process takes 650 ns.

After the ROM program completes its execution, the PLL is ready to be configured using register writes to Register 0xF000 (PLL_CTRL0), Register 0xF001 (PLL_CTRL1), Register 0xF002 (PLL_CLK_SRC), and Register 0xF003 (PLL_ENABLE).

When the PLL is configured and enabled, the PLL starts to lock to the incoming master clock signal. The absolute maximum PLL lock time is 32 × 1024 = 32,768 clock cycles on the clock signal (after the input prescaler), which is fed to the input of the PLL. In a standard 48 kHz use case, the PLL input clock frequency after the prescaler is 3.072 MHz; therefore, the maximum PLL lock time is 10.666 ms.

Typically, the PLL locks much faster than 10.666 ms. In most systems, the PLL locks within about 3.5 ms. The PLL_LOCK register (Address 0xF004) can be polled via the control port until Bit 0 (PLL_LOCK) goes high, signifying that the PLL lock is complete.

While the PLL is attempting to lock to the input clock, the I^2C slave and SPI slave control ports are inactive; therefore, no other registers are accessible over the control port. While the PLL is attempting to lock, all attempts to write to the control port fail.

Figure 13 shows an example power-up sequence with all relevant signals labeled. If possible, apply the required voltage to all four power supply domains (IOVDD, AVDD, PVDD, and DVDD) simultaneously. If the power supplies are separate, IOVDD, which is the reference for the ESD protection diodes that are situated inside the input and output pins, must be applied first to avoid stressing these diodes. PVDD, AVDD, and DVDD can then be supplied in any order (see the System Initialization Sequence section for more information). Note that the gray areas in Figure 13 represent clock signals.

System Initialization Sequence

Before the IC can process the audio in the DSP, the following initialization sequence must be completed.

1. If possible, apply the required voltage to all four power supply domains (IOVDD, AVDD, PVDD, and DVDD) simultaneously. If simultaneous application is not possible, supply IOVDD first to prevent damage or reduced operating lifetime. If using the on-board regulator, AVDD and PVDD can be supplied in any order, and DVDD is then generated automatically. If not using the on-board regulator, AVDD, PVDD, and DVDD can be supplied in any order following IOVDD.
2. Start providing a master clock signal to the XTALIN/MCLK pin, or, if using the crystal oscillator, let the crystal oscillator start generating a master clock signal. The master clock signal must be valid when the DVDD supply stabilizes.
3. If the SELFBOOT pin is pulled high, a self boot sequence initiates on the master control port. Wait until the self boot operation is complete.
4. If SPI slave control mode is desired, toggle the SS/ADDR0 pin three times. Ensure that each toggle lasts at least the duration of one cycle of the master clock being input to the XTALIN/MCLK pin. When the SS/ADDR0 line rises for the third time, the slave control port is then in SPI mode.
5. Execute the register and memory write sequence that is required to configure the device in the proper operating mode.

Table 19 contains an example series of register writes used to configure the system at startup. The contents of the data column may vary depending on the system configuration. The configuration that is listed in Table 19 represents the default initialization sequence for project files generated in SigmaStudio.

Recommended Program/Parameter Loading Procedure

When writing large amounts of data to the program or parameter RAM in direct write mode (such as when downloading the initial contents of the RAMs from an external memory), use the hibernate register (Address 0xF400) to disable the processor core, thus preventing unpleasant noises from appearing at the audio output. When small amounts of data are transmitted during real-time operation of the DSP (such as when updating individual parameters), the software safeload mechanism can be used (see the Software Safeload section).

SLAVE CONTROL PORTS

A total of four control ports are available: two slave ports and two master ports. The slave I²C port and slave SPI port allow an external master device to modify the contents of the memory and registers. The master I²C port and master SPI port allow the device to self boot and to send control messages to slave devices on the same bus.

Slave Control Port Overview

To program the DSP and configure the control registers, a slave port is available that can communicate using either the I²C or SPI protocols. Any external device that controls the ADAU1462/ADAU1466, including a hardware interface used with SigmaStudio for development or a microcontroller in a large running system, uses the slave control port to communicate with the DSP. This port is unrelated to the master communications port that also uses the I²C or SPI protocols. The master port enables applications without an external controller and can read from an external EEPROM to self boot and control external ICs.

The slave communications port defaults to I²C mode; however, it can be put into SPI mode by toggling SS (SS/ADDR0), the slave select pin, from high to low three times. The slave select pin must be held low for at least one master clock period (that is, one period of the clock on the XTALIN_MCLK input pin). Only the PLL configuration registers (0xF000 to 0xF004) are accessible before the PLL locks. For this reason, always write to the PLL registers first after the chip powers up. After the PLL locks, the remaining registers and the RAM become accessible. See the System Initialization Sequence section for more information.

SLAVE CONTROL PORT ADDRESSING

Unlike earlier SigmaDSP processors, the ADAU1462/ADAU1466 slave control port 16-bit addressing cannot provide direct access to the total amount of memory available to the DSP core on its wider internal busses. Full read/write access to all memory and addressable registers is possible, but it must be accessed as two pages of memory in the slave control port address space. Page 0 is referred to as lower memory and Page 1 as upper memory. The single-bit register SECONDPAGE_ENABLE (0xF899) selects the active page.

Within a page, all addresses are accessible using both single address mode and burst mode. The first byte (Byte 0) of a control port write contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the register location within the memory maps of the ADAU1462/ADAU1466. This subaddress must be two bytes long because the memory locations within the devices are directly addressable, and their sizes exceed the range of single byte addressing. The third byte to the end of the sequence contain the data, such as control port data, program data, or parameter data. The number of bytes written per word depends on the type of data. For more information, see the Burst Mode Writing and Reading section. The ADAU1462/ADAU1466 must have a valid master clock to write to the slave control port, with the exception of the PLL configuration registers, 0xF000 to 0xF004.

If large blocks of data must be downloaded, halt the output of the DSP core (using Register 0xF400, HIBERNATE), load new data, and then restart the device (using Register 0xF402, START_CORE). This process is most common during the booting sequence at startup or when loading a new program into RAM because the ADAU1462/ADAU1466 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks.

When updating a signal processing parameter while the DSP core is running, use the software safeload function. This function allows atomic writes to memory and prevents updates to parameters across the boundary of an audio frame, which can lead to an audio artifact such as a click or pop sound. For more information, see the Software Safeload section.

The slave control port supports either I²C or SPI, but not simultaneously. The function of each pin is described in Table 25 for the two modes.

Burst Mode Writing and Reading

Burst write and read modes are available for convenience when writing large amounts of data to contiguous registers. In these modes, the chip and memory addresses are written once, and then a large amount of data can follow uninterrupted. The subaddresses are automatically incremented at the word boundaries. This increment happens automatically after a single word write or read unless a stop condition is encountered (I²C mode) or the slave select is disabled and brought high (SPI mode). A burst write starts like a single word write, but, following the first data-word, the data-word for the next address can be written immediately without sending its 2-byte address. The control registers in the ADAU1462/ADAU1466 are two bytes wide, and the memories are four bytes wide. The auto-increment feature knows the word length at each subaddress; therefore, it is not necessary to manually specify the subaddress for each address in a burst write.

The subaddresses are automatically incremented by one address, following each read or write of a data-word, regardless of whether there is a valid register or RAM word at that address.

Footer Format

After all the data blocks, a footer signifies the end of the self boot EEPROM memory (see Figure 42). The footer consists of a 64-bit checksum, which is the sum of the header and all blocks and all data as 32-bit words.

After the self boot operation completes, the checksum of the downloaded data is calculated and the panic manager signals if it does not match the checksum in the EEPROM. If the checksum is set to 0 (decimal), the checksum checking is disabled.

Considerations when Using a 1 Mb I²C Self Boot EEPROM

Because of the way I²C addressing works, 1 Mb of I²C EEPROM memory can be divided, with a portion of its address space at Chip Address 0x50; another portion of the memory can be located at a different address (for example, Chip Address 0x51). The memory allocation varies, depending on the EEPROM design. When the EEPROM memory is divided, the memory portion that resides at a different chip address must be handled as though it exists in a separate EEPROM.

Considerations when Using Multiple EEPROMs on the SPI Master Bus

When multiple EEPROMs are connected on the same SPI master bus, the self boot mechanism works only with the first EEPROM.

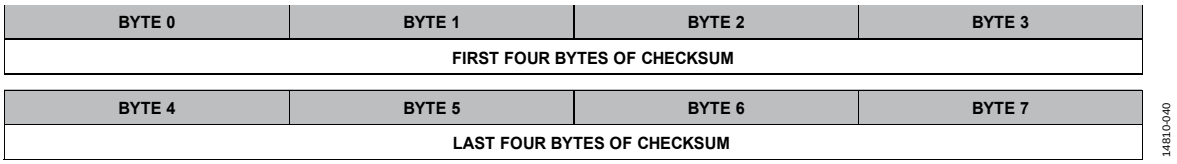


Figure 42. Self Boot EEPROM Footer Format

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0xF680 ... 0xF68B	SPDIF_RX_PB_RIGHT_x	[15:8]	SPDIF_RX_PB_RIGHT[15:8]								0x0000	R
		[7:0]	SPDIF_RX_PB_RIGHT[7:0]									
0xF690	SPDIF_TX_EN	[15:8]	RESERVED[14:7]								0x0000	RW
		[7:0]	RESERVED[6:0]							TXEN		
0xF691	SPDIF_TX_CTRL	[15:8]	RESERVED[13:6]								0x0000	RW
		[7:0]	RESERVED[5:0]							TX_ LENGTHCTRL		
0xF69F	SPDIF_TX_AUXBIT_SOURCE	[15:8]	RESERVED[14:7]								0x0000	RW
		[7:0]	RESERVED[6:0]							TX_AUXBITS_ SOURCE		
0xF6A0 ... 0xF6AB	SPDIF_TX_CS_LEFT_x	[15:8]	SPDIF_TX_CS_LEFT[15:8]								0x0000	RW
		[7:0]	SPDIF_TX_CS_LEFT[7:0]									
0xF6B0 ... 0xF6BB	SPDIF_TX_CS_RIGHT_x	[15:8]	SPDIF_TX_CS_RIGHT[15:8]								0x0000	RW
		[7:0]	SPDIF_TX_CS_RIGHT[7:0]									
0xF6C0 ... 0xF6CB	SPDIF_TX_UD_LEFT_x	[15:8]	SPDIF_TX_UD_LEFT[15:8]								0x0000	RW
		[7:0]	SPDIF_TX_UD_LEFT[7:0]									
0xF6D0 ... 0xF6DB	SPDIF_TX_UD_RIGHT_x	[15:8]	SPDIF_TX_UD_RIGHT[15:8]								0x0000	RW
		[7:0]	SPDIF_TX_UD_RIGHT[7:0]									
0xF6E0 ... 0xF6EB	SPDIF_TX_VB_LEFT_x	[15:8]	SPDIF_TX_VB_LEFT[15:8]								0x0000	RW
		[7:0]	SPDIF_TX_VB_LEFT[7:0]									
0xF6F0 ... 0xF6FB	SPDIF_TX_VB_RIGHT_x	[15:8]	SPDIF_TX_VB_RIGHT[15:8]								0x0000	RW
		[7:0]	SPDIF_TX_VB_RIGHT[7:0]									
0xF700 ... 0xF70B	SPDIF_TX_PB_LEFT_x	[15:8]	SPDIF_TX_PB_LEFT[15:8]								0x0000	RW
		[7:0]	SPDIF_TX_PB_LEFT[7:0]									
0xF710 ... 0xF71B	SPDIF_TX_PB_RIGHT_x	[15:8]	SPDIF_TX_PB_RIGHT[15:8]								0x0000	RW
		[7:0]	SPDIF_TX_PB_RIGHT[7:0]									
0xF780 ... 0xF783	BCLK_INx_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			BCLK_IN_PULL	BCLK_IN_SLEW			BCLK_IN_DRIVE		
0xF784 ... 0xF787	BCLK_OUTx_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			BCLK_OUT_ PULL	BCLK_OUT_SLEW			BCLK_OUT_DRIVE		
0xF788 ... 0xF78B	LRCLK_INx_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			LRCLK_IN_PULL	LRCLK_IN_SLEW			LRCLK_IN_DRIVE		
0xF78C ... 0xF78F	LRCLK_OUTx_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			LRCLK_OUT_ PULL	LRCLK_OUT_SLEW			LRCLK_OUT_DRIVE		
0xF790 ... 0xF793	SDATA_INx_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			SDATA_IN_PULL	SDATA_IN_SLEW			SDATA_IN_DRIVE		
0xF794 ... 0xF797	SDATA_OUTx_PIN	[15:8]	RESERVED[10:3]								0x0008	RW
		[7:0]	RESERVED[2:0]			SDATA_OUT_ PULL	SDATA_OUT_SLEW			SDATA_OUT_DRIVE		
0xF798	SPDIF_TX_PIN	[15:8]	RESERVED[10:3]								0x0008	RW
		[7:0]	RESERVED[2:0]			SPDIF_TX_PULL	SPDIF_TX_SLEW			SPDIF_TX_DRIVE		
0xF799	SCLK_SCL_PIN	[15:8]	RESERVED[10:3]								0x0008	RW
		[7:0]	RESERVED[2:0]			SCLK_SCL_PULL	SCLK_SCL_SLEW			SCLK_SCL_DRIVE		
0xF79A	MISO_SDA_PIN	[15:8]	RESERVED[10:3]								0x0008	RW
		[7:0]	RESERVED[2:0]			MISO_SDA_ PULL	MISO_SDA_SLEW			MISO_SDA_DRIVE		
0xF79B	SS_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			SS_PULL	SS_SLEW			SS_DRIVE		
0xF79C	MOSI_ADDR1_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			MOSI_ADDR1_ PULL	MOSI_ADDR1_SLEW			MOSI_ADDR1_DRIVE		
0xF79D	SCLK_SCL_M_PIN	[15:8]	RESERVED[10:3]								0x0008	RW
		[7:0]	RESERVED[2:0]			SCLK_SCL_M_ PULL	SCLK_SCL_M_SLEW			SCLK_SCL_M_DRIVE		

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0xF79E	MISO_SDA_M_PIN	[15:8]	RESERVED[10:3]								0x0008	RW
		[7:0]	RESERVED[2:0]			MISO_SDA_M_PULL	MISO_SDA_M_SLEW		MISO_SDA_M_DRIVE			
0xF79F	SS_M_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			SS_M_PULL	SS_M_SLEW		SS_M_DRIVE			
0xF7A0	MOSI_M_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			MOSI_M_PULL	MOSI_M_SLEW		MOSI_M_DRIVE			
0xF7A1	MP6_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			MP6_PULL	MP6_SLEW		MP6_DRIVE			
0xF7A2	MP7_PIN	[15:8]	RESERVED[10:3]								0x0018	RW
		[7:0]	RESERVED[2:0]			MP7_PULL	MP7_SLEW		MP7_DRIVE			
0xF7A3	CLKOUT_PIN	[15:8]	RESERVED[10:3]								0x0008	RW
		[7:0]	RESERVED[2:0]			CLKOUT_PULL	CLKOUT_SLEW		CLKOUT_DRIVE			
0xF899	SECONDPAGE_ENABLE	[15:8]	RESERVED[14:7]								0x0000	RW
		[7:0]	RESERVED[6:0]							PAGE		
0xF890	SOFT_RESET	[15:8]	RESERVED[14:7]								0x0000	RW
		[7:0]	RESERVED[6:0]							SOFT_RESET		

Power Enable 1 Register

Address: 0xF051, Reset: 0x0000, Name: POWER_ENABLE1

For the purpose of power savings, this register allows the PDM microphone interfaces, S/PDIF interfaces, and auxiliary ADCs to be disabled when not in use. When these functional blocks are disabled, the current draw on the corresponding supply pins decreases.

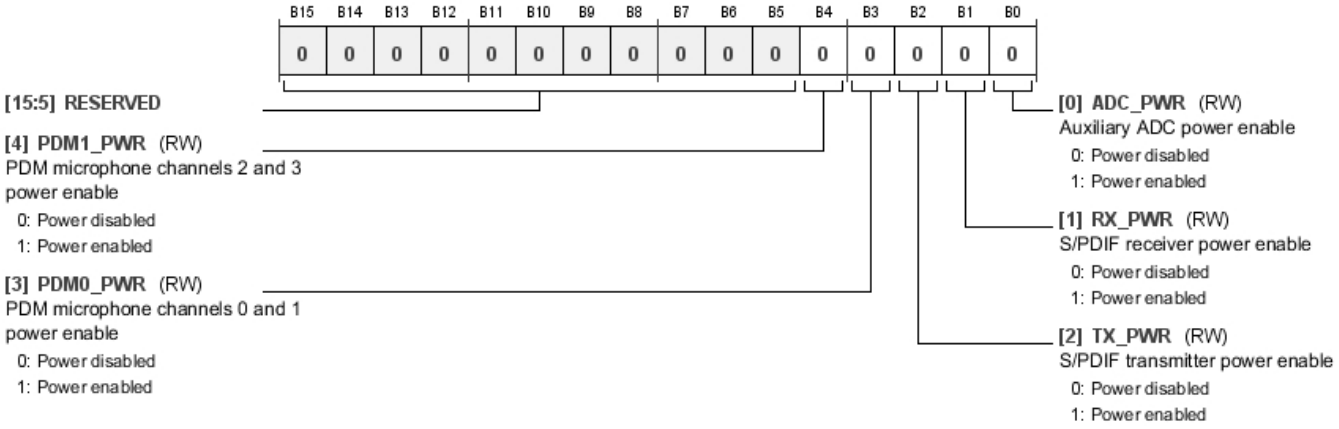


Table 75. Bit Descriptions for POWER_ENABLE1

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	PDM1_PWR		PDM Microphone Channel 2 and PDM Microphone Channel 3 power enable. When this bit is disabled, PDM Microphone Channel 2 and PDM Microphone Channel 3 and their associated circuitry are disabled, and their data values cease to update.	0x0	RW
		0	Power disabled		
		1	Power enabled		
3	PDM0_PWR		PDM Microphone Channel 0 and PDM Microphone Channel 1 power enable. When this bit is disabled, PDM Microphone Channel 0 and PDM Microphone Channel 1 and their associated circuitry are disabled, and their data values cease to update.	0x0	RW
		0	Power disabled		
		1	Power enabled		
2	TX_PWR		S/PDIF transmitter power enable. This bit disables the S/PDIF transmitter circuit. Clock and data ceases to output from the S/PDIF transmitter pin, and the output is held at logic low as long as this bit is disabled.	0x0	RW
		0	Power disabled		
		1	Power enabled		
1	RX_PWR		S/PDIF receiver power enable. This bit disables the S/PDIF receiver circuit. Clock and data recovery from the S/PDIF input stream ceases until this bit is reenabled.	0x0	RW
		0	Power disabled		
		1	Power enabled		
0	ADC_PWR		Auxiliary ADC power enable. When this bit is disabled, the auxiliary ADCs are powered down, their outputs cease to update, and they hold their last value.	0x0	RW
		0	Power disabled		
		1	Power enabled		

Table 80. Bit Descriptions for SERIAL_BYTE_x_0

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	LRCLK_SRC		LRCLK pin selection. These bits configure whether the corresponding serial port is a frame clock master or slave. When configured as a master, the corresponding LRCLK pin (LRCLK_INx for SDATA_INx pins and LRCLK_OUTx for SDATA_OUTx pins) with the same number as the serial port (for example, LRCLK_OUT0 for SDATA_OUT0) actively drives out a clock signal. When configured as a slave, the serial port can receive its clock signal from any of the four corresponding LRCLK pins (LRCLK_INx pins for SDATA_INx pins or LRCLK_OUTx pins for SDATA_OUTx pins).	0x0	RW
		000	Slave from LRCLK_IN0 or LRCLK_OUT0		
		001	Slave from LRCLK_IN1 or LRCLK_OUT1		
		010	Slave from LRCLK_IN2 or LRCLK_OUT2		
		011	Slave from LRCLK_IN3 or LRCLK_OUT3		
		100	Master mode; corresponding LRCLK pin actively outputs a clock signal		
[12:10]	BCLK_SRC		BCLK pin selection. These bits configure whether the corresponding serial port is a bit clock master or slave. When configured as a master, the corresponding BCLK pin (BCLK_INx for SDATA_INx pins and BCLK_OUTx for SDATA_OUTx pins) with the same number as the serial port (for example, BCLK_OUT0 for SDATA_OUT0) actively drives out a clock signal. When configured as a slave, the serial port can receive its clock signal from any of the four corresponding BCLK pins (BCLK_INx pins for SDATA_INx pins or BCLK_OUTx pins for SDATA_OUTx pins).	0x0	RW
		000	Slave from BCLK_IN0 or BCLK_OUT0		
		001	Slave from BCLK_IN1 or BCLK_OUT1		
		010	Slave from BCLK_IN2 or BCLK_OUT2		
		011	Slave from BCLK_IN3 or BCLK_OUT3		
		100	Master mode; corresponding BCLK pin actively outputs a clock signal		
9	LRCLK_MODE		LRCLK waveform type. The frame clock can be a 50/50 duty cycle square wave or a short pulse.	0x0	RW
		0	50% duty cycle clock (square wave)		
		1	Pulse with a width equal to one bit clock cycle		
8	LRCLK_POL		LRCLK polarity. This bit sets the frame clock polarity on the corresponding serial port. Negative polarity means that the frame starts on the falling edge of the frame clock. This conforms to the I²S standard audio format.	0x0	RW
		0	Negative polarity; frame starts on falling edge of frame clock		
		1	Positive polarity; frame starts on rising edge of frame clock		
7	BCLK_POL		BCLK polarity. This bit sets the bit clock polarity on the corresponding serial port. Negative polarity means that the data signal transitions on the falling edge of the bit clock. This conforms to the I²S standard audio format.	0x0	RW
		0	Negative polarity; data transitions on falling edge of bit clock		
		1	Positive polarity; data transitions on rising edge of bit clock		
[6:5]	WORD_LEN		Audio data-word length. These bits set the word length of the audio data channels on the corresponding serial port. For serial input ports, if the input data has more words than the length as configured by these bits, the extra data bits are ignored. For output serial ports, if the word length, as configured by these bits, is shorter than the data length coming from the data source (the DSP, ASRCs, S/PDIF receiver, PDM inputs, or serial inputs), the extra data bits are truncated and output as 0s. If Bits[6:5] (WORD_LEN) are set to 0b10 for 32-bit mode, the corresponding 32-bit input or output cells are required in SigmaStudio.	0x0	RW
		00	24 bits		
		01	16 bits		
		10	32 bits		
		11	Flexible TDM mode (configure using Register 0xF300 to Register 0xF33F, FTDM_INx, and Register 0xF380 to Register 0xF3BF, FTDM_OUTx)		

Panic Parity Register

Address: 0xF422, Reset: 0x0003, Name: PANIC_PARITY_MASK

The panic manager checks and reports memory parity mask errors. Register 0xF422 (PANIC_PARITY_MASK) allows the user to configure which memories, if any, are subject to error reporting.

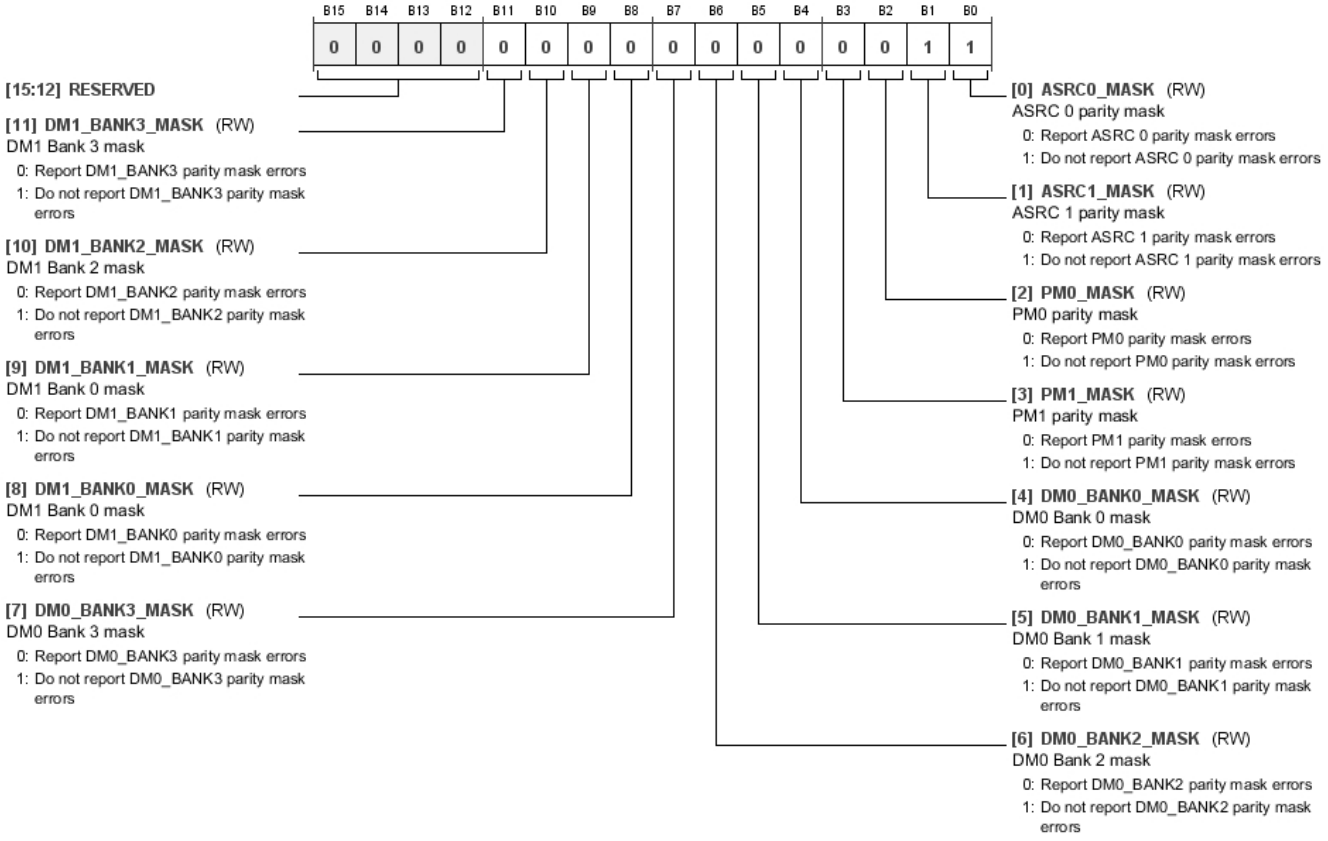


Table 91. Bit Descriptions for PANIC_PARITY_MASK

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x0	RW
11	DM1_BANK3_MASK		DM1 Bank 3 mask.	0x0	RW
		0	Report DM1_BANK3 parity mask errors		
		1	Do not report DM1_BANK3 parity mask errors		
10	DM1_BANK2_MASK		DM1 Bank 2 mask.	0x0	RW
		0	Report DM1_BANK2 parity mask errors		
		1	Do not report DM1_BANK2 parity mask errors		
9	DM1_BANK1_MASK		DM1 Bank 1 mask.	0x0	RW
		0	Report DM1_BANK1 parity mask errors		
		1	Do not report DM1_BANK1 parity mask errors		
8	DM1_BANK0_MASK		DM1 Bank 0 mask.	0x0	RW
		0	Report DM1_BANK0 parity mask errors		
		1	Do not report DM1_BANK0 parity mask errors		
7	DM0_BANK3_MASK		DM0 Bank 3 mask.	0x0	RW
		0	Report DM0_BANK3 parity mask errors		
		1	Do not report DM0_BANK3 parity mask errors		
6	DM0_BANK2_MASK		DM0 Bank 2 mask.	0x0	RW
		0	Report DM0_BANK2 parity mask errors		
		1	Do not report DM0_BANK2 parity mask errors		

SOFTWARE PANIC VALUE 0 REGISTER

Address: 0xF433, Reset: 0x0000, Name: SOFTWARE_VALUE_0

When a software error occurs, this register the lower 16 bits of the instruction at the time when the error occurred for software debugging purposes.

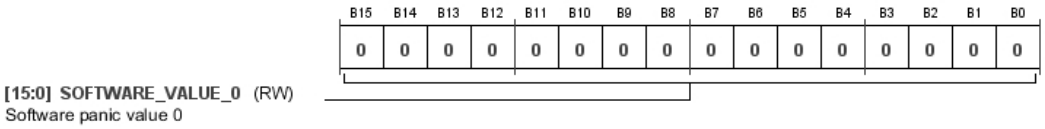


Table 99. Bit Descriptions for SOFTWARE_VALUE_0

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SOFTWARE_VALUE_0		Software panic value 0.	0x0000	RW

SOFTWARE PANIC VALUE 1 REGISTER

Address: 0xF434, Reset: 0x0000, Name: SOFTWARE_VALUE_1

When a software error occurs, this register the upper 16 bits of the instruction at the time when the error occurred for software debugging purposes.

Table 100. Bit Descriptions for SOFTWARE_VALUE_1

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SOFTWARE_VALUE_1		Software panic value 1.	0x0000	RW

DSP PROGRAM EXECUTION REGISTERS

Enable Block Interrupts Register

Address: 0xF450, Reset: 0x0000, Name: BLOCKINT_EN

This register enables block interrupts, which are necessary when frequency domain processing is required in the audio processing program. If block processing algorithms are used in SigmaStudio, SigmaStudio automatically sets this register accordingly. The user does not need to manually change the value of this register after SigmaStudio has configured it.

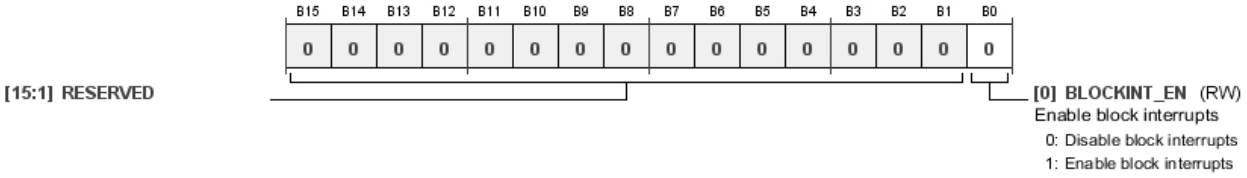


Table 103. Bit Descriptions for BLOCKINT_EN

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	BLOCKINT_EN		Enable block interrupts.	0x0	RW
		0	Disable block interrupts		
		1	Enable block interrupts		

Value for the Block Interrupt Counter Register

Address: 0xF451, Reset: 0x0000, Name: BLOCKINT_VALUE

This 16-bit register controls the duration in audio frames of a block. A counter increments each time a new frame start pulse is received by the DSP core. When the counter reaches the value determined by this register, a block interrupt is generated and the counter is reset. If block processing algorithms are used in SigmaStudio, SigmaStudio automatically sets this register accordingly. The user does not need to manually change the value of this register after SigmaStudio has configured it.

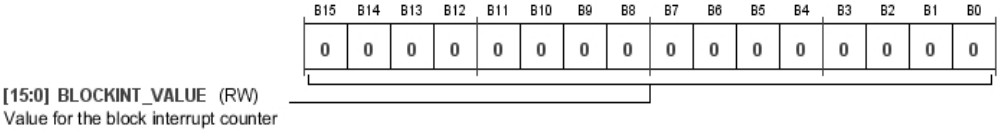


Table 104. Bit Descriptions for BLOCKINT_VALUE

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	BLOCKINT_VALUE		Value for the block interrupt counter.	0x0000	RW

Program Counter, Bits[23:16] Register

Address: 0xF460, Reset: 0x0000, Name: PROG_CNTR0

This register, in combination with Register 0xF461 (PROG_CNTR1), stores the current value of the program counter.

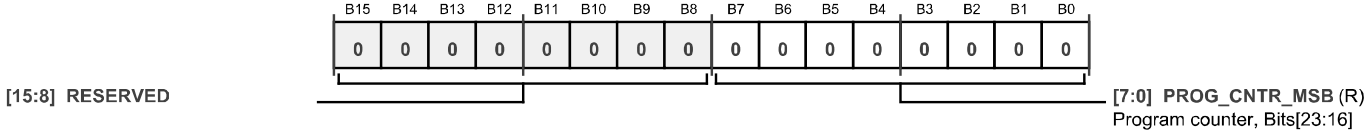


Table 105. Bit Descriptions for PROG_CNTR0

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x0	RW
[7:0]	PROG_CNTR_MSB		Program counter, Bits[23:16].	0x00	R

Program Counter Length, Bits[15:0] Register

Address: 0xF464, Reset: 0x0000, Name: PROG_CNTR_LENGTH1

This register, in combination with Register 0xF463 (PROG_CNTR_LENGTH0), keeps track of the peak value reached by the program counter during the last audio frame or block. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

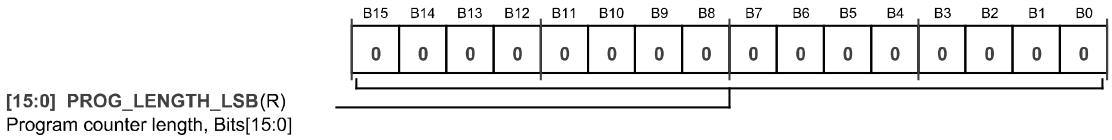


Table 109. Bit Descriptions for PROG_CNTR_LENGTH1

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PROG_LENGTH_LSB		Program counter length, Bits[15:0]	0x0000	R

Program Counter Maximum Length, Bits[23:16] Register

Address: 0xF465, Reset: 0x0000, Name: PROG_CNTR_MAXLENGTH0

This register, in combination with Register 0xF466 (PROG_CNTR_MAXLENGTH1), keeps track of the highest peak value reached by the program counter since the DSP core started. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

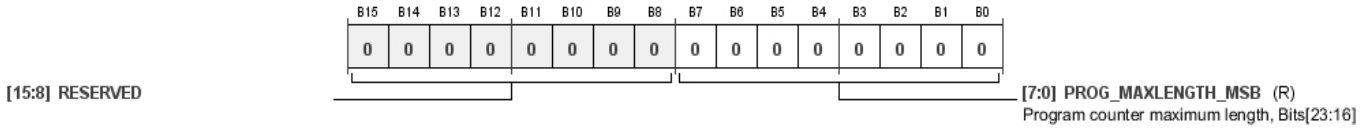


Table 110. Bit Descriptions for PROG_CNTR_MAXLENGTH0

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x0	RW
[7:0]	PROG_MAXLENGTH_MSB		Program counter maximum length, Bits[23:16]	0x00	R

Program Counter Maximum Length, Bits[15:0] Register

Address: 0xF466, Reset: 0x0000, Name: PROG_CNTR_MAXLENGTH1

This register, in combination with Register 0xF465 (PROG_CNTR_MAXLENGTH0), keeps track of the highest peak value reached by the program counter since the DSP core started. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

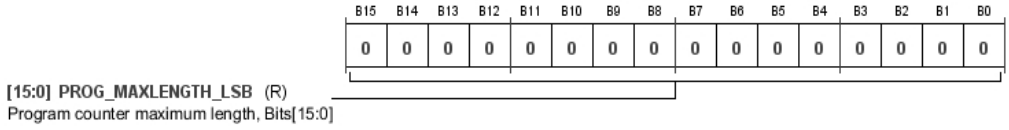


Table 111. Bit Descriptions for PROG_CNTR_MAXLENGTH1

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PROG_MAXLENGTH_LSB		Program counter maximum length, Bits[15:0]	0x0000	R

PANIC MASK REGISTERS

Panic Mask Parity DM0 Bank [1:0] Register

Address: 0xF467, Reset: 0x0000, Name: PANIC_PARITY_MASK1

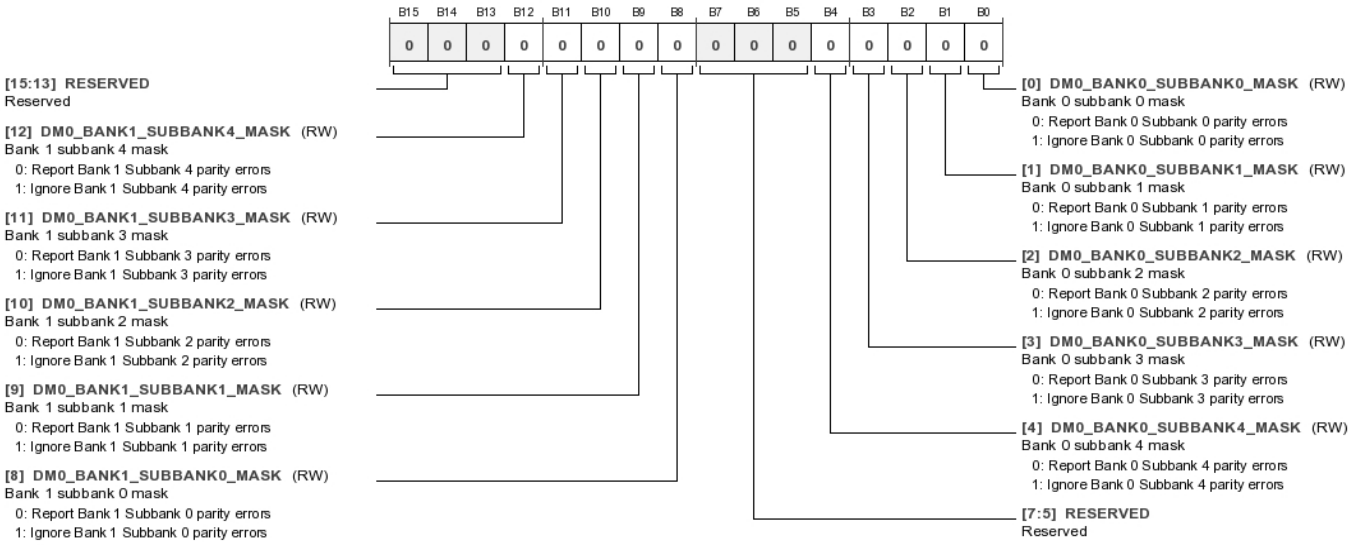


Table 112. Bit Descriptions for PANIC_PARITY_MASK1

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		Reserved.	0x0	RW
12	DM0_BANK1_SUBBANK4_MASK		Bank 1 Subbank 4 mask.	0x0	RW
		0	Report Bank 1 Subbank 4 parity errors		
		1	Ignore Bank 1 Subbank 4 parity errors		
11	DM0_BANK1_SUBBANK3_MASK		Bank 1 Subbank 3 mask.	0x0	RW
		0	Report Bank 1 Subbank 3 parity errors		
		1	Ignore Bank 1 Subbank 3 parity errors		
10	DM0_BANK1_SUBBANK2_MASK		Bank 1 Subbank 2 mask.	0x0	RW
		0	Report Bank 1 Subbank 2 parity errors		
		1	Ignore Bank 1 Subbank 2 parity errors		
9	DM0_BANK1_SUBBANK1_MASK		Bank 1 Subbank 1 mask.	0x0	RW
		0	Report Bank 1 Subbank 1 parity errors		
		1	Ignore Bank 1 Subbank 1 parity errors		
8	DM0_BANK1_SUBBANK0_MASK		Bank 1 Subbank 0 mask.	0x0	RW
		0	Report Bank 1 Subbank 0 parity errors		
		1	Ignore Bank 1 Subbank 0 parity errors		
[7:5]	RESERVED		Reserved.	0x0	RW
4	DM0_BANK0_SUBBANK4_MASK		Bank 0 Subbank 4 mask.	0x0	RW
		0	Report Bank 0 Subbank 4 parity errors		
		1	Ignore Bank 0 Subbank 4 parity errors		
3	DM0_BANK0_SUBBANK3_MASK		Bank 0 Subbank 3 mask.	0x0	RW
		0	Report Bank 0 Subbank 3 parity errors		
		1	Ignore Bank 0 Subbank 3 parity errors		
2	DM0_BANK0_SUBBANK2_MASK		Bank 0 Subbank 2 mask.	0x0	RW
		0	Report Bank 0 Subbank 2 parity errors		
		1	Ignore Bank 0 Subbank 2 parity errors		
1	DM0_BANK0_SUBBANK1_MASK		Bank 0 Subbank 1 mask.	0x0	RW
		0	Report Bank 0 Subbank 1 parity errors		
		1	Ignore Bank 0 Subbank 1 parity errors		

Decoded Signals From the S/PDIF Receiver Register

Address: 0xF602, Reset: 0x0000, Name: SPDIF_RX_DECODE

This register monitors the embedded nonaudio data bits in the incoming S/PDIF stream on the ADAU1466 and ADAU1462 and decodes them, providing insight into the data format of the S/PDIF input stream.

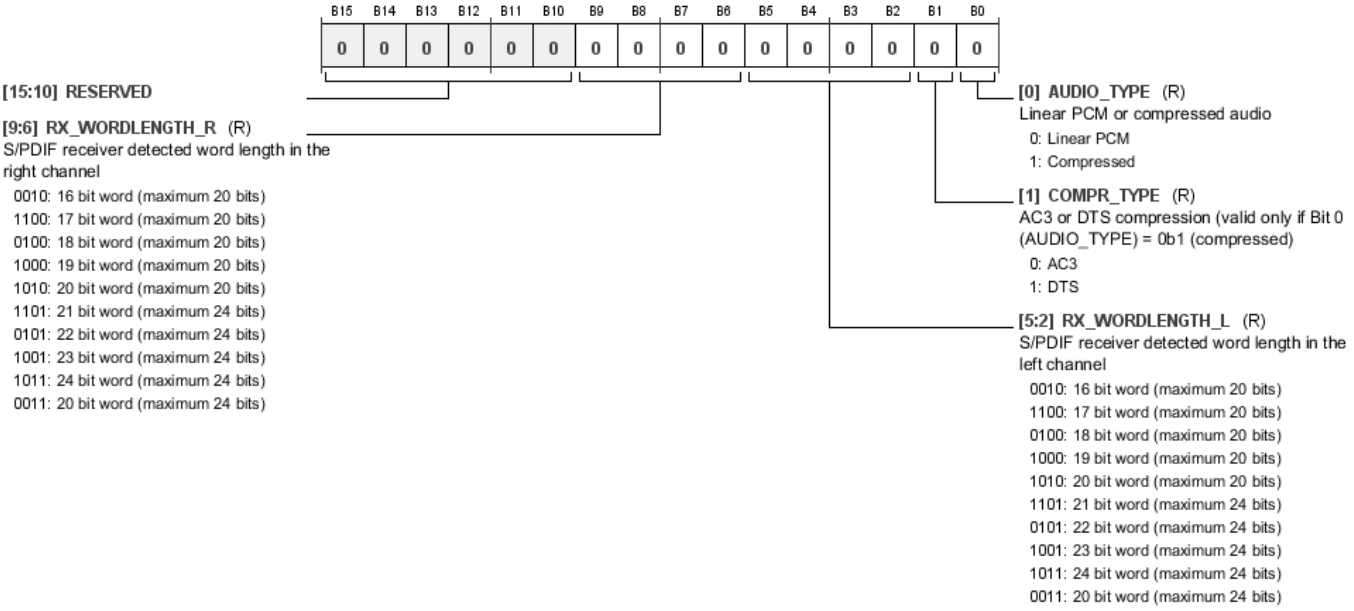


Table 134. Bit Descriptions for SPDIF_RX_DECODE

Bits	Bit Name	Settings	Description	Reset	Access
[15:10]	RESERVED			0x0	RW
[9:6]	RX_WORDLENGTH_R		S/PDIF receiver detected word length in the right channel.	0x0	R
		0010	16 bit word (maximum 20 bits)		
		1100	17 bit word (maximum 20 bits)		
		0100	18 bit word (maximum 20 bits)		
		1000	19 bit word (maximum 20 bits)		
		1010	20 bit word (maximum 20 bits)		
		1101	21 bit word (maximum 24 bits)		
		0101	22 bit word (maximum 24 bits)		
		1001	23 bit word (maximum 24 bits)		
		1011	24 bit word (maximum 24 bits)		
		0011	20 bit word (maximum 24 bits)		
[5:2]	RX_WORDLENGTH_L		S/PDIF receiver detected word length in the left channel.	0x0	R
		0010	16 bit word (maximum 20 bits)		
		1100	17 bit word (maximum 20 bits)		
		0100	18 bit word (maximum 20 bits)		
		1000	19 bit word (maximum 20 bits)		
		1010	20 bit word (maximum 20 bits)		
		1101	21 bit word (maximum 24 bits)		
		0101	22 bit word (maximum 24 bits)		
		1001	23 bit word (maximum 24 bits)		
		1011	24 bit word (maximum 24 bits)		
		0011	20 bit word (maximum 24 bits)		
1	COMPR_TYPE		AC3 or DTS compression (valid only if Bit 0 (AUDIO_TYPE) = 0b1 (compressed).	0x0	R
		0	AC3		
		1	DTS		

SS/ADDR0 Pin Drive Strength and Slew Rate Register

Address: 0xF79B, Reset: 0x0018, Name: SS_PIN

This register configures the drive strength, slew rate, and pull resistors for the SS/ADDR0 pin.

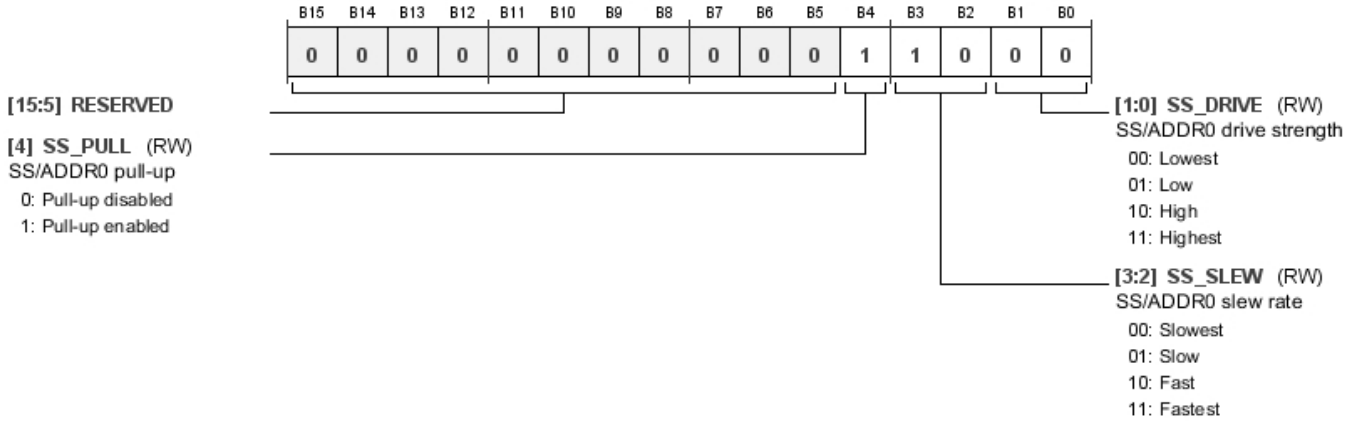


Table 168. Bit Descriptions for SS_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	SS_PULL		SS/ADDR0 pull-up.	0x1	RW
		0	Pull-up disabled		
		1	Pull-up enabled		
[3:2]	SS_SLEW		SS/ADDR0 slew rate.	0x2	RW
		00	Slowest		
		01	Slow		
		10	Fast		
		11	Fastest		
[1:0]	SS_DRIVE		SS/ADDR0 drive strength.	0x0	RW
		00	Lowest		
		01	Low		
		10	High		
		11	Highest		

SS_M/MP0 Pin Drive Strength and Slew Rate Register

Address: 0xF79F, Reset: 0x0018, Name: SS_M_PIN

This register configures the drive strength, slew rate, and pull resistors for the SS_M/MP0 pin.

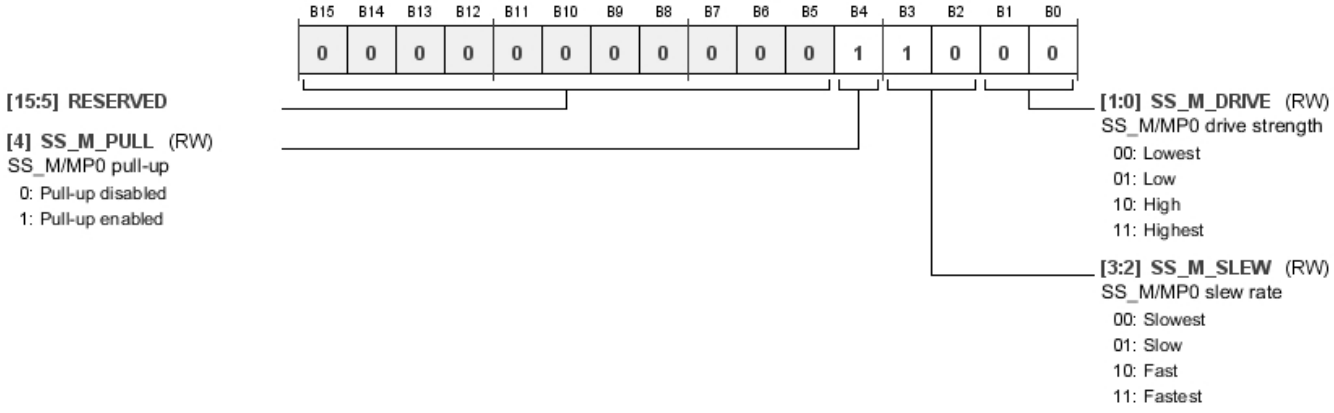


Table 172. Bit Descriptions for SS_M_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	SS_M_PULL		SS_M/MP0 pull-up.	0x1	RW
		0	Pull-up disabled		
		1	Pull-up enabled		
[3:2]	SS_M_SLEW		SS_M/MP0 slew rate.	0x2	RW
		00	Slowest		
		01	Slow		
		10	Fast		
		11	Fastest		
[1:0]	SS_M_DRIVE		SS_M/MP0 drive strength.	0x0	RW
		00	Lowest		
		01	Low		
		10	High		
		11	Highest		