Renesas Electronics America Inc - R8A77430HA01BG#UA Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A15
Number of Cores/Bus Width	-
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77430ha01bg-ua

1.3 List of Specifications

1.3.1 ARM Core

Item	Description
System CPU Cortex-A15	• ARM Cortex-A15 Dual MPCore 1.5 GHz • L1 I/D cache 32/32 Kbytes, L2 cache 1 Mbyte • NEON™/VFPv4 supported • Security extension supported
ARM debugger (CoreSight)	• CoreSight system compliant • JTAG/SWD I/F supported • CoreSight PTM-A15 supported (each CPU) • CoreSight ETR 16 Kbytes for program flow trace • CoreSight ETR 4 Kbytes for system trace

DBSC3 channel 1 (No.154 to 173): 3-Function Multiplexed

These pins function and pin states during power-on reset depend on MD28, MD 27 and MD22 pins setting, and cannot be changed after power-on reset by software.

	Function 1	Function 2	Function 3	
	MD28=1, MD27=1, MD22=1	MD28=0, MD27=1, MD22=1	MD28=1,MD27=1,MD22=0	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
154	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D15	M1DQ14	M0DQ46	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
155	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A15	M1DQ15	M0DQ47	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
156	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E14	M1DQS1	M0DQS5	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
157	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E13	M1DQS1#	M0DQS5#	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
158	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C13	M1DM1	M0DM5	-	1.35V/-
	O(Z)	O(Z)	Z	-
159	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
F13	VDDQ_M1DPLL1	VDDQ_M0DPLL5	VDDQ_M0DPLL5	-
	P	P	P	-
160	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
F12	VSSQ_M1DPLL1	VSSQ_M0DPLL5	VSSQ_M0DPLL5	-
	P	P	P	-
161	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B6	M1DQ16	M0DQ48	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
162	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A7	M1DQ17	M0DQ49	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
163	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C8	M1DQ18	M0DQ50	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
164	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B8	M1DQ19	M0DQ51	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
165	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D8	M1DQ20	M0DQ52	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
166	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A8	M1DQ21	M0DQ53	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
167	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D6	M1DQ22	M0DQ54	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
168	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B9	M1DQ23	M0DQ55	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
169	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E8	M1DQS2	M0DQS6	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
170	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E9	M1DQS2#	M0DQS6#	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
171	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C7	M1DM2	M0DM6	-	1.35V/-
	O(Z)	O(Z)	Z	-
172	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
F10	VDDQ_M1DPLL2	VDDQ_M0DPLL6	VDDQ_M0DPLL6	-
	P	P	P	-
173	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
F9	VSSQ_M1DPLL2	VSSQ_M0DPLL6	VSSQ_M0DPLL6	-
	P	P	P	-

4/5 (DBSC3 channel 1)

Note: * Reserved pins in function 3 should be opened.

MSIOF, SCIF, VIN, MMC, I2C, IIC, RCAN, DU, ADG, PWM, SCIFA, HSCIF, SCIFB, TMU and GPIO (No.515 to 533): Up to 8-Function Multiplexed and Mode Pins assigned (No.521, 522)

These pins are set for GPIO except for No.527 to 530 (I2C5 and IIC3 pins) after power-on reset. For details, refer to GPSR4, GPSR6 and GPSR7 registers in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
Mode Pin	I/O								Pull-up
515	MSIOF0	SCIF2	Reserved	Reserved	VIN1	VIN1	-		I(GPIO)
T31	MSIOF0_SCK	RX2_C	-	-	VI1_CLK_C	VI1_G0_B	-	GP6_24	3.3V/8mA
	IO	I	-	-	I	I	-	IO(I)	On
516	MSIOF0	SCIF2	Reserved	Reserved	VIN1	VIN1	-		I(GPIO)
T30	MSIOF0_SYNC	TX2_C	-	-	VI1_CLKENB_C	VI1_G1_B	-	GP6_25	3.3V/4mA
	IO	O	-	-	I	I	-	IO(I)	On
517	MSIOF0	Reserved	Reserved	VIN1	VIN1	-	-		I(GPIO)
T29	MSIOF0_TXD	-	-	VI1_FIELD_C	VI1_G2_B	-	-	GP6_26	3.3V/4mA
	O	-	-	I	I	-	-	IO(I)	On
518	MSIOF0	Reserved	Reserved	VIN1	VIN1	-	-		I(GPIO)
T28	MSIOF0_RXD	-	-	VI1_DATA0_C	VI1_G3_B	-	-	GP6_27	3.3V/4mA
	I	-	-	I	I	-	-	IO(I)	On
519	MSIOF0	MMC	Reserved	SCIF0	VIN1	I2C7(IIC0)	VIN1		I(GPIO)
T27	MSIOF0_SS1	MMC_D6	-	TX0_E	VI1_HSYNC#_C	IIC0_SCL_C	VI1_G4_B	GP6_28	3.3V/8mA
	O	IO	-	O	I	IO	I	IO(I)	On
520	MSIOF0	MMC	Reserved	SCIF0	VIN1	I2C7(IIC0)	VIN1		I(GPIO)
T26	MSIOF0_SS2	MMC_D7	-	RX0_E	VI1_VSYNC#_C	IIC0_SDA_C	VI1_G5_B	GP6_29	3.3V/8mA
	O	IO	-	I	I	IO	I	IO(I)	On
521	Reserved	Reserved	RCAN1	-	-	-	-		I(Mode Pin)
R26	-	-	CAN1_TX_D	-	-	-	-	GP4_29	3.3V/4mA
MDT1	-	-	O	-	-	-	-	IO(I)	Off
522	Reserved	Reserved	RCAN	-	-	-	-		I(Mode Pin)
R28	-	-	CAN_CLK_C	-	-	-	-	GP4_30	3.3V/4mA
MDT0	-	-	I	-	-	-	-	IO(I)	Off
523	Reserved	Reserved	RCAN1	-	-	-	-		I(GPIO)
R27	-	-	CAN1_RX_D	-	-	-	-	GP4_31	3.3V/4mA
	-	-	I	-	-	-	-	IO(I)	On
524	Reserved	DU1	ADG	PWM5	SCIFA3	-	-		I(GPIO)
R31	-	DU1_DOTCLKIN_C	AUDIO_CLKB_B	PWM5_B	SCIFA3_TXD_C	-	-	GP7_20	3.3V/4mA
	-	I	I	O	O	-	-	IO(I)	On
525	Reserved	SCIF4	SCIFA4	PWM5	VIN1	SCIFA3	-		I(GPIO)
R30	-	TX4_C	SCIFA4_TXD_C	PWM5	VI1_G6_B	SCIFA3_RXD_C	-	GP7_21	3.3V/4mA
	-	O	O	O	I	I	-	IO(I)	On
526	Reserved	SCIF4	SCIFA4	PWM6	VIN1	SCIFA3	-		I(GPIO)
R29	-	RX4_C	SCIFA4_RXD_C	PWM6	VI1_G7_B	SCIFA3_SCK_C	-	GP7_22	3.3V/4mA
	-	I	I	O	I	O	-	IO(I)	On
527	I2C5_OD	-	-	-	-	-	-		Z
AJ18	I2C5_SCL	-	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	-	-	-	-	-	-	-	-
528	I2C5_OD	-	-	-	-	-	-		Z
AH18	I2C5_SDA	-	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	-	-	-	-	-	-	-	-
529	IIC3(I2C6 DVFS)	-	-	-	-	-	-		Z
AJ19	IIC3_SCL	-	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	-	-	-	-	-	-	-	-
530	IIC3(I2C6 DVFS)	-	-	-	-	-	-		Z
AH19	IIC3_SDA	-	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	-	-	-	-	-	-	-	-
531	HSCIF0	SCIFB0	Reserved	Reserved	TMU	VIN1	-		I(GPIO)
P28	HCTS0#	SCIFB0_CTS#	-	-	TCLK1	VI1_DATA1_C	-	GP7_0	3.3V/8mA
	IO	I	-	-	I	I	-	IO(I)	On
532	HSCIF0	SCIFB0	Reserved	Reserved	VIN1	-	-		I(GPIO)
R25	HRTS0#	SCIFB0_RTS#	-	-	VI1_DATA2_C	-	-	GP7_1	3.3V/8mA
	IO	O	-	-	I	-	-	IO(I)	On
533	HSCIF0	SCIFB0	Reserved	Reserved	RCAN	TMU	VIN1		I(GPIO)
P31	HSCK0	SCIFB0_SCK	-	-	CAN_CLK	TCLK2	VI1_DATA3_C	GP7_2	3.3V/8mA
	IO	O	-	-	I	I	I	IO(I)	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
385	AL16	NMI	I	I	NMI	I	-
386	AE30	IRQ0	IO	I	GP7_10	I	On
387	AE29	IRQ1	IO	I	GP7_11	I	On
388	AD29	IRQ2	IO	I	GP7_12	I	On
389	AD28	IRQ3	IO	I	GP7_13	I	On
390	AC29	IRQ4	IO	I	GP7_14	I	On
391	AC28	IRQ5	IO	I	GP7_15	I	On
392	AC27	IRQ6	IO	I	GP7_16	I	On
393	AB26	IRQ7	IO	I	GP7_17	I	On
394	AB27	IRQ8	IO	I	GP7_18	I	On
395	AB28	IRQ9	IO	I	GP7_19	I	On
396	AL12	DU1_DR0	IO	I	GP3_0	I	On
397	AK12	DU1_DR1	IO	I	GP3_1	I	On
398	AJ12	DU1_DR2	IO	I	GP3_2	I	On
399	AH12	DU1_DR3	IO	I	GP3_3	I	On
400	AG12	DU1_DR4	IO	I	GP3_4	I	On
401	AF12	DU1_DR5	IO	I	GP3_5	I	On
402	AE12	DU1_DR6	IO	I	GP3_6	I	On
403	AE11	DU1_DR7	IO	I	GP3_7	I	On
404	AL11	DU1_DG0	IO	I	GP3_8	I	On
405	AK11	DU1_DG1	IO	I	GP3_9	I	On
406	AJ11	DU1_DG2	IO	I	GP3_10	I	On
407	AH11	DU1_DG3	IO	I	GP3_11	I	On
408	AG11	DU1_DG4	IO	I	GP3_12	I	On
409	AF11	DU1_DG5	IO	I	GP3_13	I	On
410	AF10	DU1_DG6	IO	I	GP3_14	I	On
411	AE10	DU1_DG7	IO	I	GP3_15	I	On
412	AJ9	DU1_DB0	IO	I	GP3_16	I	On
413	AH9	DU1_DB1	IO	I	GP3_17	I	On
414	AG9	DU1_DB2	IO	I	GP3_18	I	On
415	AF9	DU1_DB3	IO	I	GP3_19	I	On
416	AE9	DU1_DB4	IO	I	GP3_20	I	On
417	AJ10	DU1_DB5	IO	I(MD11)	GP3_21	I	Off
418	AH10	DU1_DB6	IO	I	GP3_22	I	On
419	AG10	DU1_DB7	IO	I	GP3_23	I	On
420	AL9	DU1_DOTCLKIN	IO	I	GP3_24	I	On
421	AL10	DU1_DOTCLKOUT0	IO	I	GP3_25	I	On
422	AK10	DU1_DOTCLKOUT1	IO	I	GP3_26	I	On
423	AE8	DU1_EXHSYNC/DU1_HSYNC	IO	I(MD3)	GP3_27	I	Off
424	AF8	DU1_EXVSYNC/DU1_VSYNC	IO	I(MD2)	GP3_28	I	Off
425	AG8	DU1_EXODDF/DU1_ODDF/DISP/CDE	IO	I	GP3_29	I	On

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
43	B27	M0DQ4	Z	-	-	-	Open
44	B29	M0DQ5	Z	-	-	-	Open
45	C27	M0DQ6	Z	-	-	-	Open
46	A30	M0DQ7	Z	-	-	-	Open
47	E26	M0DQS0	Z	-	-	-	Open
48	E25	M0DQS0#	Z	-	-	-	Open
49	A28	M0DM0	Z	-	-	-	Open
50	G22	VDDQ_M0DPLL0	P	-	-	-	Must be used
51	G23	VSSQ_M0DPLL0	P	-	-	-	Must be used
52	G24	M0VREFDQ0	P	-	-	-	Must be used
53	B23	M0DQ8	Z	-	-	-	Open
54	A24	M0DQ9	Z	-	-	-	Open
55	C24	M0DQ10	Z	-	-	-	Open
56	D24	M0DQ11	Z	-	-	-	Open
57	B26	M0DQ12	Z	-	-	-	Open
58	D26	M0DQ13	Z	-	-	-	Open
59	B24	M0DQ14	Z	-	-	-	Open
60	A25	M0DQ15	Z	-	-	-	Open
61	E23	M0DQS1	Z	-	-	-	Open
62	E24	M0DQS1#	Z	-	-	-	Open
63	C25	M0DM1	Z	-	-	-	Open
64	F22	VDDQ_M0DPLL1	P	-	-	-	Must be used
65	F23	VSSQ_M0DPLL1	P	-	-	-	Must be used
66	E31	M0DQ16	Z	-	-	-	Open
67	C30	M0DQ17	Z	-	-	-	Open
68	E29	M0DQ18	Z	-	-	-	Open
69	B31	M0DQ19	Z	-	-	-	Open
70	E30	M0DQ20	Z	-	-	-	Open
71	C31	M0DQ21	Z	-	-	-	Open
72	E28	M0DQ22	Z	-	-	-	Open
73	D29	M0DQ23	Z	-	-	-	Open
74	F27	M0DQS2	Z	-	-	-	Open
75	G27	M0DQS2#	Z	-	-	-	Open
76	D31	M0DM2	Z	-	-	-	Open
77	K25	VDDQ_M0DPLL2	P	-	-	-	Must be used
78	J25	VSSQ_M0DPLL2	P	-	-	-	Must be used
79	H25	M0VREFDQ1	P	-	-	-	Must be used
80	F28	M0DQ24	Z	-	-	-	Open
81	G31	M0DQ25	Z	-	-	-	Open
82	F30	M0DQ26	Z	-	-	-	Open
83	H30	M0DQ27	Z	-	-	-	Open
84	H28	M0DQ28	Z	-	-	-	Open
85	J30	M0DQ29	Z	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
214	AL24	RIDN1_SATA	I	-	-	-	Open
215	AL25	TODP1_SATA	O	-	-	-	Open
216	AL26	TODN1_SATA	O	-	-	-	Open
217	AJ26	CICREFP1_SATA	I	-	-	-	Fixed to VSS_SATA1
218	AJ25	CICREFN1_SATA	I	-	-	-	Fixed to VSS_SATA1
219	AE23	VSS_SATA1	P	-	-	-	Must be used
220	AF24	VDDA_SATA1	P	-	-	-	Must be used
221	AG24	VDDA_SATA1	P	-	-	-	Must be used
222	AF23	VDDD_SATA1	P	-	-	-	Must be used
223	AG23	VDDD_SATA1	P	-	-	-	Must be used
224	AH24	VDDD_SATA1	P	-	-	-	Must be used
225	AD23	VSS_SATA1	P	-	-	-	Must be used
226	AE24	VSS_SATA1	P	-	-	-	Must be used
227	AJ24	VSS_SATA1	P	-	-	-	Must be used
228	AK24	VSS_SATA1	P	-	-	-	Must be used
229	AK25	VSS_SATA1	P	-	-	-	Must be used
230	AK26	VSS_SATA1	P	-	-	-	Must be used
231	AK23	VSS_SATA1	P	-	-	-	Must be used
232	AL27	RIDP0_SATA	I	-	-	-	Open
233	AL28	RIDN0_SATA	I	-	-	-	Open
234	AL29	TODP0_SATA	O	-	-	-	Open
235	AL30	TODN0_SATA	O	-	-	-	Open
236	AJ28	CICREFP0_SATA	I	-	-	-	Fixed to VSS_SATA0
237	AJ27	CICREFN0_SATA	I	-	-	-	Fixed to VSS_SATA0
238	AF25	VSS_SATA0	P	-	-	-	Must be used
239	AG26	VDDA_SATA0	P	-	-	-	Must be used
240	AH27	VDDA_SATA0	P	-	-	-	Must be used
241	AH25	VDDD_SATA0	P	-	-	-	Must be used
242	AH26	VDDD_SATA0	P	-	-	-	Must be used
243	AG25	VDDD_SATA0	P	-	-	-	Must be used
244	AD24	VSS_SATA0	P	-	-	-	Must be used
245	AE25	VSS_SATA0	P	-	-	-	Must be used
246	AF26	VSS_SATA0	P	-	-	-	Must be used
247	AG27	VSS_SATA0	P	-	-	-	Must be used
248	AK27	VSS_SATA0	P	-	-	-	Must be used
249	AH28	VSS_SATA0	P	-	-	-	Must be used
250	AK28	VSS_SATA0	P	-	-	-	Must be used
251	AJ29	VSS_SATA0	P	-	-	-	Must be used
252	AK29	VSS_SATA0	P	-	-	-	Must be used
253	AK30	VSS_SATA0	P	-	-	-	Must be used
254	AL31	VSS_SATA0	P	-	-	-	Must be used
255	AL20	USB_EXTAL	I	-	-	-	Pulled-down to VSS
256	AL19	USB_XTAL	O	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
257	AG31	USB0_DP	I	-	-	-	Open
258	AH31	USB0_DM	I	-	-	-	Open
259	AG29	USB0_RREF	P	-	-	-	Must be used
260	AE27	VD331	P	-	-	-	Must be used
261	AD26	VD181	P	-	-	-	Must be used
262	AB24	AVDD	P	-	-	-	Must be used
263	AC24	AVSS	P	-	-	-	Must be used
264	AF31	USB0_PWEN	L	-	-	Off	Open
265	AF30	USB0_OVC/VBUS	I	-	-	On	Open
266	AJ31	USB1_DP	I	-	-	-	Open
267	AK31	USB1_DM	I	-	-	-	Open
268	AH29	USB1_RREF	P	-	-	-	Must be used
269	AF28	VD331	P	-	-	-	Must be used
270	AC25	AVDD	P	-	-	-	Must be used
271	AD25	AVSS	P	-	-	-	Must be used
272	AE26	AVSS	P	-	-	-	Must be used
273	AF27	AVSS	P	-	-	-	Must be used
274	AG28	AVSS	P	-	-	-	Must be used
275	AE28	USB1_PWEN	L	-	-	Off	Open
276	AD27	USB1_OVC	I	-	-	On	Open
277	AE20	DU0_LVDS_CLK_P	Z	-	-	-	Open
278	AF20	DU0_LVDS_CLK_N	Z	-	-	-	Open
279	AJ23	DU0_LVDS_CH0_P	Z	-	-	-	Open
280	AJ22	DU0_LVDS_CH0_N	Z	-	-	-	Open
281	AL21	DU0_LVDS_CH1_P	Z	-	-	-	Open
282	AL22	DU0_LVDS_CH1_N	Z	-	-	-	Open
283	AJ20	DU0_LVDS_CH2_P	Z	-	-	-	Open
284	AJ21	DU0_LVDS_CH2_N	Z	-	-	-	Open
285	AG22	DU0_LVDS_CH3_P	Z	-	-	-	Open
286	AG21	DU0_LVDS_CH3_N	Z	-	-	-	Open
287	AG17	DU0_DOTCLKIN	I	-	-	On	Open
288	AD22	VDDQ_LVDS	P	-	-	-	Must be used
289	AE22	VDDQ_LVDS	P	-	-	-	Must be used
290	AF22	VDDQ_LVDS	P	-	-	-	Must be used
291	AD20	DU0_LVDS_PLL1_VCC	P	-	-	-	Must be used
292	AD21	DU0_LVDS_PLL1_VSS	P	-	-	-	Must be used
293	AA7	D0	I	-	Area 0*1	On	Open
294	AA6	D1	I	-	Area 0*1	On	Open
295	AA5	D2	I	-	Area 0*1	On	Open
296	AA4	D3	I	-	Area 0*1	On	Open
297	AA3	D4	I	-	Area 0*1	On	Open
298	AA2	D5	I	-	Area 0*1	On	Open
299	AA1	D6	I	-	Area 0*1	On	Open

5.3.3 GPIO/Peripheral Function Select Register 1 (GPSR1)

Function: GPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP1 [31]	GP1 [30]	GP1 [29]	GP1 [28]	GP1 [27]	GP1 [26]	GP1 [25]	GP1 [24]	GP1 [23]	GP1 [22]	GP1 [21]	GP1 [20]	GP1 [19]	GP1 [18]	GP1 [17]	GP1 [16]
Initial value:	0	0	0	0	0	0	0	0	1/0	1/0	1/0	0	1/0	1/0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP1 [15]	GP1 [14]	GP1 [13]	GP1 [12]	GP1 [11]	GP1 [10]	GP1 [9]	GP1 [8]	GP1 [7]	GP1 [6]	GP1 [5]	GP1 [4]	GP1 [3]	GP1 [2]	GP1 [1]	GP1 [0]
Initial value:	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP1[31:0]	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000), or H'00EC 0FFF (in power-on reset)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[0]	GP-1-0	Peripheral function selected by IP1[25:23]
GP1[1]	GP-1-1	Peripheral function selected by IP1[28:26]
GP1[2]	GP-1-2	Peripheral function selected by IP1[31:29]
GP1[3]	GP-1-3	Peripheral function selected by IP2[2:0]
GP1[4]	GP-1-4	Peripheral function selected by IP2[4:3]
GP1[5]	GP-1-5	Peripheral function selected by IP2[6:5]
GP1[6]	GP-1-6	Peripheral function selected by IP2[9:7]
GP1[7]	GP-1-7	Peripheral function selected by IP2[12:10]
GP1[8]	GP-1-8	Peripheral function selected by IP2[15:13]
GP1[9]	GP-1-9	Peripheral function selected by IP2[18:16]
GP1[10]	GP-1-10	Peripheral function selected by IP2[20:19]
GP1[11]	GP-1-11	Peripheral function selected by IP2[22:21]
GP1[12]	GP-1-12	EX_CS0#
GP1[13]	GP-1-13	Peripheral function selected by IP2[24:23]
GP1[14]	GP-1-14	Peripheral function selected by IP2[26:25]
GP1[15]	GP-1-15	Peripheral function selected by IP2[29:27]
GP1[16]	GP-1-16	Peripheral function selected by IP3[2:0]
GP1[17]	GP-1-17	Peripheral function selected by IP3[5:3]
GP1[18]	GP-1-18	Peripheral function selected by IP3[8:6]
GP1[19]	GP-1-19	RD#
GP1[20]	GP-1-20	Peripheral function selected by IP3[11:9]

5.3.7 GPIO/Peripheral Function Select Register 5 (GPSR5)

Function: GPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP5 [31]	GP5 [30]	GP5 [29]	GP5 [28]	GP5 [27]	GP5 [26]	GP5 [25]	GP5 [24]	GP5 [23]	GP5 [22]	GP5 [21]	GP5 [20]	GP5 [19]	GP5 [18]	GP5 [17]	GP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP5 [15]	GP5 [14]	GP5 [13]	GP5 [12]	GP5 [11]	GP5 [10]	GP5 [9]	GP5 [8]	GP5 [7]	GP5 [6]	GP5 [5]	GP5 [4]	GP5 [3]	GP5 [2]	GP5 [1]	GP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP5[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[0]	GP-5-0	Peripheral function selected by IP11[11:9]
GP5[1]	GP-5-1	Peripheral function selected by IP11[14:12]
GP5[2]	GP-5-2	Peripheral function selected by IP11[16:15]
GP5[3]	GP-5-3	Peripheral function selected by IP11[18:17]
GP5[4]	GP-5-4	Peripheral function selected by IP11[19]
GP5[5]	GP-5-5	Peripheral function selected by IP11[20]
GP5[6]	GP-5-6	Peripheral function selected by IP11[21]
GP5[7]	GP-5-7	Peripheral function selected by IP11[22]
GP5[8]	GP-5-8	Peripheral function selected by IP11[23]
GP5[9]	GP-5-9	Peripheral function selected by IP11[24]
GP5[10]	GP-5-10	Peripheral function selected by IP11[25]
GP5[11]	GP-5-11	Peripheral function selected by IP11[26]
GP5[12]	GP-5-12	Peripheral function selected by IP11[27]
GP5[13]	GP-5-13	Peripheral function selected by IP11[29:28]
GP5[14]	GP-5-14	Peripheral function selected by IP11[31:30]
GP5[15]	GP-5-15	Peripheral function selected by IP12[1:0]
GP5[16]	GP-5-16	Peripheral function selected by IP12[3:2]
GP5[17]	GP-5-17	Peripheral function selected by IP12[6:4]
GP5[18]	GP-5-18	Peripheral function selected by IP12[9:7]
GP5[19]	GP-5-19	Peripheral function selected by IP12[12:10]
GP5[20]	GP-5-20	Peripheral function selected by IP12[15:13]
GP5[21]	GP-5-21	Peripheral function selected by IP12[17:16]
GP5[22]	GP-5-22	Peripheral function selected by IP12[19:18]
GP5[23]	GP-5-23	Peripheral function selected by IP12[21:20]
GP5[24]	GP-5-24	Peripheral function selected by IP12[23:22]

5.3.12 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP2 [29]	IP2 [28]	IP2 [27]	IP2 [26]	IP2 [25]	IP2 [24]	IP2 [23]	IP2 [22]	IP2 [21]	IP2 [20]	IP2 [19]	IP2 [18]	IP2 [17]	IP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP2 [15]	IP2 [14]	IP2 [13]	IP2 [12]	IP2 [11]	IP2 [10]	IP2 [9]	IP2 [8]	IP2 [7]	IP2 [6]	IP2 [5]	IP2 [4]	IP2 [3]	IP2 [2]	IP2 [1]	IP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP2[2:0]	A19	DACK1	SCIFA1_TXD_C	—	SCIFB1_TXD_C	—	SCIFB1_SCK_B	—	—
IP2[4:3]	A20	SPCLK	—	—	—	—	—	—	—
IP2[6:5]	A21	ATAWR0#_B	MOSI_IO0	—	—	—	—	—	—
IP2[9:7]	A22	MISO_IO1	—	TX0	SCIFA0_TXD	—	—	—	—
IP2[12:10]	A23	IO2	—	RX0	SCIFA0_RXD	—	—	—	—
IP2[15:13]	A24	DREQ2	IO3	TX1	SCIFA1_TXD	—	—	—	—
IP2[18:16]	A25	DACK2	SSL	DREQ1_C	RX1	SCIFA1_RXD	—	—	—
IP2[20:19]	CS0#	ATAG0#_B	I2C1_SCL	—	—	—	—	—	—
IP2[22:21]	CS1#/A26	ATADIR0#_B	I2C1_SDA	—	—	—	—	—	—
IP2[24:23]	EX_CS1#	MSIOF2_SCK	-	—	—	—	—	—	—
IP2[26:25]	EX_CS2#	ATAWR0#	MSIOF2_SYNC	—	—	—	—	—	—
IP2[29:27]	EX_CS3#	ATADIR0#	MSIOF2_TXD	ATAG0#	—	EX_WAIT1	—	—	—

Legend: — Setting prohibited

5.3.13 Peripheral Function Select Register 3 (IPSR3)

Function: IPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP3 [30]	IP3 [29]	IP3 [28]	IP3 [27]	IP3 [26]	IP3 [25]	IP3 [24]	IP3 [23]	IP3 [22]	IP3 [21]	IP3 [20]	IP3 [19]	IP3 [18]	IP3 [17]	IP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP3 [15]	IP3 [14]	IP3 [13]	IP3 [12]	IP3 [11]	IP3 [10]	IP3 [9]	IP3 [8]	IP3 [7]	IP3 [6]	IP3 [5]	IP3 [4]	IP3 [3]	IP3 [2]	IP3 [1]	IP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP3[2:0]	EX_CS4#	ATARD0#	MSIOF2_RXD	—	EX_WAIT2	—	—	—	—
IP3[5:3]	EX_CS5#	ATACS00#	MSIOF2_SS1	HRX1_B	SCIFB1_RXD_B	PWM1	TPU_TO1	—	—
IP3[8:6]	BS#	ATACS10#	MSIOF2_SS2	HTX1_B	SCIFB1_TXD_B	PWM2	TPU_TO2	—	—
IP3[11:9]	RD/WR#	HRX2_B\HRX2_D	—	SCIFB0_RXD_B	DREQ1_D	—	—	—	—
IP3[13:12]	WE0#	HCTS2#_B	SCIFB0_TXD_B	—	—	—	—	—	—
IP3[15:14]	WE1#	ATARD0#_B	HTX2_B	SCIFB0_RTS#_B	—	—	—	—	—
IP3[17:16]	EX_WAIT0	HRTS2#_B	SCIFB0_CTS#_B	—	—	—	—	—	—
IP3[19:18]	DREQ0	PWM3	TPU_TO3	—	—	—	—	—	—
IP3[21:20]	DACK0	DRACK0	—	—	—	—	—	—	—
IP3[24:22]	—	—	HSCK0_C	HSCK2_C	SCIFB0_SCK_B	SCIFB2_SCK_B	DREQ2_C	HTX2_D	-
IP3[27:25]	SSI_SCK0129	HRX0_C	HRX2_C	SCIFB0_RXD_C	SCIFB2_RXD_C	—	—	—	—
IP3[30:28]	SSI_WS0129	HTX0_C	HTX2_C	SCIFB0_TXD_C	SCIFB2_TXD_C	—	—	—	—

Legend: — Setting prohibited

5.3.17 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP7 [29]	IP7 [28]	IP7 [27]	IP7 [26]	IP7 [25]	IP7 [24]	IP7 [23]	IP7 [22]	IP7 [21]	IP7 [20]	IP7 [19]	IP7 [18]	IP7 [17]	IP7 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP7 [15]	IP7 [14]	IP7 [13]	IP7 [12]	IP7 [11]	IP7 [10]	IP7 [9]	IP7 [8]	IP7 [7]	IP7 [6]	IP7 [5]	IP7 [4]	IP7 [3]	IP7 [2]	IP7 [1]	IP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP7[2:0]	IRQ9	DU1_DOTCLKIN_B	CAN_CLK_D	—	SCIF_CLK_B	—	—
IP7[5:3]	DU1_DR0	—	VI1_DATA0_B	TX0_B	SCIFA0_TXD_B	MSIOF2_SCK_B	—
IP7[8:6]	DU1_DR1	—	VI1_DATA1_B	RX0_B	SCIFA0_RXD_B	MSIOF2_SYNC_B	—
IP7[10:9]	DU1_DR2	—	SSI_SCK0129_B	—	—	—	—
IP7[12:11]	DU1_DR3	—	SSI_WS0129_B	—	—	—	—
IP7[14:13]	DU1_DR4	—	SSI_SDATA0_B	—	—	—	—
IP7[16:15]	DU1_DR5	—	SSI_SCK1_B	—	—	—	—
IP7[18:17]	DU1_DR6	—	SSI_WS1_B	—	—	—	—
IP7[20:19]	DU1_DR7	—	SSI_SDATA1_B	—	—	—	—
IP7[23:21]	DU1_DG0	—	VI1_DATA2_B	TX1_B	SCIFA1_TXD_B	MSIOF2_SS1_B	—
IP7[26:24]	DU1_DG1	—	VI1_DATA3_B	RX1_B	SCIFA1_RXD_B	MSIOF2_SS2_B	—
IP7[29:27]	DU1_DG2	—	VI1_DATA4_B	SCIF1_SCK_B	SCIFA1_SCK	SSI_SCK78_B	—

Legend: — Setting prohibited

5.3.19 Peripheral Function Select Register 9 (IPSR9)

Function: IPSR9 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP9 [31]	IP9 [30]	IP9 [29]	IP9 [28]	IP9 [27]	IP9 [26]	IP9 [25]	IP9 [24]	IP9 [23]	IP9 [22]	IP9 [21]	IP9 [20]	IP9 [19]	IP9 [18]	IP9 [17]	IP9 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP9 [15]	IP9 [14]	IP9 [13]	IP9 [12]	IP9 [11]	IP9 [10]	IP9 [9]	IP9 [8]	IP9 [7]	IP9 [6]	IP9 [5]	IP9 [4]	IP9 [3]	IP9 [2]	IP9 [1]	IP9 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP9[2:0]	DU1_DB6	—	I2C3_SCL_C	RX3	SCIFA3_RXD	—	—	—
IP9[5:3]	DU1_DB7	—	I2C3_SDA_C	SCIF3_SCK	SCIFA3_SCK	—	—	—
IP9[6]	DU1_DOTCLKIN	—	—	—	—	—	—	—
IP9[7]	DU1_DOTCLKOUT0	—	—	—	—	—	—	—
IP9[10:8]	DU1_DOTCLKOUT1	—	CAN0_TX	TX3_B	I2C2_SCL_B	PWM4	—	—
IP9[11]	DU1_EXHSYNC_DU1_HSYNC	—	—	—	—	—	—	—
IP9[12]	DU1_EXVSYNC_DU1_VSYNC	—	—	—	—	—	—	—
IP9[15:13]	DU1_EXODDF_DU1_ODDF_DISP_CDE	—	CAN0_RX	RX3_B	I2C2_SDA_B	—	—	—
IP9[16]	DU1_DISP	—	—	—	—	—	—	—
IP9[18:17]	DU1_CDE	—	PWM4_B	—	—	—	—	—
IP9[20:19]	VI0_CLKENB	TX4	SCIFA4_TXD	TS_SDATA0_D	—	—	—	—
IP9[22:21]	VI0_FIELD	RX4	SCIFA4_RXD	TS_SCK0_D	—	—	—	—
IP9[24:23]	VI0_HSYNC#	TX5	SCIFA5_TXD	TS_SDEN0_D	—	—	—	—
IP9[26:25]	VI0_VSYNC#	RX5	SCIFA5_RXD	TS_SPSYNC0_D	—	—	—	—
IP9[28:27]	VI0_DATA3_VI0_B3	SCIF3_SCK_B	SCIFA3_SCK_B	—	—	—	—	—
IP9[31:29]	VI0_G0	IIC1_SCL	—	I2C4_SCL	HCTS2#	SCIFB2_CTS#	ATAWR1#	—

Legend: — Setting prohibited

5.3.23 Peripheral Function Select Register 13 (IPSR13)

Function: IPSR13 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP13 [30]	IP13 [29]	IP13 [28]	IP13 [27]	IP13 [26]	IP13 [25]	IP13 [24]	IP13 [23]	IP13 [22]	IP13 [21]	IP13 [20]	IP13 [19]	IP13 [18]	IP13 [17]	IP13 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP13 [15]	IP13 [14]	IP13 [13]	IP13 [12]	IP13 [11]	IP13 [10]	IP13 [9]	IP13 [8]	IP13 [7]	IP13 [6]	IP13 [5]	IP13 [4]	IP13 [3]	IP13 [2]	IP13 [1]	IP13 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP13[2:0]	—	AVB_TX_ER	SCIFB2_SCK_C	—	MSIOF0_SS1_C	—	—	—	—
IP13[4:3]	—	AVB_TX_CLK	—	MSIOF0_SS2_C	—	—	—	—	—
IP13[6:5]	—	AVB_COL	—	MSIOF0_RXD_C	—	—	—	—	—
IP13[9:7]	—	AVB_GTX_CLK	PWM0_B	—	MSIOF0_TXD_C	—	—	—	—
IP13[10]	SD0_CLK	SPCLK_B	—	—	—	—	—	—	—
IP13[11]	SD0_CMD	MOSI_IO0_B	—	—	—	—	—	—	—
IP13[12]	SD0_DATA0	MISO_IO1_B	—	—	—	—	—	—	—
IP13[13]	SD0_DATA1	IO2_B	—	—	—	—	—	—	—
IP13[14]	SD0_DATA2	IO3_B	—	—	—	—	—	—	—
IP13[15]	SD0_DATA3	SSL_B	—	—	—	—	—	—	—
IP13[18:16]	SD0_CD	MMC_D6_B	—	CAN0_RX_F	SCIFA5_TXD_B	TX3_C			—
IP13[21:19]	SD0_WP	MMC_D7_B	—	CAN0_TX_F	SCIFA5_RXD_B	RX3_C			—
IP13[22]	SD2_CMD	—	—	—	—	—	—	—	—
IP13[24:23]	SD2_DATA0	—	—	—	—	—	—	—	—
IP13[25]	SD2_DATA1	—	—	—	—	—	—	—	—
IP13[26]	SD2_DATA2	—	—	—	—	—	—	—	—
IP13[27]	SD2_DATA3	—	—	—	—	—	—	—	—
IP13[30:28]	SD2_CD	PWM0	TPU_TO0	I2C1_SCL_C		—	—	—	—

Legend: — Setting prohibited

5.3.28 Module Select Register 2 (MOD_SEL2)

Function: MOD_SEL2 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF, RCAN, ADG and SSI is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 and ssi7 (in MOD_SEL register) are to be used simultaneously, the values of sel_ssi8 and sel_ssi7 must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_ scif0_2	sel_ scif0_1	sel_ scif0_0	—	sel_scif	sel_ can0_2	sel_ can0_1	sel_ can0_0	sel_ can1_1	sel_ can1_0	—	sel_ scifa2_0	sel_ scif4_1	sel_ scif4_0	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ adg_0	—	—	—	sel_ scifa5_1	sel_ scifa5_0	—	—	—	sel_ scifa4_1	sel_ scifa4_0	sel_ scifa3_1	sel_ scifa3_0	—	—	sel_ ssi8_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)
sel_scif0[2:0]	RX0 of the A23 pin TX0 of the A22 pin	RX0_B of the DU1_DR1 pin TX0_B of the DU1_DR0 pin	RX0_C of the VI0_R5 pin TX0_C of the VI0_R4 pin	RX0_D of the SSI_SDATA7 pin TX0_D of the SSI_WS78 pin	RX0_E of the MSIOF0_SS2 pin TX0_E of the MSIOF0_SS1 pin	—
sel_scif	SCIF_CLK of the AUDIO_CLKB pin	SCIF_CLK_B of the IRQ9 pin	—	—	—	—
sel_can0[2:0]	CAN0_RX of the DU1_EXODDF_ DU1_ODDF_DISP_CDE pin CAN0_TX of the DU1_DOTCLKOUT1 pin	CAN0_RX_B of the HRX0 pin CAN0_TX_B of the HTX0 pin	CAN0_RX_C of the ETH_LINK pin CAN0_TX_C of the ETH_RXD1 pin	CAN0_RX_D of the SSI_SDATA9 pin CAN0_TX_D of the SSI_WS9 pin	CAN0_RX_E of the VI0_R7 pin CAN0_TX_E of the VI0_G5 pin	CAN0_RX_F of the SD0_CD pin CAN0_TX_F of the SD0_WP pin
sel_can1[1:0]	CAN1_RX of the DU1_DB4 pin CAN1_TX of the DU1_DB5 pin	CAN1_RX_B of the HRTS1# pin CAN1_TX_B of the HCTS1# pin	CAN1_RX_C of the ETH_REFCLK pin CAN1_TX_C of the ETH_TXD1 pin	CAN1_RX_D of the SIM0_D pin CAN1_TX_D of the SIM0_RST pin	—	—
sel_scifa2	SCIFA2_RXD of the AUDIO_CLKC pin SCIFA2_TXD of the AUDIO_CLKOUT pin	SCIFA2_SCK of the DU1_DB2 pin * SCIFA2_RXD_B of the DU1_DB1 pin SCIFA2_TXD_B of the DU1_DB0 pin	—	—	—	—
sel_scif4[1:0]	RX4 of the VI0_FIELD pin TX4 of the VI0_CLKENB pin	RX4_B of the VI1_VSYNC# pin TX4_B of the VI1_HSYNC# pin	RX4_C of the GPS_MAG pin TX4_C of the GPS_SIGN pin	—	—	—
sel_adg	AUDIO_CLKB of the AUDIO_CLKB pin	AUDIO_CLKB_B of the GPS_CLK pin	—	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scif5	RX5 of the VI0_VSYNC# pin TX5 of the VI0_HSYNC# pin	RX5_B of the SD3_WP pin TX5_B of the SD3_CD pin	—	—	—
sel_i2c2[1:0]	I2C2_SCL of the SSI_SCK2 pin I2C2_SDA of the SSI_WS2 pin	I2C2_SCL_B of the DU1_DOTCLKOUT1 pin I2C2_SDA_B of the DU1_EXODDF_ DU1_ODDF_DISP_CDE pin	I2C2_SCL_C of the ETH_MDIO pin I2C2_SDA_C of the ETH_CRS_DV pin	I2C2_SCL_D of the ETH_RXD1 pin I2C2_SDA_D of the ETH_LINK pin	—
sel_i2c1[2:0]	I2C1_SCL of the CS0# pin I2C1_SDA of the CS1#/A26 pin	I2C1_SCL_B of the SSI_WS1 pin I2C1_SDA_B of the SSI_SDATA1 pin	I2C1_SCL_C of the SD2_CD pin I2C1_SDA_C of the SD2_WP pin	I2C1_SCL_D of the VI0_R4 pin I2C1_SDA_D of the VI0_R5 pin	I2C1_SCL_E of the IRQ5 pin I2C1_SDA_E of the IRQ6 pin
sel_i2c0[1:0]	I2C0_SCL of the A8 pin I2C0_SDA of the A9 pin	I2C0_SCL_B of the SSI_SDATA0 pin I2C0_SDA_B of the SSI_SCK1 pin	I2C0_SCL_C of the A0 pin I2C0_SDA_C of the A17 pin	—	—

Legend: – Setting prohibited

5.3.31 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR0 [31]	PUPR0 [30]	PUPR0 [29]	PUPR0 [28]	PUPR0 [27]	PUPR0 [26]	PUPR0 [25]	PUPR0 [24]	PUPR0 [23]	PUPR0 [22]	PUPR0 [21]	PUPR0 [20]	PUPR0 [19]	PUPR0 [18]	PUPR0 [17]	PUPR0 [16]
Initial value:	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR0 [15]	PUPR0 [14]	PUPR0 [13]	PUPR0 [12]	PUPR0 [11]	PUPR0 [10]	PUPR0 [9]	PUPR0 [8]	PUPR0 [7]	PUPR0 [6]	PUPR0 [5]	PUPR0 [4]	PUPR0 [3]	PUPR0 [2]	PUPR0 [1]	PUPR0 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR0[31:0]	H'D87F FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR0[31]	A9 pin is pulled up
PUPR0[30]	A8 pin is pulled up
PUPR0[29]	A7 pin is pulled up
PUPR0[28]	A6 pin is pulled up
PUPR0[27]	A5 pin is pulled up
PUPR0[26]	A4 pin is pulled up
PUPR0[25]	A3 pin is pulled up
PUPR0[24]	A2 pin is pulled up
PUPR0[23]	A1 pin is pulled up
PUPR0[22]	A0 pin is pulled up
PUPR0[21]	D15 pin is pulled up
PUPR0[20]	D14 pin is pulled up
PUPR0[19]	D13 pin is pulled up
PUPR0[18]	D12 pin is pulled up
PUPR0[17]	D11 pin is pulled up
PUPR0[16]	D10 pin is pulled up
PUPR0[15]	D9 pin is pulled up
PUPR0[14]	D8 pin is pulled up
PUPR0[13]	D7 pin is pulled up
PUPR0[12]	D6 pin is pulled up
PUPR0[11]	D5 pin is pulled up
PUPR0[10]	D4 pin is pulled up
PUPR0[9]	D3 pin is pulled up
PUPR0[8]	D2 pin is pulled up
PUPR0[7]	D1 pin is pulled up

Bit Name	Set Value = 1
PUPR3[6]	IRQ8 pin is pulled up
PUPR3[5]	IRQ7 pin is pulled up
PUPR3[4]	IRQ6 pin is pulled up
PUPR3[3]	IRQ5 pin is pulled up
PUPR3[2]	IRQ4 pin is pulled up
PUPR3[1]	IRQ3 pin is pulled up
PUPR3[0]	IRQ2 pin is pulled up

5.4 Operation

5.4.1 Function Setting for Multiplexed Pins

Setting the LSI multiplexed pin setting mask register (PMMR) is necessary before setting each of the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16). Specifically, the inverse of the value to be set in the select register must be written to the LSI multiplexed pin setting mask register. Otherwise, the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16) cannot be set. IPSR0 to IPSR16, MOD_SEL and MOD_SEL2 to MOD_SEL4 registers shall be set before setting GPSR0 to GPSR7 registers in case that they need to be configured. MOD_SEL and MOD_SEL2 to MOD_SEL4 registers can be set either earlier or later than setting IPSR0 to IPSR16 registers.

Note: When GPIO is selected by GPSRn for an LSI pin and one of the below pin functions is selected by IPSRn, make sure to disable data reception of SCIFA3/4/5.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

(1) Procedure for changing pin function from GPIO to peripheral function

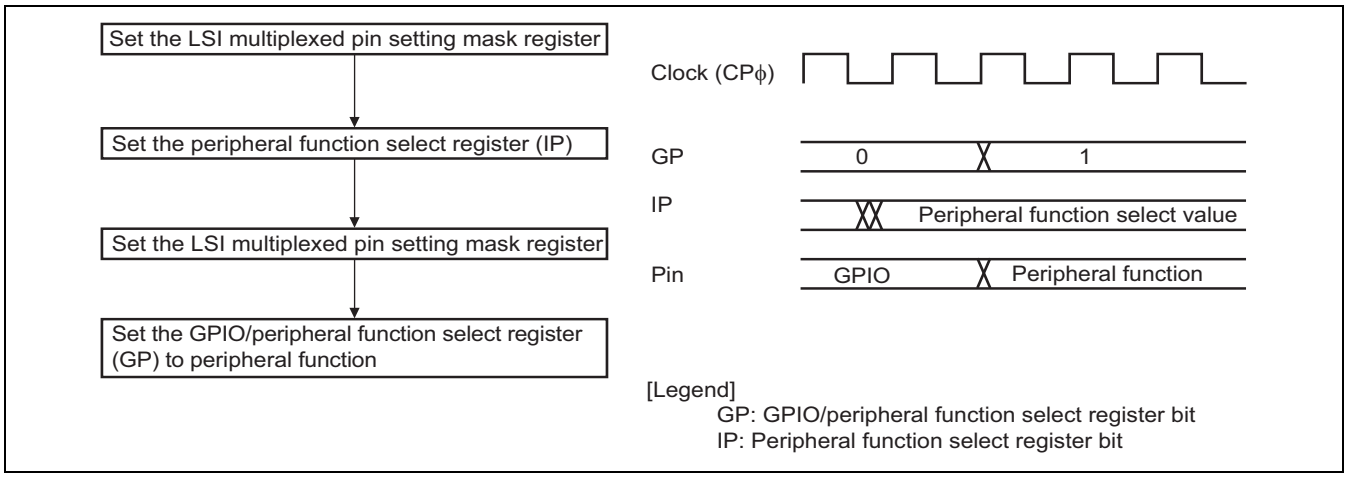

Figure 5.1 Procedure for Changing Pin Function from GPIO to Peripheral Function

RZ/G1M

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