Renesas Electronics America Inc - R8A77430HA02BG#UA Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77430ha02bg-ua

1.3.2 CPU Core Peripherals

Item	Description
Operating clock pulse generation circuit (CPG)	• Generates the clocks from external clock (EXTAL1). — Maximum Cortex-A15 clock: 1.5 GHz — Maximum AXI-bus clock: 260 MHz — Maximum SDRAM bus clock: 800 MHz (DDR3L-1600), 666 MHz (DDR3L-1333) — Maximum media clock: 260 MHz — Maximum peripheral clock (HPϕ): 130 MHz • System-CPU shut down mode control supported • Module-standby mode supported • Includes module reset registers to control reset operation of individual on-chip peripheral modules
System controller (SYSC)	• Shuts down and restores power to target modules. Target modules: — Cortex-A15 (with independent shutting down of CPUs 0, 1, and SCU+L2$)*1 — 3DGE*2 Notes: 1. SCU and L2$ are treated as one power-domain. When CPU is working, SCU+L2$ can't be powered off. 2. Although 3DGE is a target of power-shutdown, version/revision is different from H1's 3DGE. Please refer to 3DGE's specification.
Reset (RST)	• Includes one reset-signal external output port for external modules • Includes Boot Address Register etc.
Pin function controller (PFC)	• Setting multiplexed pin functions for LSI pins Function of the RZ/G1M pin selectable by setting the registers in the PFC module. • Module selection Enable and disable the functions of RZ/G1M LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module. • Pull-up control for each LSI pin On/off of the pull-up resistor on each LSI pin can be controlled by setting the registers in the PFC module. • Control of SDIO functions SDIO functions, including the driving ability of pins for the SDIF, can be controlled by setting registers of the PFC.
General-purpose I/O (GPIO)	• General-purpose I/O ports: 244 • Supports GPIO interrupts.
Thermal sensor (THS/TSC)	• Single channel of thermal sensor • Programmable 4 temperature level for the sensor, to indicate the temperature level • Selectable operation (Interrupt/Reset) when the temperature reaches programmed

1.3.10 Network

Item	Description
CAN interface (CAN)	• Two channels • Supports CAN specification 2.0B • ISO-11898-1 compliant • Maximum bit rate: 1 Mbps • Message box — Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception — FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception • Reception — Data frame and remote frame can be received. — Selectable receiving ID format — Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • Acceptance filter — Mask can be enabled or disabled for each mailbox. • Transmission — Data frame and remote frame can be transmitted. — Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) — Selectable ID priority mode or mailbox number priority mode • Sleep mode for reducing power consumption
PCI-Express Controller (PCIEC)	• PCI Express Base Specification Revision 2.0 • Single channel • PHY integrated
Ethernet AVB	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Supports transfer at 1000 Mbps and 100 Mbps • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY GMII (Gigabit Media Independent Interface) and MII (Media Independent Interface)
Ethernet MAC	• IEEE802.3u MAC (Ether) function • Supports transfer at 10 and 100 Mbps • Flow control conforming to IEEE802.3x or back pressure system • Supports interface conforming to IEEE802.3u • Magic packet detection • Includes DMAC • Supports RMII (Reduced Media Independent Interface)

1.3.11 Timer

Item	Description
Watchdog timer (RWDT)	• Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time-period: more than 1 hour count capable

CPG, RESET, SYSTEM, AVS, POWER ISO and Debug (No.189 to 212): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
189	CPG	I
AL18	EXTAL	1.8V/-
	I	-
190	CPG	O
AL17	XTAL	1.8V/-
	O	-
191	CPG	P
F16	VDD_CPGPLL1	-
	P	-
192	CPG	P
F15	VSS_CPGPLL1	-
	P	-
193	CPG	P
H15	VDD_CPGPLL2	-
	P	-
194	CPG	P
G15	VSS_CPGPLL2	-
	P	-
195	CPG	P
L25	VDD_CPGPLL0	-
	P	-
196	CPG	P
M25	VSS_CPGPLL0	-
	P	-
197	CPG	P
L26	VDD_CPGPLL3	-
	P	-
198	CPG	P
M26	VSS_CPGPLL3	-
	P	-
199	RESET	I(S)
AE19	PRESET#	1.8V/-
	I(S)	-
200	RESET	L
U5	PRESETOUT#	3.3V/4mA
	O(L to H)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up(pull-down)*2
201	SYSTEM	I(S)
AG19	MPMD0	1.8V/-
	I(S)	-
202	SYSTEM	I(S)
AG18	MPMD1	1.8V/-
	I(S)	-
203	SYSTEM	I(S)
AF17	BSMODE	1.8V/-
	I(S)	-
204	AVS	L
U6	AVS1	3.3V/4mA
	O(H/L)*1	Off
205	AVS	L
U7	AVS2	3.3V/4mA
	O(H/L)*1	Off
206	POWER ISO	P
AD19	VCCQ_ISO	-
	P	-
207	Debug	I
AF19	TRST#	1.8V/-
	I	On
208	Debug	I
AE18	TCK	1.8V/-
	I	On
209	Debug	I
AF18	TMS	1.8V/-
	I(I)	On
210	Debug	I
AH17	TDI	1.8V/-
	I	On
211	Debug	Z
AJ17	TDO	1.8V/8mA
	O(Z)	-
212	Debug	I
AE17	ACK	1.8V/4mA
	IO(I)	On(pulled-down)*2

Notes: 1. (No.204 and 205): Output value of the AVS[2:1] pins depends on each product.
2. (No.212): ACK pin is available for pull-down function.

LBSC, MSIOF, I2C, SCIFA, SCIFB, QSPI, SCIF, HSCIF, PWM, TPU, GPIO (No.344 to 360): Up to 9-Function Multiplexed and Mode Pins assigned (No.344, 345, 347, 348, 351)

These pins default function (function 1 or GPIO) after power-on reset depends on MD[3:1] pins setting except for No.346 and 350 to 360 pins.

	Function									
	1	2	3	4	5	6	7	8	GPIO	
	MD[3:1]=000								MD[3:1]≠000	
No.	Module									During POR
Pin No.	Pin Name									V/|IOH|
Mode Pin	I/O									Pull-up
344	LBSC	LBSC	MSIOF2	HSCIF1	SCIFB1	PWM2	TPU	Reserved		I(Mode Pin)
N3	BS#	ATACS10#	MSIOF2_SS2	HTX1_B	SCIFB1_TXD_B	PWM2	TPU_TO2	-	GP1_18	3.3V/4mA
MD10	O(H)	O	O	O	O	O	O	-	IO(I)	Off
345	LBSC	-	-	-	-	-	-	-		I(Mode Pin)
V2	RD#	-	-	-	-	-	-	-	GP1_19	3.3V/4mA
MD12	O(H)	-	-	-	-	-	-	-	IO(I)	Off
346*	LBSC	HSCIF2	Reserved	SCIFB0	LBSC	HSCIF2	-	-		I(GPIO)
N4	RD/WR#	HRX2_B	-	SCIFB0_RXD_B	DREQ1_D	HRX2_D	-	-	GP1_20	3.3V/4mA
	O	I	-	I	I	I	-	-	IO(I)	On
347	LBSC	HSCIF2	SCIFB0	-	-	-	-	-		I(Mode Pin)
N5	WE0#	HCTS2#_B	SCIFB0_TXD_B	-	-	-	-	-	GP1_21	3.3V/4mA
MD6	O(H)	IO	O	-	-	-	-	-	IO(I)	Off
348	LBSC	LBSC	HSCIF2	SCIFB0	-	-	-	-		I(Mode Pin)
N6	WE1#	ATARD0#_B	HTX2_B	SCIFB0_RTS#_B	-	-	-	-	GP1_22	3.3V/4mA
MD4	O(H)	O	O	O	-	-	-	-	IO(I)	Off
349	LBSC	HSCIF2	SCIFB0	-	-	-	-	-		I(GPIO)
U3	EX_WAIT0	HRTS2#_B	SCIFB0_CTS#_B	-	-	-	-	-	GP1_23	3.3V/4mA
	I(I)	IO	I	-	-	-	-	-	IO(I)	On
350*	LBSC	PWM3	TPU	-	-	-	-	-		I(GPIO)
U4	DREQ0	PWM3	TPU_TO3	-	-	-	-	-	GP1_24	3.3V/4mA
	I	O	O	-	-	-	-	-	IO(I)	On
351*	LBSC	LBSC	Reserved	-	-	-	-	-		I(Mode Pin)
N7	DACK0	DRACK0	-	-	-	-	-	-	GP1_25	3.3V/4mA
MD7	O	O	-	-	-	-	-	-	IO(I)	Off
352*	Reserved	Reserved	HSCIF0	HSCIF2	SCIFB0	SCIFB2	LBSC	HSCIF2		I(GPIO)
T25	-	-	HSCK0_C	HSCK2_C	SCIFB0_SCK_B	SCIFB2_SCK_B	DREQ2_C	HTX2_D	GP5_31	3.3V/4mA
	-	-	IO	IO	O	O	I	O	IO(I)	On
353*	SSI	HSCIF0	HSCIF2	SCIFB0	SCIFB2	-	-	-		I(GPIO)
V31	SSI_SCK0129	HRX0_C	HRX2_C	SCIFB0_RXD_C	SCIFB2_RXD_C	-	-	-	GP2_0	3.3V/8mA
	IO	I	I	I	I	-	-	-	IO(I)	On
354*	SSI	HSCIF0	HSCIF2	SCIFB0	SCIFB2	-	-	-		I(GPIO)
V30	SSI_WS0129	HTX0_C	HTX2_C	SCIFB0_TXD_C	SCIFB2_TXD_C	-	-	-	GP2_1	3.3V/8mA
	IO	O	O	O	O	-	-	-	IO(I)	On
355*	SSI	I2C0	IIC0(I2C7)	MSIOF2	-	-	-	-		I(GPIO)
V29	SSI_SDATA0	I2C0_SCL_B	IIC0_SCL_B	MSIOF2_SCK_C	-	-	-	-	GP2_2	3.3V/8mA
	IO	IO	IO	IO	-	-	-	-	IO(I)	On
356*	SSI	I2C0	IIC0(I2C7)	MSIOF2	Reserved	-	-	-		I(GPIO)
W31	SSI_SCK1	I2C0_SDA_B	IIC0_SDA_B	MSIOF2_SYNC_C	-	-	-	-	GP2_3	3.3V/8mA
	IO	IO	IO	IO	-	-	-	-	IO(I)	On
357*	SSI	I2C1	IIC1(I2C8)	MSIOF2	Reserved	-	-	-		I(GPIO)
V28	SSI_WS1	I2C1_SCL_B	IIC1_SCL_B	MSIOF2_TXD_C	-	-	-	-	GP2_4	3.3V/8mA
	IO	IO	IO	O	-	-	-	-	IO(I)	On
358*	SSI	I2C1	IIC1(I2C8)	MSIOF2	-	-	-	-		I(GPIO)
V27	SSI_SDATA1	I2C1_SDA_B	IIC1_SDA_B	MSIOF2_RXD_C	-	-	-	-	GP2_5	3.3V/8mA
	IO	IO	IO	I	-	-	-	-	IO(I)	On
359*	SSI	I2C2	Reserved	Reserved	HSCIF1	-	-	-		I(GPIO)
W30	SSI_SCK2	I2C2_SCL	-	-	HSCK1_E	-	-	-	GP2_6	3.3V/8mA
	IO	IO	-	-	IO	-	-	-	IO(I)	On
360*	SSI	I2C2	Reserved	SCIF2	Reserved	HSCIF1	Reserved	-		I(GPIO)
W29	SSI_WS2	I2C2_SDA	-	RX2_E	-	HCTS1#_E	-	-	GP2_7	3.3V/8mA
	IO	IO	-	I	-	IO	-	-	IO(I)	On

Note: * (No.346 and 350 to 360): These pins are set for GPIO even if MD[3:1] = 000 after power-on reset. For details, refer to GPSR1, GPSR2 and GPSR5 registers in section 5, Pin Function Controller (PFC).

VIN, I2C, HSCIF, SCIFB, LBSC, RCAN and GPIO (No.436 to 455): Up to 8-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR4 register in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
	I/O								Pull-up
436	VIN0	SCIF3	SCIFA3	Reserved	-	-	-		I(GPIO)
AC3	VI0_DATA3/VI0_B3	SCIF3_SCK_B	SCIFA3_SCK_B	-	-	-	-	GP4_8	3.3V/4mA
	I	IO	O	-	-	-	-	IO(I)	On
437	VIN0	-	-	-	-	-	-		I(GPIO)
AB7	VI0_DATA4/VI0_B4	-	-	-	-	-	-	GP4_9	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
438	VIN0	-	-	-	-	-	-		I(GPIO)
AC4	VI0_DATA5/VI0_B5	-	-	-	-	-	-	GP4_10	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
439	VIN0	-	-	-	-	-	-		I(GPIO)
AC6	VI0_DATA6/VI0_B6	-	-	-	-	-	-	GP4_11	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
440	VIN0	-	-	-	-	-	-		I(GPIO)
AC7	VI0_DATA7/VI0_B7	-	-	-	-	-	-	GP4_12	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
441	VIN0	IIC1(I2C8)	Reserved	I2C4	HSCIF2	SCIFB2	LBSC		I(GPIO)
AD1	VI0_G0	IIC1_SCL	-	I2C4_SCL	HCTS2#	SCIFB2_CTS#	ATAWR1#	GP4_13	3.3V/4mA
	I	IO	-	IO	IO	I	O	IO(I)	On
442	VIN0	IIC1(I2C8)	Reserved	I2C4	HSCIF2	SCIFB2	LBSC		I(GPIO)
AD2	VI0_G1	IIC1_SDA	-	I2C4_SDA	HRTS2#	SCIFB2_RTS#	ATADIR1#	GP4_14	3.3V/4mA
	I	IO	-	IO	IO	O	O	IO(I)	On
443	VIN0	VIN2	Reserved	I2C3	HSCIF2	SCIFB2	LBSC		I(GPIO)
AD3	VI0_G2	VI2_HSYNC#	-	I2C3_SCL_B	HSCK2	SCIFB2_SCK	ATARD1#	GP4_15	3.3V/4mA
	I	I	-	IO	IO	O	O	IO(I)	On
444	VIN0	VIN2	Reserved	I2C3	HSCIF2	SCIFB2	LBSC		I(GPIO)
AD4	VI0_G3	VI2_VSYNC#	-	I2C3_SDA_B	HRX2	SCIFB2_RXD	ATACS01#	GP4_16	3.3V/4mA
	I	I	-	IO	I	I	O	IO(I)	On
445	VIN0	VIN2	Reserved	HSCIF2	SCIFB2	SCIFB0	-		I(GPIO)
AD5	VI0_G4	VI2_CLKENB	-	HTX2	SCIFB2_TXD	SCIFB0_SCK_D	-	GP4_17	3.3V/4mA
	I	I	-	O	O	O	-	IO(I)	On
446	VIN0	VIN2	Reserved	Reserved	RCAN0	HSCIF1	SCIFB0		I(GPIO)
AD6	VI0_G5	VI2_FIELD	-	-	CAN0_TX_E	HTX1_D	SCIFB0_TXD_D	GP4_18	3.3V/4mA
	I	I	-	-	O	O	O	IO(I)	On
447	VIN0	VIN2	Reserved	-	-	-	-		I(GPIO)
AE6	VI0_G6	VI2_CLK	-	-	-	-	-	GP4_19	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
448	VIN0	VIN2	Reserved	-	-	-	-		I(GPIO)
AD7	VI0_G7	VI2_DATA0	-	-	-	-	-	GP4_20	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
449	VIN0	VIN2	Reserved	TSIF0	LBSC	-	-		I(GPIO)
AE1	VI0_R0	VI2_DATA1	-	TS_SDATA0_C	ATACS11#	-	-	GP4_21	3.3V/4mA
	I	I	-	I	O	-	-	IO(I)	On
450	VIN0	VIN2	Reserved	TSIF0	LBSC	-	-		I(GPIO)
AE3	VI0_R1	VI2_DATA2	-	TS_SCK0_C	ATAG1#	-	-	GP4_22	3.3V/4mA
	I	I	-	I	O	-	-	IO(I)	On
451	VIN0	VIN2	Reserved	TSIF0	-	-	-		I(GPIO)
AE4	VI0_R2	VI2_DATA3	-	TS_SDEN0_C	-	-	-	GP4_23	3.3V/4mA
	I	I	-	I	-	-	-	IO(I)	On
452	VIN0	VIN2	Reserved	TSIF0	-	-	-		I(GPIO)
AE5	VI0_R3	VI2_DATA4	-	TS_SPSYNC0_C	-	-	-	GP4_24	3.3V/4mA
	I	I	-	I	-	-	-	IO(I)	On
453	VIN0	VIN2	Reserved	SCIF0	I2C1	-	-		I(GPIO)
AF3	VI0_R4	VI2_DATA5	-	TX0_C	I2C1_SCL_D	-	-	GP4_25	3.3V/4mA
	I	I	-	O	IO	-	-	IO(I)	Off
454	VIN0	VIN2	Reserved	SCIF0	I2C1	-	-		I(GPIO)
AF4	VI0_R5	VI2_DATA6	-	RX0_C	I2C1_SDA_D	-	-	GP4_26	3.3V/4mA
	I	I	-	I	IO	-	-	IO(I)	Off
455	VIN0	VIN2	Reserved	SCIF1	I2C4	-	-		I(GPIO)
AF5	VI0_R6	VI2_DATA7	-	TX1_C	I2C4_SCL_B	-	-	GP4_27	3.3V/4mA
	I	I	-	O	IO	-	-	IO(I)	Off

HSCIF, SCIFB, VIN, RCAN and GPIO (No.534 to 540): Up to 7-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR7 register in section 5, Pin Function Controller (PFC).

	Function							
	1	2	3	4	5	6	GPIO	
No.	Module							During POR
Pin No.	Pin Name							V/|IOH|
	I/O							Pull-up
534	HSCIF0	SCIFB0	Reserved	Reserved	RCAN0	VIN1		I(GPIO)
P29	HRX0	SCIFB0_RXD	-	-	CAN0_RX_B	VI1_DATA4_C	GP7_3	3.3V/8mA
	I	I	-	-	I	I	IO(I)	On
535	HSCIF0	SCIFB0	Reserved	Reserved	RCAN0	VIN1		I(GPIO)
P30	HTX0	SCIFB0_TXD	-	-	CAN0_TX_B	VI1_DATA5_C	GP7_4	3.3V/8mA
	O	O	-	-	O	I	IO(I)	Off
536	HSCIF1	SCIFB1	VIN1	Reserved	VIN1	-		I(GPIO)
V25	HRX1	SCIFB1_RXD	VI1_R0_B	-	VI1_DATA6_C	-	GP7_5	3.3V/8mA
	I	I	I	-	I	-	IO(I)	Off
537	HSCIF1	SCIFB1	VIN1	Reserved	VIN1	-		I(GPIO)
V26	HTX1	SCIFB1_TXD	VI1_R1_B	-	VI1_DATA7_C	-	GP7_6	3.3V/8mA
	O	O	I	-	I	-	IO(I)	Off
538	HSCIF1	SCIFB1	Reserved	Reserved	-	-		I(GPIO)
U31	HSCK1	SCIFB1_SCK	-	-	-	-	GP7_7	3.3V/16mA
	IO	O	-	-	-	-	IO(I)	-
539	HSCIF1	SCIFB1	Reserved	RCAN1	-	-		I(GPIO)
U29	HCTS1#	SCIFB1_CTS#	-	CAN1_TX_B	-	-	GP7_8	3.3V/16mA
	IO	I	-	O	-	-	IO(I)	-
540	HSCIF1	SCIFB1	Reserved	RCAN1	-	-		I(GPIO)
U28	HRTS1#	SCIFB1_RTS#	-	CAN1_RX_B	-	-	GP7_9	3.3V/16mA
	IO	O	-	I	-	-	IO(I)	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
43	B27	M0DQ4	IO	Z	M0DQ4	Z	-
44	B29	M0DQ5	IO	Z	M0DQ5	Z	-
45	C27	M0DQ6	IO	Z	M0DQ6	Z	-
46	A30	M0DQ7	IO	Z	M0DQ7	Z	-
47	E26	M0DQS0	IO	Z	M0DQS0	Z	-
48	E25	M0DQS0#	IO	Z	M0DQS0#	Z	-
49	A28	M0DM0	O	Z	M0DM0	Z	-
50	G22	VDDQ_M0DPLL0	-	P	VDDQ_M0DPLL0	P	-
51	G23	VSSQ_M0DPLL0	-	P	VSSQ_M0DPLL0	P	-
52	G24	M0VREFDQ0	-	P	M0VREFDQ0	P	-
53	B23	M0DQ8	IO	Z	M0DQ8	Z	-
54	A24	M0DQ9	IO	Z	M0DQ9	Z	-
55	C24	M0DQ10	IO	Z	M0DQ10	Z	-
56	D24	M0DQ11	IO	Z	M0DQ11	Z	-
57	B26	M0DQ12	IO	Z	M0DQ12	Z	-
58	D26	M0DQ13	IO	Z	M0DQ13	Z	-
59	B24	M0DQ14	IO	Z	M0DQ14	Z	-
60	A25	M0DQ15	IO	Z	M0DQ15	Z	-
61	E23	M0DQS1	IO	Z	M0DQS1	Z	-
62	E24	M0DQS1#	IO	Z	M0DQS1#	Z	-
63	C25	M0DM1	O	Z	M0DM1	Z	-
64	F22	VDDQ_M0DPLL1	-	P	VDDQ_M0DPLL1	P	-
65	F23	VSSQ_M0DPLL1	-	P	VSSQ_M0DPLL1	P	-
66	E31	M0DQ16	IO	Z	M0DQ16	Z	-
67	C30	M0DQ17	IO	Z	M0DQ17	Z	-
68	E29	M0DQ18	IO	Z	M0DQ18	Z	-
69	B31	M0DQ19	IO	Z	M0DQ19	Z	-
70	E30	M0DQ20	IO	Z	M0DQ20	Z	-
71	C31	M0DQ21	IO	Z	M0DQ21	Z	-
72	E28	M0DQ22	IO	Z	M0DQ22	Z	-
73	D29	M0DQ23	IO	Z	M0DQ23	Z	-
74	F27	M0DQS2	IO	Z	M0DQS2	Z	-
75	G27	M0DQS2#	IO	Z	M0DQS2#	Z	-
76	D31	M0DM2	O	Z	M0DM2	Z	-
77	K25	VDDQ_M0DPLL2	-	P	VDDQ_M0DPLL2	P	-
78	J25	VSSQ_M0DPLL2	-	P	VSSQ_M0DPLL2	P	-
79	H25	M0VREFDQ1	-	P	M0VREFDQ1	P	-
80	F28	M0DQ24	IO	Z	M0DQ24	Z	-
81	G31	M0DQ25	IO	Z	M0DQ25	Z	-
82	F30	M0DQ26	IO	Z	M0DQ26	Z	-
83	H30	M0DQ27	IO	Z	M0DQ27	Z	-
84	H28	M0DQ28	IO	Z	M0DQ28	Z	-
85	J30	M0DQ29	IO	Z	M0DQ29	Z	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
342	V4	EX_CS4#	IO	I	GP1_16	I	On
343	V5	EX_CS5#	IO	I(MD8)	GP1_17	I	Off
344	N3	BS#	IO	I(MD10)	BS#/GP1_18*5	H/I	Off
345	V2	RD#	IO	I(MD12)	RD#/GP1_19*5	H/I	Off
346	N4	RD/WR#	IO	I	GP1_20	I	On
347	N5	WE0#	IO	I(MD6)	WE0#/GP1_21*5	H/I	Off
348	N6	WE1#	IO	I(MD4)	WE1#/GP1_22*5	H/I	Off
349	U3	EX_WAIT0	IO	I	EX_WAIT0/GP1_23*5	I/I	On
350	U4	DREQ0	IO	I	GP1_24	I	On
351	N7	DACK0	IO	I(MD7)	GP1_25	I	Off
352	T25	SPEEDIN	IO	I	GP5_31	I	On
353	V31	SSI_SCK0129	IO	I	GP2_0	I	On
354	V30	SSI_WS0129	IO	I	GP2_1	I	On
355	V29	SSI_SDATA0	IO	I	GP2_2	I	On
356	W31	SSI_SCK1	IO	I	GP2_3	I	On
357	V28	SSI_WS1	IO	I	GP2_4	I	On
358	V27	SSI_SDATA1	IO	I	GP2_5	I	On
359	W30	SSI_SCK2	IO	I	GP2_6	I	On
360	W29	SSI_WS2	IO	I	GP2_7	I	On
361	W28	SSI_SDATA2	IO	I	GP2_8	I	On
362	W27	SSI_SCK34	IO	I	GP2_9	I	On
363	W26	SSI_WS34	IO	I	GP2_10	I	On
364	W25	SSI_SDATA3	IO	I	GP2_11	I	On
365	Y31	SSI_SCK4	IO	I	GP2_12	I	Off
366	Y30	SSI_WS4	IO	I	GP2_13	I	Off
367	Y29	SSI_SDATA4	IO	I	GP2_14	I	On
368	Y28	SSI_SCK5	IO	I	GP2_15	I	On
369	Y27	SSI_WS5	IO	I	GP2_16	I	On
370	Y26	SSI_SDATA5	IO	I	GP2_17	I	On
371	AA31	SSI_SCK6	IO	I	GP2_18	I	On
372	AA30	SSI_WS6	IO	I	GP2_19	I	Off
373	AA29	SSI_SDATA6	IO	I	GP2_20	I	Off
374	AA27	SSI_SCK78	IO	I	GP2_21	I	Off
375	AA26	SSI_WS78	IO	I	GP2_22	I	Off
376	Y25	SSI_SDATA7	IO	I	GP2_23	I	On
377	AA25	SSI_SDATA8	IO	I	GP2_24	I	On
378	AB31	SSI_SCK9	IO	I	GP2_25	I	Off
379	AB30	SSI_WS9	IO	I	GP2_26	I	Off
380	AB29	SSI_SDATA9	IO	I	GP2_27	I	On
381	AD31	AUDIO_CLKA	IO	I	GP2_28	I	On
382	AC30	AUDIO_CLKB	IO	I	GP2_29	I	On
383	AD30	AUDIO_CLKC	IO	I	GP2_30	I	On
384	AE31	AUDIO_CLKOUT	IO	I(MD5)	GP2_31	I	Off

Table 4.3 Handling of Unused Pins

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
1	F20	M0CKE0	L	-	-	-	Open
2	C19	M0CKE1	L	-	-	-	Open
3	G16	VSS	P	-	-	-	Must be used
4	H18	M0BKPRST#	I	-	-	-	Pulled-up to VDDQ_M0BKUP or pulled-down to VSS
5	E19	M0RESET#	H to L	-	-	-	Open
6	G20	M0CK0	O	-	-	-	Open
7	G19	M0CK0#	O	-	-	-	Open
8	G17	M0CK1	O	-	-	-	Open
9	G18	M0CK1#	O	-	-	-	Open
10	B20	M0CS0#	H	-	-	-	Open
11	A19	M0CS1#	H	-	-	-	Open
12	D20	M0ODT0	L	-	-	-	Open
13	E18	M0ODT1	L	-	-	-	Open
14	H16	M0ZQ	IO	-	-	-	Must be used
15	E21	M0WE#	H	-	-	-	Open
16	D22	M0RAS#	H	-	-	-	Open
17	C22	M0CAS#	H	-	-	-	Open
18	E17	M0A0	L	-	-	-	Open
19	B22	M0A1	L	-	-	-	Open
20	A22	M0A2	L	-	-	-	Open
21	D17	M0A3	L	-	-	-	Open
22	A21	M0A4	L	-	-	-	Open
23	D16	M0A5	L	-	-	-	Open
24	B17	M0A6	L	-	-	-	Open
25	B21	M0A7	L	-	-	-	Open
26	A16	M0A8	L	-	-	-	Open
27	B18	M0A9	L	-	-	-	Open
28	C18	M0A10	L	-	-	-	Open
29	A18	M0A11	L	-	-	-	Open
30	E16	M0A12	L	-	-	-	Open
31	A17	M0A13	L	-	-	-	Open
32	B16	M0A14	L	-	-	-	Open
33	D18	M0A15	L	-	-	-	Open
34	C21	M0BA0	L	-	-	-	Open
35	C16	M0BA1	L	-	-	-	Open
36	D21	M0BA2	L	-	-	-	Open
37	G21	VDDQ_M0APLL	P	-	-	-	Must be used
38	H21	VSSQ_M0APLL	P	-	-	-	Must be used
39	A27	M0DQ0	Z	-	-	-	Open
40	C28	M0DQ1	Z	-	-	-	Open
41	D27	M0DQ2	Z	-	-	-	Open
42	A29	M0DQ3	Z	-	-	-	Open

5. Pin Function Controller (PFC)

5.1 Overview

The pin function controller (PFC) is a module that consists of registers for selecting the function of the multiplexed pins and controlling the pull-up resistor on each LSI pin.

5.1.1 Features

- Register access through the APB bus interface
- Setting multiplexed pin functions for LSI pins

  Function of the RZ/G1M pin selectable by setting the registers in the PFC module

  (The function of the LSI pin can be selected by the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16) in the PFC module. For details, see sections 5.3.2, GPIO/Peripheral Function Select Register 0 (GPSR0) through 5.3.26, Peripheral Function Select Register 16 (IPSR16).)
- Module selection

  Enable and disable the functions of RZ/G1M LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.

  (Selection is handled by the module select register (MOD_SEL), module select register 2 (MOD_SEL2), module select register 3 (MOD_SEL3) and module register4 (MOD_SEL4). For details, see sections 5.3.27, Module Select Register (MOD_SEL), through 5.3.30, Module Select Register 4 (MOD_SEL4).
- Pull-up control for each LSI pin.

  On/off of the pull-up or pull-down resistors on each LSI pin can be controlled by setting the registers in the PFC module.

  (The pull-up or pull-down resistors on each LSI pin can be turned on or off individually by setting the LSI pin pull-up/down control registers 0 to 7 (PUPR0 to PUPR7) in the PFC module. For details, see sections 5.3.31, LSI Pin Pull-Up Control Register 0 (PUPR0) through 5.3.38, LSI Pin Pull-Up Control Register 7 (PUPR7).)
- Control of IO functions, including SDHI, IRQ, DU, Ethernet, ADG, SSI and LBSC.

  SDIO functions, including the driving ability, POC of pins, can be controlled by setting registers of the PFC module. For details, see sections 5.3.39, SD Control Register 0 (IOCTRL0) through 5.3.44, IIC3 (DVFS) and TDBG IO Cell Control Register (IOCTRL7).

  DDR3 GPIO function can also be selected by setting registers of the PFC. For details, see sections 5.3.45, DDR3 General Port IO Enable Register (DDR3GPEN) through 5.3.48, DDR3 General Port Input Data Register (DDR3GPID).

5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR)

Function: PMMR enables/disables writing to the multiplexed pin setting registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMPM															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PMPM															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PMPM[31:0]	H'0000 0000	R/W	Multiplexed Pin Setting Mask Writing a value to any register from among the GPIO/peripheral function select registers GPSR0 to GPSR7, peripheral function select registers IPSR0 to IPSR16, module select registers MOD_SEL, MOD_SEL2, MOD_SEL3 and MOD_SEL4, IO cell control registers IOCTRL0, IOCTRL1 and IOCTRL4 to IOCTRL7 is enabled by writing the inverse of the value to this register.

Note: This register must be set before setting each of the GPIO/peripheral function select registers GPSR0 to GPSR7, peripheral function select registers IPSR0 to IPSR16, module select registers MOD_SEL, MOD_SEL2, MOD_SEL3 and MOD_SEL4, IO cell control registers IOCTRL0, IOCTRL1 and IOCTRL4 to IOCTRL7.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[21]	GP-1-21	Peripheral function selected by IP3[13:12]
GP1[22]	GP-1-22	Peripheral function selected by IP3[15:14]
GP1[23]	GP-1-23	Peripheral function selected by IP3[17:16]
GP1[24]	GP-1-24	Peripheral function selected by IP3[19:18]
GP1[25]	GP-1-25	Peripheral function selected by IP3[21:20]
GP1[26]	—	—
GP1[27]	—	—
GP1[28]	—	—
GP1[29]	—	—
GP1[30]	—	—
GP1[31]	—	—

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP7[25]	GP-7-25	USB1_PWEN
GP7[26]	GP-7-26	—
GP7[27]	GP-7-27	—
GP7[28]	GP-7-28	—
GP7[29]	GP-7-29	—
GP7[30]	GP-7-30	—
GP7[31]	GP-7-31	—

5.3.17 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP7 [29]	IP7 [28]	IP7 [27]	IP7 [26]	IP7 [25]	IP7 [24]	IP7 [23]	IP7 [22]	IP7 [21]	IP7 [20]	IP7 [19]	IP7 [18]	IP7 [17]	IP7 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP7 [15]	IP7 [14]	IP7 [13]	IP7 [12]	IP7 [11]	IP7 [10]	IP7 [9]	IP7 [8]	IP7 [7]	IP7 [6]	IP7 [5]	IP7 [4]	IP7 [3]	IP7 [2]	IP7 [1]	IP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP7[2:0]	IRQ9	DU1_DOTCLKIN_B	CAN_CLK_D	—	SCIF_CLK_B	—	—
IP7[5:3]	DU1_DR0	—	VI1_DATA0_B	TX0_B	SCIFA0_TXD_B	MSIOF2_SCK_B	—
IP7[8:6]	DU1_DR1	—	VI1_DATA1_B	RX0_B	SCIFA0_RXD_B	MSIOF2_SYNC_B	—
IP7[10:9]	DU1_DR2	—	SSI_SCK0129_B	—	—	—	—
IP7[12:11]	DU1_DR3	—	SSI_WS0129_B	—	—	—	—
IP7[14:13]	DU1_DR4	—	SSI_SDATA0_B	—	—	—	—
IP7[16:15]	DU1_DR5	—	SSI_SCK1_B	—	—	—	—
IP7[18:17]	DU1_DR6	—	SSI_WS1_B	—	—	—	—
IP7[20:19]	DU1_DR7	—	SSI_SDATA1_B	—	—	—	—
IP7[23:21]	DU1_DG0	—	VI1_DATA2_B	TX1_B	SCIFA1_TXD_B	MSIOF2_SS1_B	—
IP7[26:24]	DU1_DG1	—	VI1_DATA3_B	RX1_B	SCIFA1_RXD_B	MSIOF2_SS2_B	—
IP7[29:27]	DU1_DG2	—	VI1_DATA4_B	SCIF1_SCK_B	SCIFA1_SCK	SSI_SCK78_B	—

Legend: — Setting prohibited

5.3.24 Peripheral Function Select Register 14 (IPSR14)

Function: IPSR14 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP14 [31]	IP14 [30]	IP14 [29]	IP14 [28]	IP14 [27]	IP14 [26]	IP14 [25]	IP14 [24]	IP14 [23]	IP14 [22]	IP14 [21]	IP14 [20]	IP14 [19]	IP14 [18]	IP14 [17]	IP14 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP14 [15]	IP14 [14]	IP14 [13]	IP14 [12]	IP14 [11]	IP14 [10]	IP14 [9]	IP14 [8]	IP14 [7]	IP14 [6]	IP14 [5]	IP14 [4]	IP14 [3]	IP14 [2]	IP14 [1]	IP14 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP14[1:0]	SD2_WP	PWM1_B	I2C1_SDA_C	—	—	—	—	—
IP14[2]	SD3_CLK	MMC_CLK	—	—	—	—	—	—
IP14[3]	SD3_CMD	MMC_CMD	—	—	—	—	—	—
IP14[4]	SD3_DATA0	MMC_D0	—	—	—	—	—	—
IP14[5]	SD3_DATA1	MMC_D1	—	—	—	—	—	—
IP14[6]	SD3_DATA2	MMC_D2	—	—	—	—	—	—
IP14[7]	SD3_DATA3	MMC_D3	—	—	—	—	—	—
IP14[10:8]	SD3_CD	MMC_D4	IIC1_SCL_C	TX5_B	SCIFA5_TXD_C	—	—	—
IP14[13:11]	SD3_WP	MMC_D5	IIC1_SDA_C	RX5_B	SCIFA5_RXD_C	—	—	—
IP14[16:14]	MSIOF0_SCK	RX2_C	—	—	VI1_CLK_C	VI1_G0_B	—	—
IP14[19:17]	MSIOF0_SYNC	TX2_C	—	—	VI1_CLKENB_C	VI1_G1_B	—	—
IP14[22:20]	MSIOF0_TXD	—	—	VI1_FIELD_C	VI1_G2_B	—	—	—
IP14[25:23]	MSIOF0_RXD	—	—	VI1_DATA0_C	VI1_G3_B	—	—	—
IP14[28:26]	MSIOF0_SS1	MMC_D6	—	TX0_E	VI1_HSYNC#_C	IIC0_SCL_C	VI1_G4_B	—
IP14[31:29]	MSIOF0_SS2	MMC_D7	—	RX0_E	VI1_VSYNC#_C	IIC0_SDA_C	VI1_G5_B	—

Legend: — Setting prohibited

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)
sel_scifa5 [1:0]	SCIFA5_RXD of the VI0_VSYNC# pin SCIFA5_TXD of the VI0_HSYNC# pin	SCIFA5_RXD_B of the SD0_WP pin SCIFA5_TXD_B of the SD0_CD pin	SCIFA5_RXD_C of the SD3_WP pin SCIFA5_TXD_C of the SD3_CD pin	—	—	—
sel_scifa4 [1:0]	SCIFA4_RXD of the VI0_FIELD pin SCIFA4_TXD of the VI0_CLKENB pin	SCIFA4_RXD_B of the VI1_VSYNC# pin SCIFA4_TXD_B of the VI1_HSYNC# pin	SCIFA4_RXD_C of the GPS_MAG pin SCIFA4_TXD_C of the GPS_SIGN pin	—	—	—
sel_scifa3 [1:0]	SCIFA3_RXD of the DU1_DB6 pin SCIFA3_SCK of the DU1_DB7 pin SCIFA3_TXD of the DU1_DB5 pin	SCIFA3_RXD_B of the ETH_REFCLK pin SCIFA3_SCK_B of the VI0_DATA3_VI0_B3 pin SCIFA3_TXD_B of the ETH_TXD1 pin	SCIFA3_RXD_C of the GPS_SIGN pin SCIFA3_SCK_C of the GPS_MAG pin SCIFA3_TXD_C of the GPS_CLK pin	—	—	—
sel_ssi8	SSI_SDATA8 of the SSI_SDATA8 pin	SSI_SDATA8_B of the DU1_DG5 pin	—	—	—	—

Legend: – Setting prohibited

Note: * Using SCIFA2_SCK is regardless of value of the bit sel_scifa2.

Bit Name	Set Value = 1
PUPR6[6]	SD0_DATA0 pin is pulled up
PUPR6[5]	SD0_CMD pin is pulled up
PUPR6[4]	SD0_CLK pin is pulled up
PUPR6[3]	STP_OPWM_0 pin is pulled up
PUPR6[2]	STP_ISSYNC_0 pin is pulled up
PUPR6[1]	STP_ISEN_0 pin is pulled up
PUPR6[0]	STP_ISD_0 pin is pulled up

Bit	Bit Name	Initial Value	R/W	Description
1	drv2_sd3d0	1	R/W	SD3_DATA0 Setting.
0	drv1_sd3d0	1	R/W	The value of these bits must be 11.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.43 SD Control Register 6 (IOCTRL6)

Function: IOCTRL6 controls the IO voltage of pins in use for the SD interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	poc_sd 0clk	poc_sd 0cmd	poc_sd 0dat0	poc_sd 0dat1	poc_sd 0dat2	poc_sd 0dat3	poc_sd 0cd	poc_sd 0wp	poc_sd 2clk	poc_sd 2cmd	poc_sd 2dat0	poc_sd 2dat1	poc_sd 2dat2	poc_sd 2dat3	poc_sd 2cd	poc_sd 2wp
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	poc_sd 3clk	poc_sd 3cmd	poc_sd 3dat0	poc_sd 3dat1	poc_sd 3dat2	poc_sd 3dat3	poc_sd 3cd	poc_sd 3wp	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	poc_sd0clk	1	R/W	Selecting IO voltage for the pin SD0_CLK 0: 1.8 V 1: 3.3 V
30	poc_sd0cmd	1	R/W	Selecting IO voltage for the pin SD0_CMD 0: 1.8 V 1: 3.3 V
29	poc_sd0dat0	1	R/W	Selecting IO voltage for the pin SD0_DATA0 0: 1.8 V 1: 3.3 V
28	poc_sd0dat1	1	R/W	Selecting IO voltage for the pin SD0_DATA1 0: 1.8 V 1: 3.3 V
27	poc_sd0dat2	1	R/W	Selecting IO voltage for the pin SD0_ DATA2 0: 1.8 V 1: 3.3 V
26	poc_sd0dat3	1	R/W	Selecting IO voltage for the pin SD0_ DATA3 0: 1.8 V 1: 3.3 V
25	poc_sd0cd	1	R/W	Selecting IO voltage for the pin SD0_CD 0: 1.8 V 1: 3.3 V
24	poc_sd0wp	1	R/W	Selecting IO voltage for the pin SD0_WP 0: 1.8 V 1: 3.3 V
23	poc_sd2clk	1	R/W	Selecting IO voltage for the pin SD2_CLK 0: 1.8 V 1: 3.3 V
22	poc_sd2cmd	1	R/W	Selecting IO voltage for the pin SD2_CMD 0: 1.8 V 1: 3.3 V
21	poc_sd2dat0	1	R/W	Selecting IO voltage for the pin SD2_DATA0 0: 1.8 V 1: 3.3 V

In case that one of the pin function in the following list is selected, make sure to disable the data reception of corresponding SCIFAn channel before performing the sequence in the Figure 5.3.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

5.4.2 Setting Pull-Up/Down Resistors

The LSI pin pull-up/down control registers 0 to 7 (PUPR0 to PUPR7) are used to switch the pull-up/down resistors on and off.