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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	2MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	30
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11f1cfn2

SECTION 1INTRODUCTION

The MC68HC11F1 high-performance microcontroller unit (MCU) is an enhanced derivative of the M68HC11 family of microcontrollers and includes many advanced features. This MCU, with a nonmultiplexed expanded bus, is characterized by high speed and low power consumption. The fully static design allows operation at frequencies from 4 MHz to dc.

1.1 Features

- M68HC11 Central Processing Unit (CPU)
- Power Saving STOP and WAIT Modes
- 512 Bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- 1024 Bytes RAM, Data Retained During Standby
- Nonmultiplexed Address and Data Buses
- Enhanced 16-Bit Timer
- Three Input Capture (IC) Channels
- Four Output Compare (OC) Channels
- One Additional Channel, Selectable as Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog
- Enhanced Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- Enhanced Synchronous Serial Peripheral Interface (SPI)
- Eight-Channel 8-Bit Analog-to-Digital (A/D) Converter
- Four Chip-Select Signal Outputs with Programmable Clock Stretching
  - — Two I/O Chip Selects
  - — One Program Chip Select
  - — One General-Purpose Chip Select
- Available in 68-Pin Plastic Leaded Chip Carrier (PLCC) and 80-Pin Plastic Quad Flat Pack (QFP)

2.11.2 Port B

Port B is an 8-bit output-only port. In single-chip modes, port B pins are general-purpose output pins (PB[7:0]). In expanded modes, port B pins act as the high-order address lines (ADDR[15:8]) of the address bus.

PORTB can be read at any time. Reads of PORTB return the pin driver input level. If PORTB is written, the data is stored in internal latches. It drives the pins only in single-chip or bootstrap mode. In expanded operating modes, port B pins are the high-order address outputs (ADDR[15:8]).

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

2.11.3 Port C

Port C is an 8-bit general-purpose I/O port with a data register (PORTC) and a data direction register (DDRC). In single-chip modes, port C pins are general-purpose I/O pins (PC[7:0]). In expanded modes, port C pins are configured as data bus pins (DATA[7:0]).

PORTC can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If PORTC is written, the data is stored in internal latches. It drives the pins only if they are configured as outputs in single-chip or bootstrap mode. Port C pins are general-purpose inputs out of reset in single-chip and bootstrap modes. In expanded and test modes, these pins are data bus lines out of reset.

The CWOM control bit in the OPT2 register disables port C's P-channel output drivers. Because the N-channel driver is not affected by CWOM, setting CWOM causes port C to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTC bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port C bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port C can only be configured for wired-OR operation when the MCU is in single-chip or bootstrap modes.

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

2.11.4 Port D

Port D, a 6-bit general-purpose I/O port, has a data register (PORTD) and a data direction register (DDRD). The six port D lines (D[5:0]) can be used for general-purpose I/O, for the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems.

PORTD can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If PORTD is written, the data is stored in internal latches and can be driven only if port D is configured for general-purpose output.

The DWOM control bit in the SPCR register disables port D's P-channel output drivers. Because the N-channel driver is not affected by DWOM, setting DWOM causes port D to become an open-drain-type output port suitable for wired-OR operation. In wired-

OR mode, (PORTD bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port D bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port D can be configured for wired-OR operation in any operating mode.

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**, **SECTION 7 SERIAL COMMUNICATIONS INTERFACE**, and **SECTION 8 SERIAL PERIPHERAL INTERFACE**.

2.11.5 Port E

Port E is an 8-bit input-only port that is also used as the analog input port for the analog-to-digital converter. Port E pins that are not used for the A/D system can be used as general-purpose inputs. However, PORTE should not be read during the sample portion of an A/D conversion sequence.

Refer to **SECTION 10 ANALOG-TO-DIGITAL CONVERTER**.

2.11.6 Port F

Port F is an 8-bit output-only port. In single-chip mode, port F pins are general-purpose output pins (PF[7:0]). In expanded mode, port F pins act as the low-order address outputs (ADDR[7:0]).

PORTF can be read at any time. Reads of PORTF return the pin driver input level. If PORTF is written, the data is stored in internal latches. It drives the pins only in single-chip or bootstrap mode. In expanded operating modes, port F pins are the low-order address outputs (ADDR[7:0]).

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

2.11.7 Port G

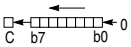
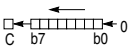
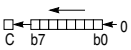
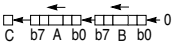
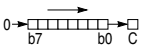
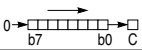
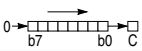
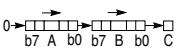
Port G is an 8-bit general-purpose I/O port. When enabled, four chip select signals are alternate functions of port G bits [7:4].

PORTG can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If PORTG is written, the data is stored in internal latches. It drives the pins only if they are configured as outputs.

The GWOM control bit in the OPT2 register disables port G's P-channel output drivers. Because the N-channel driver is not affected by GWOM, setting GWOM causes port G to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTG bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port G bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port G can be configured for wired-OR operation in any operating mode.

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT** and **SECTION 4 OPERATING MODES AND ON-CHIP MEMORY**.

Table 3-2 Instruction Set (Sheet 4 of 6)

Mnemonic	Operation	Description	Addressing Mode	Instruction Opcode	Operand	Cycles	Condition Codes S	X	H	I	N	Z	V	C
INY	Increment Index Register Y	IY + 1 ⇒ IY	INH	18 08	—	4	—	—	—	—	—	Δ	—	—
JMP (opr)	Jump	See Figure 3–2	EXT IND,X IND,Y	7E 6E 18 6E	hh ll ff ff	3 3 4	—	—	—	—	—	—	—	—
JSR (opr)	Jump to Subroutine	See Figure 3–2	DIR EXT IND,X IND,Y	9D BD AD 18 AD	dd hh ll ff ff	5 6 6 7	—	—	—	—	—	—	—	—
LDAA (opr)	Load Accumulator A	M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	86 96 B6 A6 18 A6	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
LDAB (opr)	Load Accumulator B	M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C6 D6 F6 E6 18 E6	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
LDD (opr)	Load Double Accumulator D	M ⇒ A,M + 1 ⇒ B	IMM DIR EXT IND,X IND,Y	CC DC FC EC 18 EC	jj kk dd hh ll ff ff	3 4 5 5 6	—	—	—	—	Δ	Δ	0	—
LDS (opr)	Load Stack Pointer	M : M + 1 ⇒ SP	IMM DIR EXT IND,X IND,Y	8E 9E BE AE 18 AE	jj kk dd hh ll ff ff	3 4 5 5 6	—	—	—	—	Δ	Δ	0	—
LDX (opr)	Load Index Register X	M : M + 1 ⇒ IX	IMM DIR EXT IND,X IND,Y	CE DE FE EE CD EE	jj kk dd hh ll ff ff	3 4 5 5 6	—	—	—	—	Δ	Δ	0	—
LDY (opr)	Load Index Register Y	M : M + 1 ⇒ IY	IMM DIR EXT IND,X IND,Y	18 CE 18 DE 18 FE 1A EE 18 EE	jj kk dd hh ll ff ff	4 5 6 6 6	—	—	—	—	Δ	Δ	0	—
LSL (opr)	Logical Shift Left		EXT IND,X IND,Y	78 68 18 68	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
LSLA	Logical Shift Left A		A INH	48	—	2	—	—	—	—	Δ	Δ	Δ	Δ
LSLB	Logical Shift Left B		B INH	58	—	2	—	—	—	—	Δ	Δ	Δ	Δ
LSLD	Logical Shift Left Double		INH	05	—	3	—	—	—	—	Δ	Δ	Δ	Δ
LSR (opr)	Logical Shift Right		EXT IND,X IND,Y	74 64 18 64	hh ll ff ff	6 6 7	—	—	—	—	0	Δ	Δ	Δ
LSRA	Logical Shift Right A		A INH	44	—	2	—	—	—	—	0	Δ	Δ	Δ
LSRB	Logical Shift Right B		B INH	54	—	2	—	—	—	—	0	Δ	Δ	Δ
LSRD	Logical Shift Right Double		INH	04	—	3	—	—	—	—	0	Δ	Δ	Δ
MUL	Multiply 8 by 8	A * B ⇒ D	INH	3D	—	10	—	—	—	—	—	—	—	Δ
NEG (opr)	Two's Complement Memory Byte	0 – M ⇒ M	EXT IND,X IND,Y	70 60 18 60	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
NEGA	Two's Complement A	0 – A ⇒ A	A INH	40	—	2	—	—	—	—	Δ	Δ	Δ	Δ
NEGB	Two's Complement B	0 – B ⇒ B	B INH	50	—	2	—	—	—	—	Δ	Δ	Δ	Δ

RAM[3:0] — RAM Map Position

These four bits, which specify the upper hexadecimal digit of the RAM address, control position of RAM in the memory map. RAM can be positioned at the beginning of any 4-Kbyte page in the memory map. Refer to **Table 4-5**.

REG[3:0] — 128-Byte Register Block Position

These four bits specify the upper hexadecimal digit of the address for the 128-byte block of internal registers. The register block is positioned at the beginning of any 4-Kbyte page in the memory map. Refer to **Table 4-5**.

Table 4-5 RAM and Register Mapping

RAM[3:0]	Location
0000	$0000–$03FF
0001	$1000–$13FF
0010	$2000–$23FF
0011	$3000–$33FF
0100	$4000–$43FF
0101	$5000–$53FF
0110	$6000–$63FF
0111	$7000–$73FF
1000	$8000–$83FF
1001	$9000–$93FF
1010	$A000–$A3FF
1011	$B000–$B3FF
1100	$C000–$C3FF
1101	$D000–$D3FF
1110	$E000–$E3FF
1111	$F000–$F3FF

REG[3:0]	Location
0000	$0000–$005F
0001	$1000–$105F
0010	$2000–$205F
0011	$3000–$305F
0100	$4000–$405F
0101	$5000–$505F
0110	$6000–$605F
0111	$7000–$705F
1000	$8000–$805F
1001	$9000–$905F
1010	$A000–$A05F
1011	$B000–$B05F
1100	$C000–$C05F
1101	$D000–$D05F
1110	$E000–$E05F
1111	$F000–$F05F

When the memory map has the 96-byte register block mapped at the same location as RAM, the registers have priority and the lower 96 bytes of RAM are inaccessible. No harmful conflicts occur due to a hardware resource priority scheme. On-chip registers have the highest priority of all on-chip resources, followed by on-chip RAM, bootstrap ROM, and on-chip EEPROM.

4.3.2.3 OPTION Register

The 8-bit special-purpose OPTION register sets internal system configuration options during initialization. In single-chip and expanded modes (SMOD = 0), IRQE, DLY, FCME, and CR[1:0] can be written only once and only in the first 64 cycles after a reset. This minimizes the possibility of any accidental changes to the system configuration. In special test and bootstrap modes (SMOD = 1), these bits can be written at any time.

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	FCME*	CR1*	CR0*
RESET:	0	0	0	0	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes.

```
ROWE    LDAB    #$0E        ROW=1, ERASE=1, EELAT=1, EEPGM=0
        STAB    $103B       Set to ROW erase mode
        STAB    0,X         Store any data to any address in ROW
        LDAB    #$0F        ROW=1, ERASE=1, EELAT=1, EEPGM=1
        STAB    $103B       Turn on high voltage
        JSR     DLY10       Delay 10 ms
        CLR     $103B       Turn off high voltage and set to READ mode
```

4.4.1.4 EEPROM Byte Erase

The following is an example of how to erase a single byte of EEPROM and assumes that index register X contains the address of the byte to be erased.

```
BYTEE   LDAB    #$16        BYTE=1, ROW=0, ERASE=1, EELAT=1, EEPGM=0
        STAB    $103B       Set to BYTE erase mode
        STAB    0,X         Store any data to address to be erased
        LDAB    #$17        BYTE=1, ROW=0, ERASE=1, EELAT=1, EEPGM=1
        STAB    $103B       Turn on high voltage
        JSR     DLY10       Delay 10 ms
        CLR     $103B       Turn off high voltage and set to READ mode
```

4.4.2 PPROG EEPROM Programming Control Register

Bits in PPROG register control parameters associated with EEPROM programming.

PPROG — EEPROM Programming Control **$103B**

	Bit 7	6	5	4	3	2	1	Bit 0
	ODD	EVEN	—	BYTE	ROW	ERASE	EELAT	EEPGM
RESET:	0	0	0	0	0	0	0	0

ODD — Program Odd Rows in Half of EEPROM (TEST)

EVEN — Program Even Rows in Half of EEPROM (TEST)

Bit 5 — Not implemented
Always reads zero

BYTE — Byte/Other EEPROM Erase Mode
0 = Row or bulk erase mode used
1 = Erase only one byte of EEPROM

ROW — Row/All EEPROM Erase Mode (only valid when BYTE = 0)
0 = All 512 bytes of EEPROM erased
1 = Erase only one 16-byte row of EEPROM

Table 4-12 Chip Select Control Parameter Summary

CSIO1	Enable	IO1EN in CSCTL —	1 = On, off at reset (0)
	Valid	IO1AV in CSGSIZ —	1 = Address valid, 0 = E valid
	Polarity	IO1PL in CSCTL —	1 = Active high, 0 = Active low
	Size	Fixed —	($x060–$x7FF)
	Start Address	$x060 —	“x” is determined by REG[3:0] in INIT
	Stretch	IO1SA–IO1SB in CSSTRH —	0, 1, 2, or 3 E clocks

CSIO2	Enable	IO2EN in CSCTL —	1 = On, off at reset (0)
	Valid	IO2AV in CSGSIZ —	1 = Address valid, 0 = E valid
	Polarity	IO2PL in CSCTL —	1 = Active high, 0 = Active low
	Size	Fixed —	($x800–$xFFF)
	Start Address	$x800 —	“x” is determined by REG[3:0] in INIT
	Stretch	IO2SA–IO2SB in CSSTRH —	0, 1, 2, or 3 E clocks

$\overline{\text{CSPROG}}$	Enable	PCSEN in CSCTL —	1 = On, on after reset in expanded modes off after reset in single-chip modes
	Valid	Fixed (Address valid)	
	Polarity	Fixed (Active low)	
	Size	PSIZA–PSIZB — in CSCTL	0:0 = 64K ($0000–$FFFF) 0:1 = 32K ($8000–$FFFF) 1:0 = 16K ($C000–$FFFF) 1:1 = 8K ($E000–$FFFF)
	Start Address	Fixed (determined by size)	
	Stretch	PSTHA–PSTHB in CSSTRH —	0, 1, 2, or 3 E clocks 1 cycle after reset in expanded mode no delay after reset in all other modes
	Priority	GCSPR in CSCTL —	1 = CSGEN above $\overline{\text{CSPROG}}$ 0 = $\overline{\text{CSPROG}}$ above CSGEN

CSGEN	Enable	Set size to 0K to disable —	1 = CSGEN above $\overline{\text{CSPROG}}$ 0 = $\overline{\text{CSPROG}}$ above CSGEN
	Valid	GAVLD in CSGSIZ —	Address valid or E valid
	Polarity	GNPOL in CSGSIZ —	Active high or low
	Size	GSIZA–GSIZC in CSGSIZ —	Refer to Table 4–12
	Start Address	GA[15:10] in CSGADR	
	Stretch	GSTHA–GSTHB in CSSTRH —	0, 1, 2, or 3 E clocks

impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port C can only be configured for wired-OR operation when the MCU is in single-chip or bootstrap modes.

PORTC — Port C Data **$1006**

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	I	I	I	I	I	I	I	I
Expan. or Test:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

DDRC — Data Direction Register for Port C **$1007**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction for Port C
0 = Input
1 = Output

6.4 Port D

In all modes, port D bits [5:0] can be used either for general-purpose I/O, or with the SCI and SPI subsystems. During reset, port D pins are configured as high impedance inputs (DDRD bits cleared).

The DWOM control bit in the SPCR register disables port D's P-channel output drivers. Because the N-channel driver is not affected by DWOM, setting DWOM causes port D to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTD bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port D bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port D can be configured for wired-OR operation in any operating mode.

PORTD — Port D Data **$1008**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	I	I	I	I	I	I
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

PORTF — Port F Data **$1005**

	Bit 7	6	5	4	3	2	1	Bit 0
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
S. Chip or Boot:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

6.7 Port G

Port G pins reset to high-impedance inputs except in expanded modes where reset causes PG7 to become the $\overline{\text{CSPROG}}$ output. Alternate functions for port G bits [7:4] are chip select outputs. All port G bits are bidirectional and have corresponding data direction bits.

The GWOM control bit in the OPT2 register disables port G's P-channel output drivers. Because the N-channel driver is not affected by GWOM, setting GWOM causes port G to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTG bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port G bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port G can be configured for wired-OR operation in any operating mode.

PORTG — Port G Data **$1002**

	Bit 7	6	5	4	3	2	1	Bit 0
	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
RESET:	I	I	I	I	I	I	I	I
Alt. Pin Func.:	$\overline{\text{CSPROG}}$	CSGEN	CSIO1	CSIO2	—	—	—	—

DDRG — Data Direction Register for Port G **$1003**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0
RESET:	0	0	0	0	0	0	0	0

DDG[7:0] — Data Direction for Port G
0 = Input
1 = Output

6.8 System Configuration Options 2

The system configuration options 2 register controls several configuration parameters. Bit 6, CWOM, is the only bit in this register that directly affects parallel I/O.

OPT2 — System Configuration Options 2 **$1038**

	Bit 7	6	5	4	3	2	1	Bit 0
	GWOM	CWOM	CLK4X	—	—	—	—	—
RESET:	0	0	1	0	0	0	0	0

GWOM — Port G Wired-OR Mode
0 = Port G operates normally
1 = Port G outputs are open drain

CWOM — Port C Wired-OR Mode
0 = Port C operates normally
1 = Port C outputs are open drain

CLK4X — 4XOUT Clock Enable
Refer to **SECTION 2 PIN DESCRIPTIONS**.

Bits [4:0] — Not implemented
Always read zero

R8 — Receive Data Bit 8
If M bit is set, R8 stores the ninth bit in the receive data character.

T8 — Transmit Data Bit 8
If M bit is set, T8 stores the ninth bit in the transmit data character.

M — Mode (Select Character Format)
0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup by Address Mark/Idle
0 = Wakeup by IDLE line recognition
1 = Wakeup by address mark (most significant data bit set)

7.6.3 Serial Communications Control Register 2

The SCCR2 register provides the control bits that enable or disable individual SCI functions.

SCCR2 — SCI Control Register 2 **$102D**

	Bit 7	6	5	4	3	2	1	Bit 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle-Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
When TE goes from zero to one, one unit of idle character time (logic one) is queued as a preamble.
0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable
0 = Receiver disabled
1 = Receiver enabled

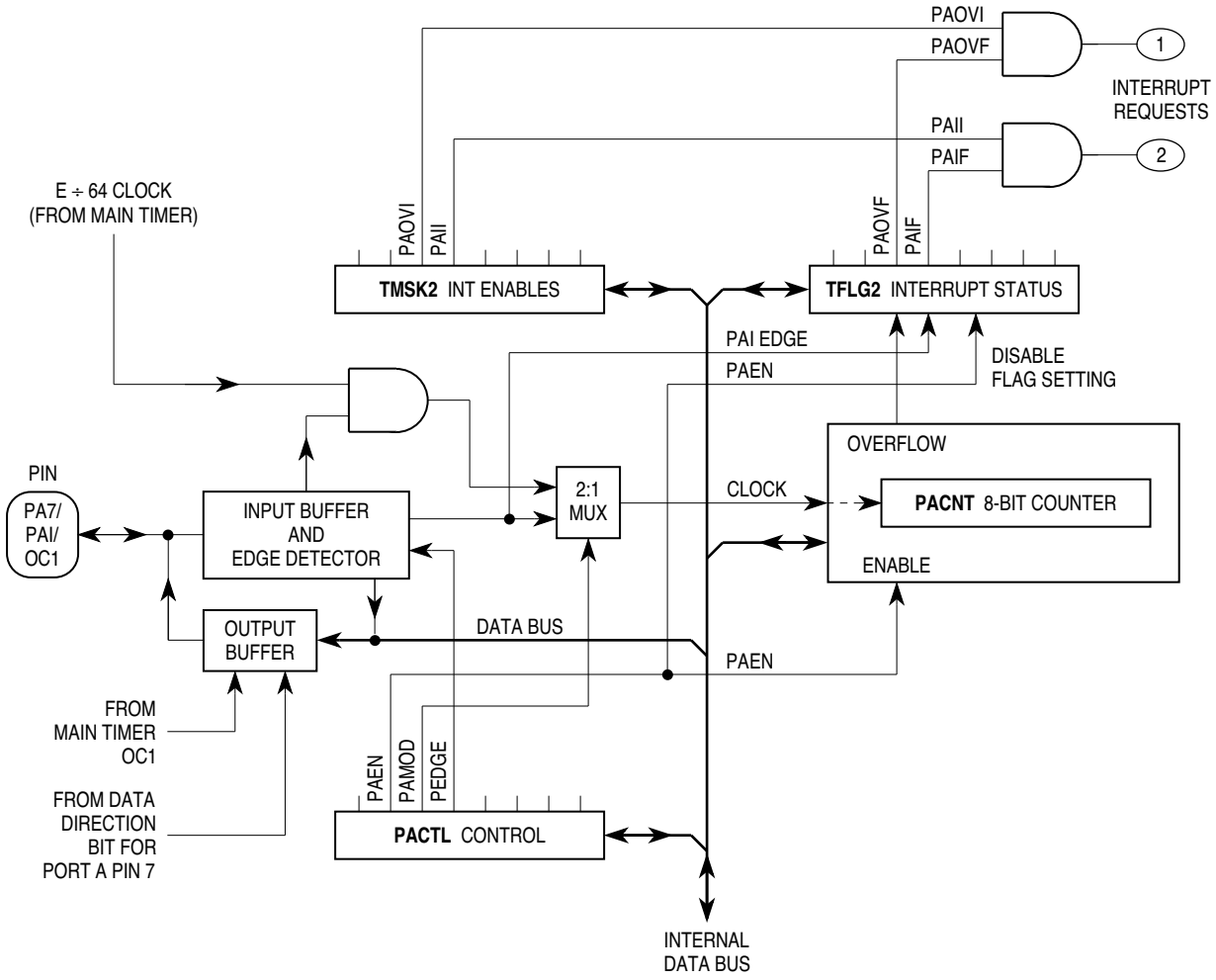


Figure 9-3 Pulse Accumulator

Table 9-5 Pulse Accumulator Timing

Crystal Frequency (4∗E)	E Clock (E)	Cycle Time (1/E)	2^6/E (64/E)	PACNT Overflow (16384/E)
4.0 MHz	1.0 MHz	1000 ns	64 µs	16.384 ms
8.0 MHz	2.0 MHz	500 ns	32 µs	8.192 ms
12.0 MHz	3.0 MHz	333 ns	21.33 µs	5.461 ms
16.0 MHz	4.0 MHz	250 ns	16.0 µs	4.096 ms

Pulse accumulator control bits are also located within two timer registers, TMSK2 and TFLG2, as described in the following paragraphs.

9.6.1 Pulse Accumulator Control Register

Four of this register's bits control an 8-bit pulse accumulator system. Another bit enables either the OC5 function or the IC4 function, while two other bits select the rate for the real-time interrupt system.

9.6.3 Pulse Accumulator Status and Interrupt Bits

The pulse accumulator control bits, PAOVI, PAII, PAOVF, and PAIF are located within timer registers TMSK2 and TFLG2.

TMSK2 — Timer Interrupt Mask 2 Register **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TFLG2 — Timer Interrupt Flag 2 Register **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

PAOVI and PAOVF — Pulse Accumulator Interrupt Enable and Overflow Flag

The PAOVF status bit is set each time the pulse accumulator count rolls over from $FF to $00. To clear this status bit, write a one in the corresponding data bit position (bit 5) of the TFLG2 register. The PAOVI control bit allows configuring the pulse accumulator overflow for polled or interrupt-driven operation and does not affect the state of PAOVF. When PAOVI is zero, pulse accumulator overflow interrupts are inhibited, and the system operates in a polled mode, which requires that PAOVF be polled by user software to determine when an overflow has occurred. When the PAOVI control bit is set, a hardware interrupt request is generated each time PAOVF is set. Before leaving the interrupt service routine, software must clear PAOVF by writing to the TFLG2 register.

PAII and PAIF — Pulse Accumulator Input Edge Interrupt Enable and Flag

The PAIF status bit is automatically set each time a selected edge is detected at the PA7/PAI/OC1 pin. To clear this status bit, write to the TFLG2 register with a one in the corresponding data bit position (bit 4). The PAII control bit allows configuring the pulse accumulator input edge detect for polled or interrupt-driven operation but does not affect setting or clearing the PAIF bit. When PAII is zero, pulse accumulator input interrupts are inhibited, and the system operates in a polled mode. In this mode, the PAIF bit must be polled by user software to determine when an edge has occurred. When the PAII control bit is set, a hardware interrupt request is generated each time PAIF is set. Before leaving the interrupt service routine, software must clear PAIF by writing to the TFLG2 register.

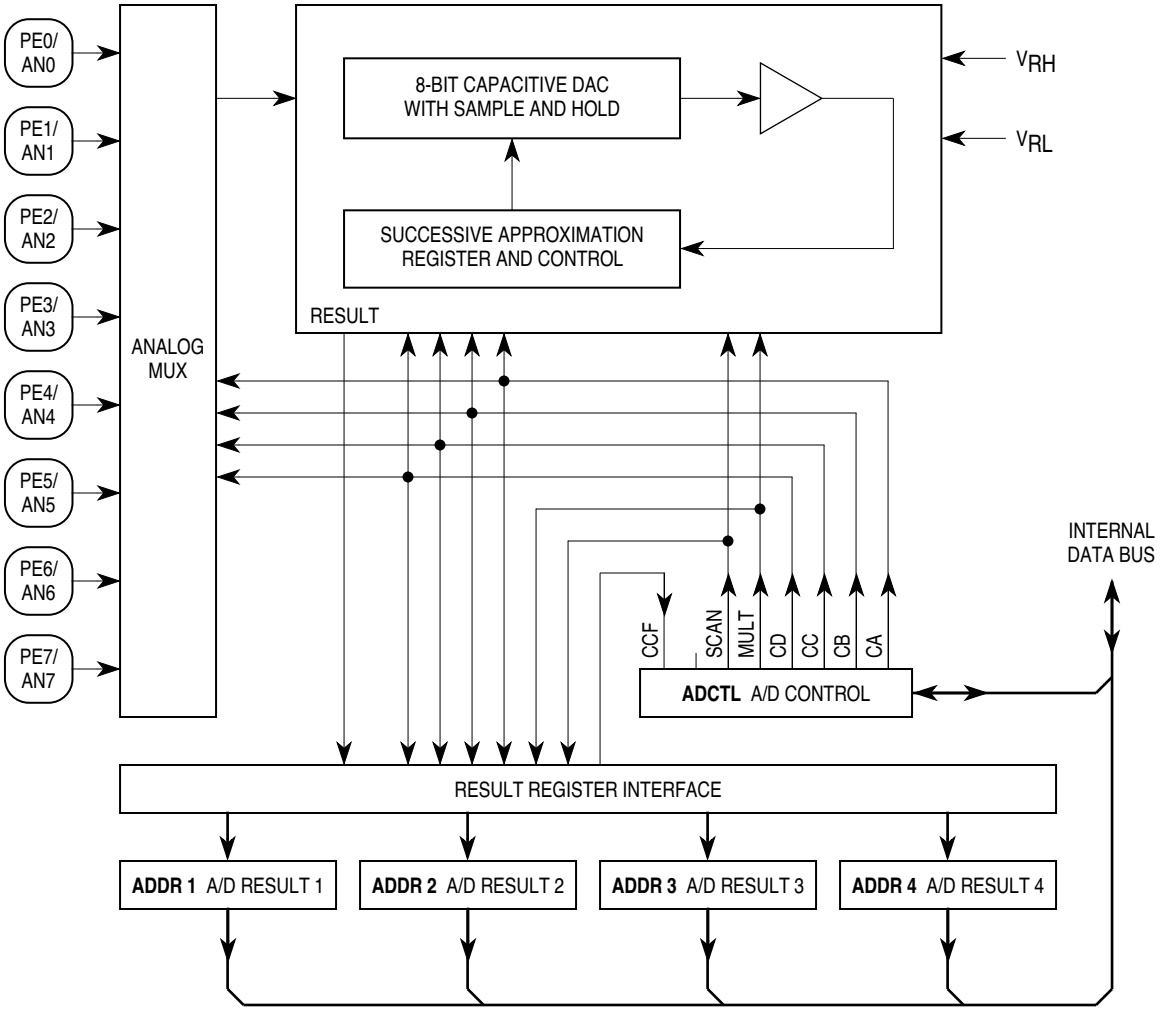


Figure 10-1 A/D Converter Block Diagram

Port E pins can also be used as digital inputs. Reads of port E pins are not recommended during the sample portion of an A/D conversion cycle, when the gate signal to the N-channel input gate is on. Because no P-channel devices are directly connected to either input pins or reference voltage pins, voltages above V_{DD} do not cause a latchup problem, although current should be limited according to maximum ratings. Refer to **Figure 10-2**, which is a functional diagram of an input pin.

10.2 A/D Converter Power-Up and Clock Select

Bit 7 of the OPTION register controls A/D converter power up. Clearing ADPU removes power from and disables the A/D converter system. Setting ADPU enables the A/D converter system. Stabilization of the analog bias voltages requires a delay of as much as 100 µs after turning on the A/D converter. When the A/D converter system is operating with the MCU E clock, all switching and comparator operations are synchronized to the MCU clocks. This allows the comparator results to be sampled at quiet times, which minimizes noise errors. The internal RC oscillator is asynchronous to the MCU clock, so noise affects A/D converter results, which lowers accuracy slightly while CSEL = 1.

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	FCME*	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes

ADPU — A/D Power-Up
- 0 = A/D powered down
- 1 = A/D powered up

CSEL — Clock Select
- 0 = A/D and EEPROM use system E clock
- 1 = A/D and EEPROM use internal RC clock

IRQE — Configure $\overline{\text{IRQ}}$ for Edge-Sensitive Only Operation
Refer to **SECTION 5 RESETS AND INTERRUPTS**.

DLY — Enable Oscillator Start-up Delay
Refer to **SECTION 5 RESETS AND INTERRUPTS**.

CME — Clock Monitor Enable
Refer to **SECTION 5 RESETS AND INTERRUPTS**.

FCME — Force Clock Monitor Enable
Refer to **SECTION 5 RESETS AND INTERRUPTS**.

CR[1:0] — COP Timer Rate Select Bits
Refer to **SECTION 5 RESETS AND INTERRUPTS** and **SECTION 9 TIMING SYSTEM**.

10.3 Conversion Process

The A/D conversion sequence begins one E-clock cycle after a write to the A/D control/status register, ADCTL. The bits in ADCTL select the channel and the mode of conversion.

An input voltage equal to V_{RL} converts to $00 and an input voltage equal to V_{RH} converts to $FF (full scale), with no overflow indication. For ratiometric conversions of this type, the source of each analog input should use V_{RH} as the supply voltage and be referenced to V_{RL}.

Table A-6 Analog-To-Digital Converter Characteristics

V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 750 kHz ≤ E ≤ 3.0 MHz, unless otherwise noted

Characteristic	Parameter	Min	Absolute	2.0 MHz	3.0 MHz	4.0 MHz	Unit
				Max	Max	Max	
Resolution	Number of Bits Resolved by A/D Converter	—	8	—	—	—	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	—	—	± 1	± 1	± 1	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual for Zero Input Voltage	—	—	± 1	± 1	± 1	LSB
Full Scale Error	Difference Between the Output of an Ideal and an Actual A/D for Full-Scale Input Voltage	—	—	± 1	± 1	± 1	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	—	—	± 1/2	± 1 1/2	± 1 1/2	LSB
Quantization Error	Uncertainty Because of Converter Resolution	—	—	± 1/2	± 1/2	± 1/2	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	—	—	± 1	± 2	± 2	LSB
Conversion Range	Analog Input Voltage Range	V_{RL}	—	V_{RH}	V_{RH}	V_{RH}	V
V_{RH}	Maximum Analog Reference Voltage (Note 2)	V_{RL}	—	V_{DD} + 0.1	V_{DD} + 0.1	V_{DD} + 0.1	V
V_{RL}	Minimum Analog Reference Voltage (Note 2)	V_{SS} –0.1	—	V_{RH}	V_{RH}	V_{RH}	V
ΔV_R	Minimum Difference between V_{RH} and V_{RL} (Note 2)	3	—	—	—	—	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion: E Clock Internal RC Oscillator	 — —	 32 —	 — t_{cyc} + 32	 — t_{cyc} + 32	 — t_{cyc} + 32	 t_{cyc} µs
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes		Guaranteed				
Zero Input Reading	Conversion Result when $V_{in} = V_{RL}$	00	—	—	—	—	Hex
Full Scale Reading	Conversion Result when $V_{in} = V_{RH}$	—	—	FF	FF	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time: E Clock Internal RC Oscillator	 — —	 12 —	 — 12	 — 12	 — 12	 t_{cyc} µs
Sample/Hold Capacitance	Input Capacitance during Sample PE[7:0]	—	20 (Typ)	—	—	—	pF
Input Leakage	Input Leakage on A/D Pins PE[7:0] V_{RL}, V_{RH}	— —	— —	400 1.0	400 1.0	400 1.0	nA µA

NOTES:

1. For f_{op} < 2 MHz, source impedances should equal approximately 10 kΩ. For f_{op} ≥ 2 MHz, source impedances should equal approximately 5 kΩ – 10 kΩ. Source impedances greater than 10 kΩ affect accuracy adversely because of input leakage.
2. Performance verified down to 2.5 V ΔV_R, but accuracy is tested and guaranteed at ΔV_R = 5 V ± 10%

Table A-7 Expansion Bus Timing

V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of Operation (E-Clock Frequency)	f_o	dc	2.0	dc	3.0	dc	4.0	MHz
1	Cycle Time $t_{cyc} = 1/f_o$	t_{cyc}	500	—	333	—	250	—	ns
2	Pulse Width, E Low $PW_{EL} = 1/2\ t_{cyc} - 20$ ns	PW_{EL}	230	—	147	—	105	—	ns
3	Pulse Width, E High $PW_{EH} = 1/2\ t_{cyc} - 25$ ns (Note 2)	PW_{EH}	225	—	142	—	100	—	ns
4A 4B	E Clock Rise Time Fall Time	t_r t_f	— —	20 20	— —	20 18	— —	20 15	ns ns
9	Address Hold Time $t_{AH} = 1/8\ t_{cyc} - 10$ ns	t_{AH}	53	—	32	—	21	—	ns
11	Address Delay Time $t_{AD} = 1/8\ t_{cyc} + 40$ ns	t_{AD}	—	103	—	82	—	71	ns
12	Address Valid Time to E Rise $t_{AV} = PW_{EL} - t_{AD}$	t_{AV}	128	—	65	—	34	—	ns
17	Read Data Setup Time	t_{DSR}	30	—	30	—	20	—	ns
18	Read Data Hold Time	t_{DHR}	0	—	0	—	0	—	ns
19	Write Data Delay Time	t_{DDW}	—	40	—	40	—	40	ns
21	Write Data Hold Time $t_{DHW} = 1/8\ t_{cyc}$	t_{DHW}	63	—	42	—	31	—	ns
29	MPU Address Access Time $t_{ACCA} = t_{cyc} - t_f - t_{DSR} - t_{AD}$ (Note 2)	t_{ACCA}	348	—	203	—	144	—	ns
39	Write Data Setup Time $t_{DSW} = PW_{EH} - t_{DDW}$ (Note 2)	t_{DSW}	185	—	102	—	60	—	ns
50	E Valid Chip Select Delay Time	t_{ECSD}	—	40	—	40	—	40	ns
51	E Valid Chip Select Access Time $t_{ECSA} = PW_{EH} - t_{ECSD} - t_{DSR}$ (Note 2)	t_{ECSA}	155	—	72	—	40	—	ns
52	Chip Select Hold Time	t_{CH}	0	20	0	20	0	20	ns
54	Address Valid Chip Select Delay Time $t_{ACSD} = 1/4\ t_{cyc} + 40$ ns	t_{ACSD}	—	165	—	123	—	103	ns
55	Address Valid Chip Select Access Time $t_{ACSA} = t_{cyc} - t_f - t_{DSR} - t_{ACSD}$ (Note 2)	t_{ACSA}	285	—	162	—	113	—	ns
56	Address Valid to Chip Select Time	t_{AVCS}	10	—	10	—	10	—	ns
57	Address Valid to Data Three-State Time	t_{AVDZ}	—	10	—	10	—	10	ns

NOTES:

1. Input clocks with duty cycles other than 50% affect bus performance.
2. Indicates a parameter affected by clock stretching. Add n(t_{cyc}) to parameter value, where:
   n = 1, 2, or 3 depending on values written to CSSTRH register.
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

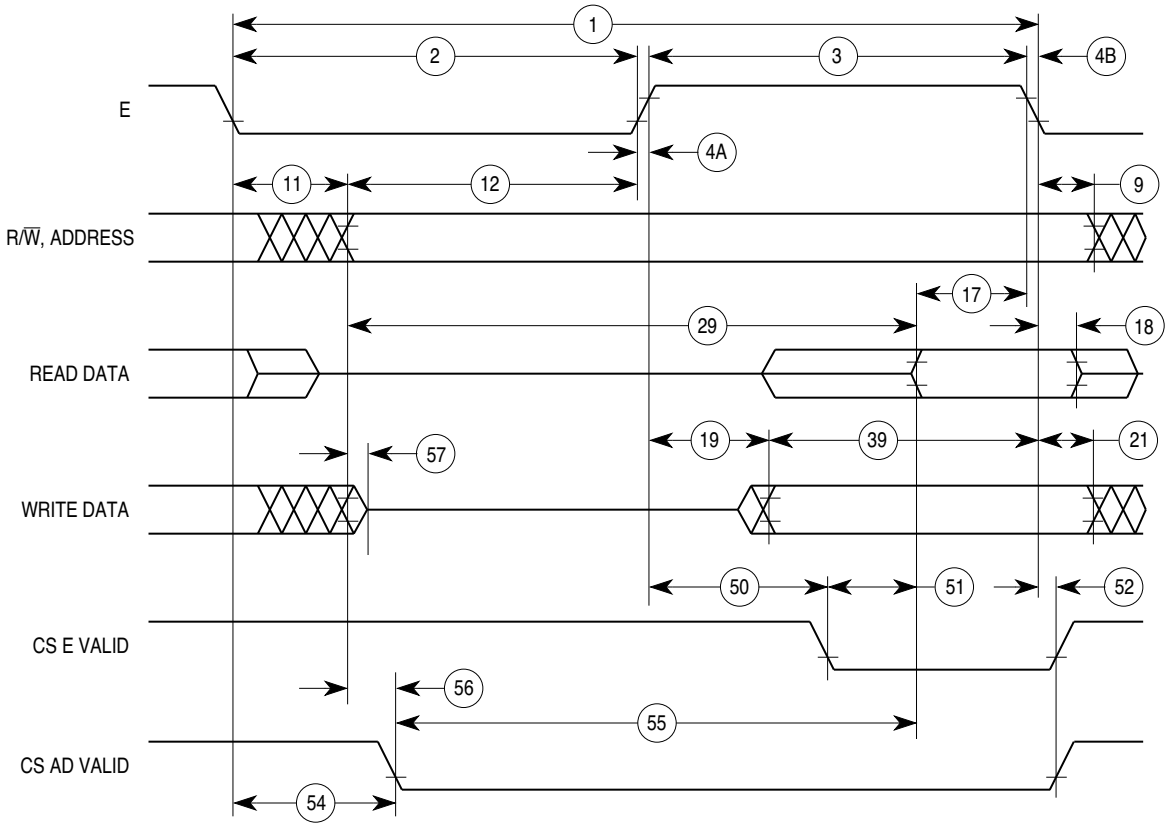


Figure A-9 Expansion Bus Timing

Table A-8 Serial Peripheral Interface Timing

V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Operating Frequency Master Slave	 $f_{op(m)}$ $f_{op(s)}$	 dc dc	 1.0 2.0	 dc dc	 1.5 3.0	 dc dc	 2.0 4.0	 MHz MHz
1	Cycle Time Master Slave	 $t_{cyc(m)}$ $t_{cyc(s)}$	 2.0 500	 — —	 2.0 333	 — —	 2.0 250	 — —	 t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	 $t_{lead(m)}$ $t_{lead(s)}$	 — 250	 — —	 — 240	 — —	 — 200	 — —	 ns ns
3	Enable Lag Time Master (Note 2) Slave	 $t_{lag(m)}$ $t_{lag(s)}$	 — 250	 — —	 — 240	 — —	 — 200	 — —	 ns ns
4	Clock (SCK) High Time Master Slave	 $t_{w(SCKH)m}$ $t_{w(SCKH)s}$	 340 190	 — —	 227 127	 — —	 130 85	 — —	 ns ns
5	Clock (SCK) Low Time Master Slave	 $t_{w(SCKL)m}$ $t_{w(SCKL)s}$	 340 190	 — —	 227 127	 — —	 130 85	 — —	 ns ns
6	Data Setup Time (Inputs) Master Slave	 $t_{su(m)}$ $t_{su(s)}$	 100 100	 — —	 100 100	 — —	 100 100	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{h(m)}$ $t_{h(s)}$	 100 100	 — —	 100 100	 — —	 100 100	 — —	 ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	 t_a	 0	 120	 0	 120	 0	 120	 ns
9	Disable Time (Hold Time to High-Impedance State) Slave	 t_{dis}	 —	 240	 —	 167	 —	 125	 ns
10	Data Valid (After Enable Edge) (Note 3)	$t_{v(s)}$	—	240	—	167	—	125	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{rm} t_{rs}	 — —	 100 2.0	 — —	 100 2.0	 — —	 100 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{fm} t_{fs}	 — —	 100 2.0	 — —	 100 2.0	 — —	 100 2.0	 ns µs

NOTES:
1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 200 pF load on all SPI pins.

Table A-9 EEPROM Characteristics

V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic		Temperature Range			Unit
		0 to 70, – 40 to 85	**–40 to 105**	**–40 to 125**	**° C**
Programming Time (Note 1)	<1.0 MHz, RCO Enabled	10	15	20	ms
	1.0 to 2.0 MHz, RCO Disabled	20	Must use RCO	Must use RCO	
	≥ 2.0 MHz (or Anytime RCO Enabled)	10	15	20	
Erase Time (Note 1)	Byte, Row and Bulk	10	10	10	ms
Write/Erase Endurance (Note 2)		10,000	10,000	10,000	Cycles
Data Retention (Note 2)		10	10	10	Years

NOTES:

1. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0 MHz.
2. Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.