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Applications of "Embedded - Microcontrollers"

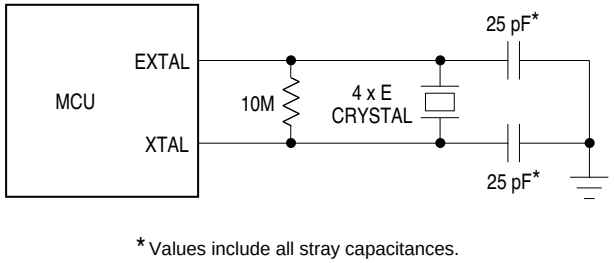
Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	30
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc11f1cfne4r

LIST OF TABLES

The XTAL pin is normally left unterminated when an external CMOS compatible clock is connected to the EXTAL pin. However, a 10 kΩ to 100 kΩ load resistor connected from the XTAL output to ground can be used to reduce RFI noise emission.

The XTAL output is normally used to drive a crystal. The XTAL output can be buffered with a high-impedance buffer, or it can be used to drive the EXTAL input of another M68HC11 device. Refer to **Figure 2-6**.

In all cases, use caution when designing circuitry associated with the oscillator pins. Load capacitances shown in the oscillator circuits include all stray layout capacitances. Refer to **Figure 2-4**, **Figure 2-5**, and **Figure 2-6**.



*Values include all stray capacitances.

Figure 2-4 Common Crystal Connections

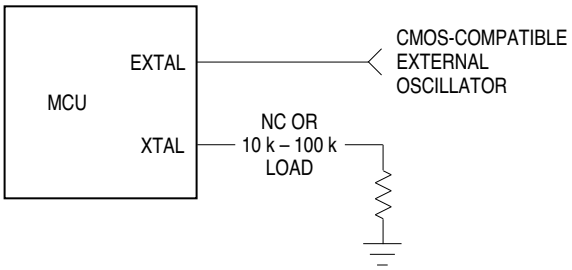
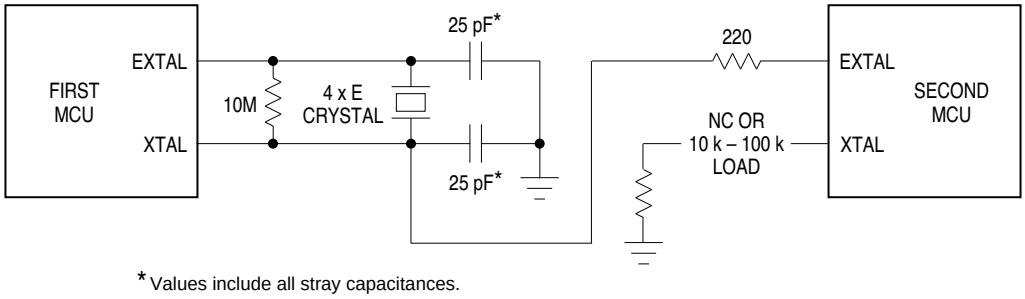


Figure 2-5 External Oscillator Connections



*Values include all stray capacitances.

Figure 2-6 One Crystal Driving Two MCUs

2.11.2 Port B

Port B is an 8-bit output-only port. In single-chip modes, port B pins are general-purpose output pins (PB[7:0]). In expanded modes, port B pins act as the high-order address lines (ADDR[15:8]) of the address bus.

PORTB can be read at any time. Reads of PORTB return the pin driver input level. If PORTB is written, the data is stored in internal latches. It drives the pins only in single-chip or bootstrap mode. In expanded operating modes, port B pins are the high-order address outputs (ADDR[15:8]).

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

2.11.3 Port C

Port C is an 8-bit general-purpose I/O port with a data register (PORTC) and a data direction register (DDRC). In single-chip modes, port C pins are general-purpose I/O pins (PC[7:0]). In expanded modes, port C pins are configured as data bus pins (DATA[7:0]).

PORTC can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If PORTC is written, the data is stored in internal latches. It drives the pins only if they are configured as outputs in single-chip or bootstrap mode. Port C pins are general-purpose inputs out of reset in single-chip and bootstrap modes. In expanded and test modes, these pins are data bus lines out of reset.

The CWOM control bit in the OPT2 register disables port C's P-channel output drivers. Because the N-channel driver is not affected by CWOM, setting CWOM causes port C to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTC bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port C bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port C can only be configured for wired-OR operation when the MCU is in single-chip or bootstrap modes.

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

2.11.4 Port D

Port D, a 6-bit general-purpose I/O port, has a data register (PORTD) and a data direction register (DDRD). The six port D lines (D[5:0]) can be used for general-purpose I/O, for the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems.

PORTD can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If PORTD is written, the data is stored in internal latches and can be driven only if port D is configured for general-purpose output.

The DWOM control bit in the SPCR register disables port D's P-channel output drivers. Because the N-channel driver is not affected by DWOM, setting DWOM causes port D to become an open-drain-type output port suitable for wired-OR operation. In wired-

3.1.6.3 Zero (Z)

The Z bit is set if the result of an arithmetic, logic, or data manipulation operation is zero. Otherwise, the Z bit is cleared. Compare instructions do an internal implied subtraction and the condition codes, including Z, reflect the results of that subtraction. A few operations (INX, DEX, INY, and DEY) affect the Z bit and no other condition flags. For these operations, only = and - conditions can be determined.

3.1.6.4 Negative (N)

The N bit is set if the result of an arithmetic, logic, or data manipulation operation is negative (MSB = 1). Otherwise, the N bit is cleared. A result is said to be negative if its most significant bit (MSB) is a one. A quick way to test whether the contents of a memory location has the MSB set is to load it into an accumulator and then check the status of the N bit.

3.1.6.5 Interrupt Mask (I)

The interrupt request (IRQ) mask (I bit) is a global mask that disables all maskable interrupt sources. While the I bit is set, interrupts can become pending, but the operation of the CPU continues uninterrupted until the I bit is cleared. After any reset, the I bit is set by default and can only be cleared by a software instruction. When an interrupt is recognized, the I bit is set after the registers are stacked, but before the interrupt vector is fetched. After the interrupt has been serviced, a return from interrupt instruction is normally executed, restoring the registers to the values that were present before the interrupt occurred. Normally, the I bit is zero after a return from interrupt is executed. Although the I bit can be cleared within an interrupt service routine, “nesting” interrupts in this way should only be done when there is a clear understanding of latency and of the arbitration mechanism. Refer to **SECTION 5 RESETS AND INTERRUPTS**.

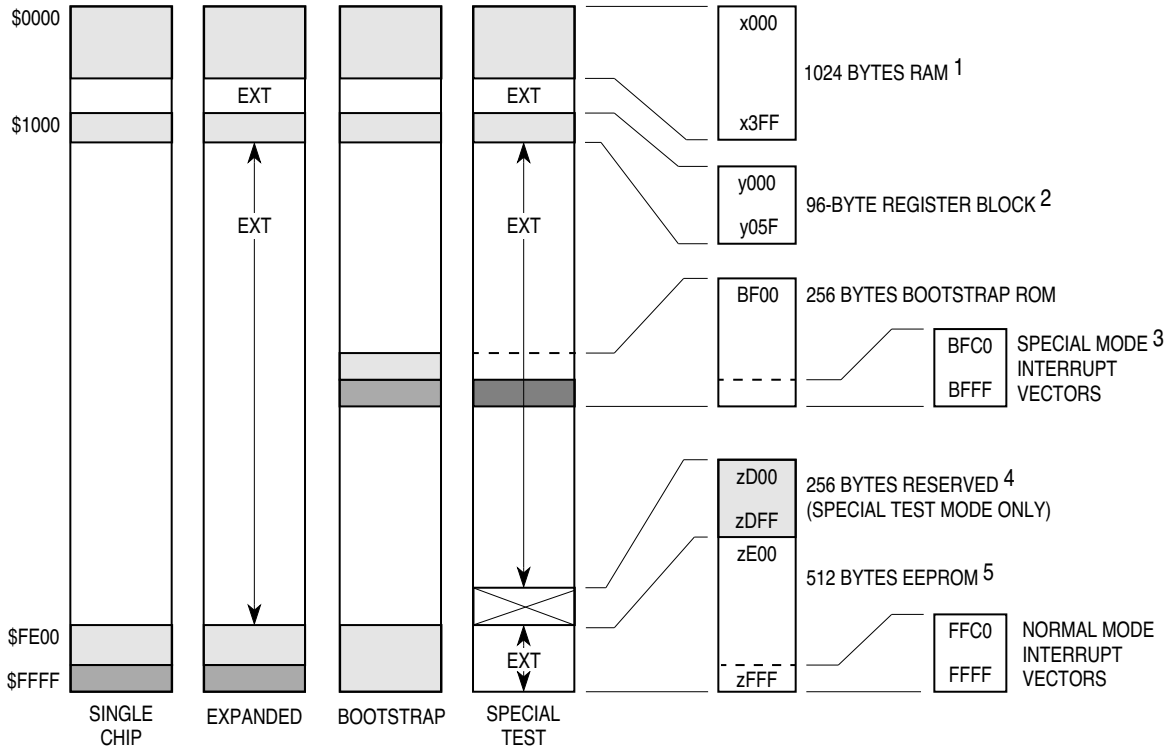
3.1.6.6 Half Carry (H)

The H bit is set when a carry occurs between bits 3 and 4 of the arithmetic logic unit during an ADD, ABA, or ADC instruction. Otherwise, the H bit is cleared. Half carry is used during BCD operations.

3.1.6.7 X Interrupt Mask (X)

The $\overline{\text{XIRQ}}$ mask (X) bit disables interrupts from the $\overline{\text{XIRQ}}$ pin. After any reset, X is set by default and must be cleared by a software instruction. When an $\overline{\text{XIRQ}}$ interrupt is recognized, the X and I bits are set after the registers are stacked, but before the interrupt vector is fetched. After the interrupt has been serviced, an RTI instruction is normally executed, causing the registers to be restored to the values that were present before the interrupt occurred. The X interrupt mask bit is set only by hardware ($\overline{\text{RESET}}$ or $\overline{\text{XIRQ}}$ acknowledge). X is cleared only by program instruction (TAP, where the associated bit of A is zero; or RTI, where bit 6 of the value loaded into the CCR from the stack has been cleared). There is no hardware action for clearing X.

4.2.2 Memory Map



NOTES:
1. RAM can be remapped to any 4-Kbyte boundary ($x000). "x" represents the value contained in RAM[3:0] in the init register.
2. The register block can be remapped to any 4-Kbyte boundary ($y000). "y" represents the value contained in reg[3:0] in the init register.
3. Special test mode vectors are externally addressed.
4. In special test mode the address locations $zD00–$zDFF are not externally addressable. "z" represents the value of bits EE[3:0] in the config register.
5. EEPROM can be remapped to any 4-Kbyte boundary ($z000). "z" represents the value contained in EE[3:0] in the config register.

Figure 4-1 MC68HC11F1 Memory Map

4.2.2.1 RAM

The MC68HC11F1 microcontroller has 1024 bytes of fully static RAM that can be used for storing instructions, variables, and temporary data during program execution. RAM can be placed at any 4-Kbyte boundary in the 64 Kbyte address space by writing an appropriate value to the INIT register.

RAM is initially located at $0000 in the memory map upon reset. Direct addressing mode can access the first 256 locations of RAM using a one-byte address operand. Direct mode accesses save program memory space and execution time.

The on-chip RAM is a fully static memory. RAM contents can be preserved during periods of processor inactivity by either of two methods, both of which reduce power consumption.

RAM[3:0] — RAM Map Position

These four bits, which specify the upper hexadecimal digit of the RAM address, control position of RAM in the memory map. RAM can be positioned at the beginning of any 4-Kbyte page in the memory map. Refer to **Table 4-5**.

REG[3:0] — 128-Byte Register Block Position

These four bits specify the upper hexadecimal digit of the address for the 128-byte block of internal registers. The register block is positioned at the beginning of any 4-Kbyte page in the memory map. Refer to **Table 4-5**.

Table 4-5 RAM and Register Mapping

RAM[3:0]	Location
0000	$0000–$03FF
0001	$1000–$13FF
0010	$2000–$23FF
0011	$3000–$33FF
0100	$4000–$43FF
0101	$5000–$53FF
0110	$6000–$63FF
0111	$7000–$73FF
1000	$8000–$83FF
1001	$9000–$93FF
1010	$A000–$A3FF
1011	$B000–$B3FF
1100	$C000–$C3FF
1101	$D000–$D3FF
1110	$E000–$E3FF
1111	$F000–$F3FF

REG[3:0]	Location
0000	$0000–$005F
0001	$1000–$105F
0010	$2000–$205F
0011	$3000–$305F
0100	$4000–$405F
0101	$5000–$505F
0110	$6000–$605F
0111	$7000–$705F
1000	$8000–$805F
1001	$9000–$905F
1010	$A000–$A05F
1011	$B000–$B05F
1100	$C000–$C05F
1101	$D000–$D05F
1110	$E000–$E05F
1111	$F000–$F05F

When the memory map has the 96-byte register block mapped at the same location as RAM, the registers have priority and the lower 96 bytes of RAM are inaccessible. No harmful conflicts occur due to a hardware resource priority scheme. On-chip registers have the highest priority of all on-chip resources, followed by on-chip RAM, bootstrap ROM, and on-chip EEPROM.

4.3.2.3 OPTION Register

The 8-bit special-purpose OPTION register sets internal system configuration options during initialization. In single-chip and expanded modes (SMOD = 0), IRQE, DLY, FCME, and CR[1:0] can be written only once and only in the first 64 cycles after a reset. This minimizes the possibility of any accidental changes to the system configuration. In special test and bootstrap modes (SMOD = 1), these bits can be written at any time.

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	FCME*	CR1*	CR0*
RESET:	0	0	0	0	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes.

SECTION 5 RESETS AND INTERRUPTS

Resets and interrupt operations load the program counter with a vector that points to a new location from which instructions are to be fetched. A reset causes the internal control registers to be initialized to a known state. The program counter is loaded with a known starting address and execution of instructions begins. An interrupt temporarily suspends normal program execution while an interrupt service routine is being executed. After an interrupt has been serviced, the main program resumes as if there had been no interruption.

5.1 Resets

There are four possible sources of reset. Power-on reset (POR) and external reset share the normal reset vector. The computer operating properly (COP) reset and the clock monitor reset each has its own vector.

5.1.1 Power-On Reset

A positive transition on V_{DD} generates a power-on reset (POR), which is used only for power-up conditions. POR cannot be used to detect drops in power supply voltages. A 4064 t_{cyc} (internal clock cycle) delay after the oscillator becomes active allows the clock generator to stabilize. If $\overline{\text{RESET}}$ is at logical zero at the end of 4064 t_{cyc}, the CPU remains in the reset condition until $\overline{\text{RESET}}$ goes to logical one.

It is important to protect the MCU during power transitions. To protect data in EEPROM, M68HC11 systems need an external circuit that holds the $\overline{\text{RESET}}$ pin low whenever V_{DD} is below the minimum operating level. This external voltage level detector, or other external reset circuits, are the usual source of reset in a system. The POR circuit only initializes internal circuitry during cold starts. Refer to Figure 2–3.

5.1.2 External Reset ($\overline{\text{RESET}}$)

The CPU distinguishes between internal and external reset conditions by sensing whether the reset pin rises to a logic one in less than two E-clock cycles after an internal device releases reset. When a reset condition is sensed, the $\overline{\text{RESET}}$ pin is driven low by an internal device for four E-clock cycles, then released. Two E-clock cycles later it is sampled. If the pin is still held low, the CPU assumes that an external reset has occurred. If the pin is high, it indicates that the reset was initiated internally by either the COP system or the clock monitor. It is not advisable to connect an external resistor capacitor (RC) power-up delay circuit to the reset pin of M68HC11 devices because the circuit charge time constant can cause the device to misinterpret the type of reset that occurred.

5.5.1 WAIT

The WAI opcode places the MCU in the WAIT condition, during which the CPU registers are stacked and CPU processing is suspended until a qualified interrupt is detected. The interrupt can be an external $\overline{\text{IRQ}}$, an $\overline{\text{XIRQ}}$, or any of the internally generated interrupts, such as the timer or serial interrupts. The on-chip crystal oscillator remains active throughout the WAIT standby period.

The reduction of power in the WAIT condition depends on how many internal clock signals driving on-chip peripheral functions can be shut down. The CPU is always shut down during WAIT. While in the wait state, the address/data bus repeatedly runs read cycles to the address where the CCR contents were stacked. Ensuring that the stack contents are placed in internal RAM will further reduce power consumption. The MCU leaves the wait state when it senses any interrupt that has not been masked.

The free-running timer system is shut down only if the I bit is set to one and the COP system is disabled by NOCOP being set to one. Several other systems can also be in a reduced power consumption state depending on the state of software-controlled configuration control bits. Power consumption by the analog-to-digital (A/D) converter is not affected significantly by the WAIT condition. However, the A/D converter current can be eliminated by writing the ADPU bit to zero. The SPI system is enabled or disabled by the SPE control bit. The SCI transmitter is enabled or disabled by the TE bit, and the SCI receiver is enabled or disabled by the RE bit. Therefore the power consumption in WAIT is dependent on the particular application.

5.5.2 STOP

Executing the STOP instruction while the S bit in the CCR is equal to zero places the MCU in the STOP condition. If the S bit is not zero, the STOP opcode is treated as a no-op (NOP). The STOP condition offers minimum power consumption because all clocks, including the crystal oscillator, are stopped while in this mode. To exit STOP and resume normal processing, a logic low level must be applied to one of the external interrupts ($\overline{\text{IRQ}}$ or $\overline{\text{XIRQ}}$) or to the $\overline{\text{RESET}}$ pin. A pending edge-triggered $\overline{\text{IRQ}}$ can also bring the CPU out of STOP.

Because all clocks are stopped in this mode, all internal peripheral functions also stop. The data in the internal RAM is retained as long as V_{DD} power is maintained. The CPU state and I/O pin levels are static and are unchanged by STOP. Therefore, when an interrupt restarts the system, the MCU resumes processing as if there were no interruption. If reset is used to restart the system a normal reset sequence results where all I/O pins and functions are also restored to their initial states.

To use the $\overline{\text{IRQ}}$ pin as a means of recovering from STOP, the I bit in the CCR must be clear ($\overline{\text{IRQ}}$ not masked). The $\overline{\text{XIRQ}}$ pin can be used to wake up the MCU from STOP regardless of the state of the X bit in the CCR, although the recovery sequence depends on the state of the X bit. If X is set to zero ($\overline{\text{XIRQ}}$ not masked), the MCU starts up, beginning with the stacking sequence leading to normal service of the $\overline{\text{XIRQ}}$ request. If X is set to one ($\overline{\text{XIRQ}}$ masked or inhibited), then processing continues with the instruction that immediately follows the STOP instruction, and no $\overline{\text{XIRQ}}$ interrupt service is requested or pending.

impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port C can only be configured for wired-OR operation when the MCU is in single-chip or bootstrap modes.

PORTC — Port C Data **$1006**

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	I	I	I	I	I	I	I	I
Expan. or Test:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

DDRC — Data Direction Register for Port C **$1007**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction for Port C
0 = Input
1 = Output

6.4 Port D

In all modes, port D bits [5:0] can be used either for general-purpose I/O, or with the SCI and SPI subsystems. During reset, port D pins are configured as high impedance inputs (DDRD bits cleared).

The DWOM control bit in the SPCR register disables port D's P-channel output drivers. Because the N-channel driver is not affected by DWOM, setting DWOM causes port D to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTD bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port D bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port D can be configured for wired-OR operation in any operating mode.

PORTD — Port D Data **$1008**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	I	I	I	I	I	I
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

PORTF — Port F Data **$1005**

	Bit 7	6	5	4	3	2	1	Bit 0
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
S. Chip or Boot:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

6.7 Port G

Port G pins reset to high-impedance inputs except in expanded modes where reset causes PG7 to become the $\overline{\text{CSPROG}}$ output. Alternate functions for port G bits [7:4] are chip select outputs. All port G bits are bidirectional and have corresponding data direction bits.

The GWOM control bit in the OPT2 register disables port G's P-channel output drivers. Because the N-channel driver is not affected by GWOM, setting GWOM causes port G to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTG bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port G bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port G can be configured for wired-OR operation in any operating mode.

PORTG — Port G Data **$1002**

	Bit 7	6	5	4	3	2	1	Bit 0
	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
RESET:	I	I	I	I	I	I	I	I
Alt. Pin Func.:	$\overline{\text{CSPROG}}$	CSGEN	CSIO1	CSIO2	—	—	—	—

DDRG — Data Direction Register for Port G **$1003**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0
RESET:	0	0	0	0	0	0	0	0

DDG[7:0] — Data Direction for Port G
0 = Input
1 = Output

6.8 System Configuration Options 2

The system configuration options 2 register controls several configuration parameters. Bit 6, CWOM, is the only bit in this register that directly affects parallel I/O.

OPT2 — System Configuration Options 2 **$1038**

	Bit 7	6	5	4	3	2	1	Bit 0
	GWOM	CWOM	CLK4X	—	—	—	—	—
RESET:	0	0	1	0	0	0	0	0

GWOM — Port G Wired-OR Mode
0 = Port G operates normally
1 = Port G outputs are open drain

CWOM — Port C Wired-OR Mode
0 = Port C operates normally
1 = Port C outputs are open drain

CLK4X — 4XOUT Clock Enable
Refer to **SECTION 2 PIN DESCRIPTIONS**.

Bits [4:0] — Not implemented
Always read zero

SECTION 8 SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI), an independent serial communications subsystem, allows the MCU to communicate synchronously with peripheral devices, such as transistor-transistor logic (TTL) shift registers, liquid crystal display (LCD) drivers, analog-to-digital converter subsystems, and other microprocessors. The SPI is also capable of inter-processor communication in a multiple master system. The SPI system can be configured as either a master or a slave device. When configured as a master, data transfer rates can be as high as one-half the E-clock rate (2.5 Mbits per second for a 5-MHz bus frequency). When configured as a slave, data transfers can be as fast as the E-clock rate (5 Mbits per second for a 5-MHz bus frequency).

8.1 Functional Description

The central element in the SPI system is the block containing the shift register and the read data buffer. The system is single buffered in the transmit direction and double buffered in the receive direction. This means that new data for transmission cannot be written to the shifter until the previous transfer is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition occurs. A single MCU register address is used for reading data from the read data buffer and for writing data to the shifter.

The SPI status block represents the SPI status flags (transfer complete, write collision, and mode fault) located in the SPI status register (SPSR). The SPI control block represents those functions that control the SPI system through the serial peripheral control register (SPCR).

Refer to **Figure 8-1**, which shows the SPI block diagram.

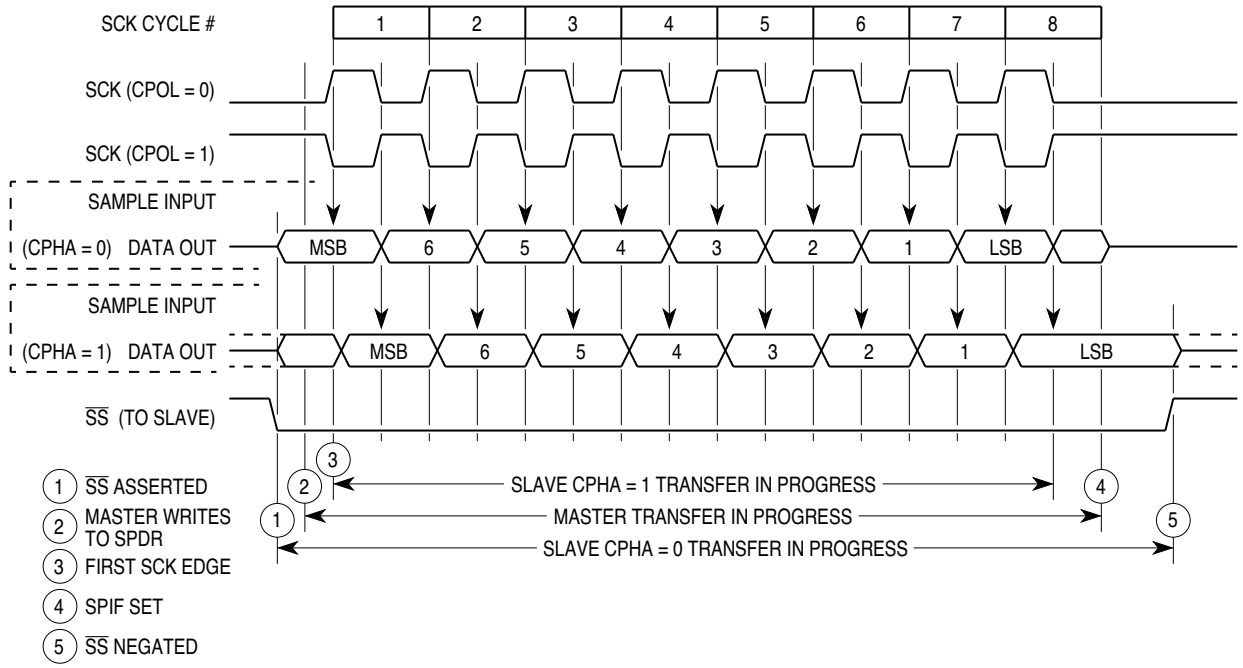


Figure 8-2 SPI Transfer Format

8.2.1 Clock Phase and Polarity Controls

Software can select one of four combinations of serial clock phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock, and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements.

When CPHA equals zero, the $\overline{SS}$ line must be negated and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while $\overline{SS}$ is low, a write collision error results.

When CPHA equals one, the $\overline{SS}$ line can remain low between successive transfers.

8.3 SPI Signals

The following paragraphs contain descriptions of the four SPI signals: master in slave out (MISO), master out slave in (MOSI), serial clock (SCK), and slave select ($\overline{SS}$).

Any SPI output line must have its corresponding data direction bit in DDRD register set. If the DDR bit is clear, that line is disconnected from the SPI logic and becomes a general-purpose input. All SPI input lines are forced to act as inputs regardless of the state of the corresponding DDR bits in DDRD register.

SECTION 9 TIMING SYSTEM

The M68HC11 timing system is composed of five clock divider chains. The main clock divider chain includes a 16-bit free-running counter, which is driven by a programmable prescaler. The main timer's programmable prescaler provides one of the four clocking rates to drive the 16-bit counter. Two prescaler control bits select the prescale rate.

The prescaler output divides the system clock by 1, 4, 8, or 16. Taps off of this main clocking chain drive circuitry that generates the slower clocks used by the pulse accumulator, the real-time interrupt (RTI), and the computer operating properly (COP) watchdog subsystems, also described in this section. Refer to **Figure 9-1**.

All main timer system activities are referenced to this free-running counter. The counter begins incrementing from $0000 as the MCU comes out of reset, and continues to the maximum count, $FFFF. At the maximum count, the counter rolls over to $0000, sets an overflow flag, and continues to increment. As long as the MCU is running in a normal operating mode, there is no way to reset, change, or interrupt the counting. The capture/compare subsystem features three input capture channels, four output compare channels, and one channel that can be selected to perform either input capture or output compare. Each of the three input capture functions has its own 16-bit input capture register (time capture latch) and each of the output compare functions has its own 16-bit compare register. All timer functions, including the timer overflow and RTI have their own interrupt controls and separate interrupt vectors.

The pulse accumulator contains an 8-bit counter and edge select logic. The pulse accumulator can operate in either event counting mode or gated time accumulation mode. During event counting mode, the pulse accumulator's 8-bit counter increments when a specified edge is detected on an input signal. During gated time accumulation mode, an internal clock source increments the 8-bit counter while an input signal has a predetermined logic level.

The real-time interrupt (RTI) is a programmable periodic interrupt circuit that permits pacing the execution of software routines by selecting one of four interrupt rates.

The COP watchdog clock input ($E \div 2^{15}$) is tapped off of the free-running counter chain. The COP automatically times out unless it is serviced within a specific time by a program reset sequence. If the COP is allowed to time out, a reset is generated, which drives the $\overline{\text{RESET}}$ pin low to reset the MCU and the external system. Refer to **Table 9-1** for crystal related frequencies and periods.

indicates when valid data is present in the result registers. The result registers are written during a portion of the system clock cycle when reads do not occur, so there is no conflict.

10.1.5 A/D Converter Clocks

The CSEL bit in the OPTION register selects whether the A/D converter uses the system E clock or an internal RC oscillator for synchronization. When the A/D system is operating with the MCU E clock, all switching and comparator functions are synchronized to the MCU clocks. This allows the comparator results to be sampled at relatively quiet clock times to minimize noise errors.

When E-clock frequency is below 750 kHz, charge leakage in the capacitor array can cause errors, and the internal oscillator should be used. The RC clock is asynchronous to the MCU internal E clock. Therefore, when the RC clock is used, additional errors can occur because the comparator is sensitive to the additional system clock noise.

10.1.6 Conversion Sequence

A/D converter operations are performed in sequences of four conversions each. A conversion sequence can repeat continuously or stop after one iteration. The conversion complete flag (CCF) is set after the fourth conversion in a sequence to show the availability of data in the result registers. **Figure 10-3** shows the timing of a typical sequence. Synchronization is referenced to the system E clock.

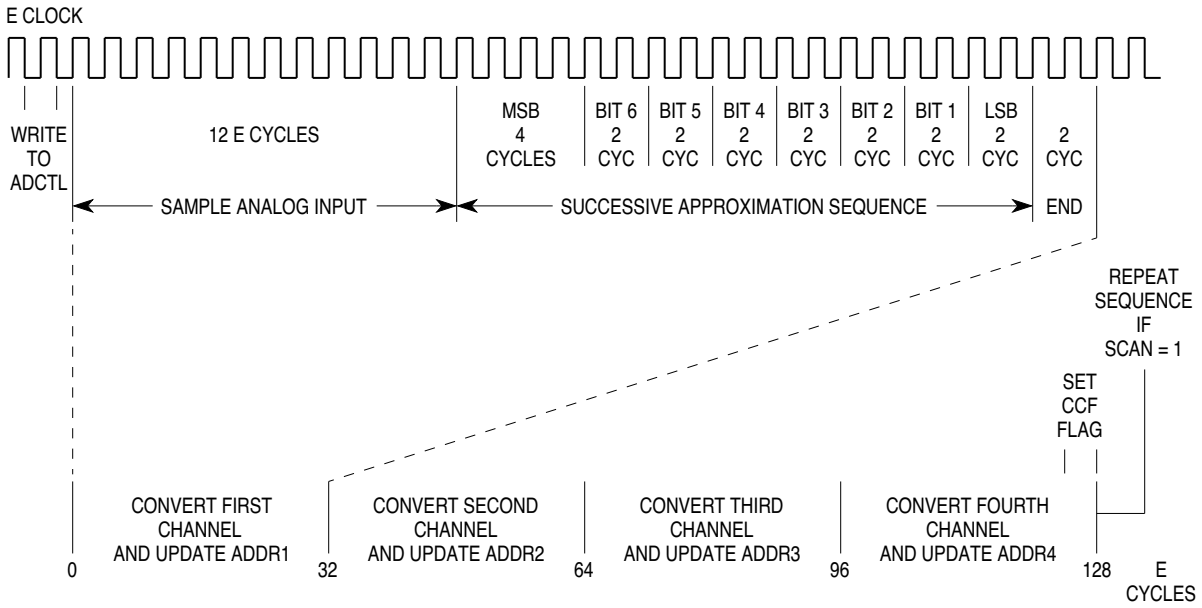


Figure 10-3 A/D Conversion Sequence

APPENDIX A ELECTRICAL CHARACTERISTICS

This appendix contains electrical parameters for the MC68HC11F1 microcontroller.

Table A-1 Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to + 7.0	V
Input Voltage	V_{in}	– 0.3 to + 7.0	V
Operating Temperature Range MC68HC11F1 MC68HC11F1C MC68HC11F1V MC68HC11F1M	T_A	T_L to T_H 0 to + 70 – 40 to + 85 – 40 to + 105 – 40 to + 125	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C
Current Drain per Pin* Excluding V_{DD}, V_{SS}, AV_{DD}, V_{RH}, and V_{RL}	I_D	25	mA

*One pin at a time, observing maximum power dissipation limits.

Internal circuitry protects the inputs against damage caused by high static voltages or electric fields; however, normal precautions are necessary to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Extended operation at the maximum ratings can adversely affect device reliability. Tying unused inputs to an appropriate logic voltage level (either GND or V_{DD}) enhances reliability of operation.

Table A-3 DC Electrical Characteristics

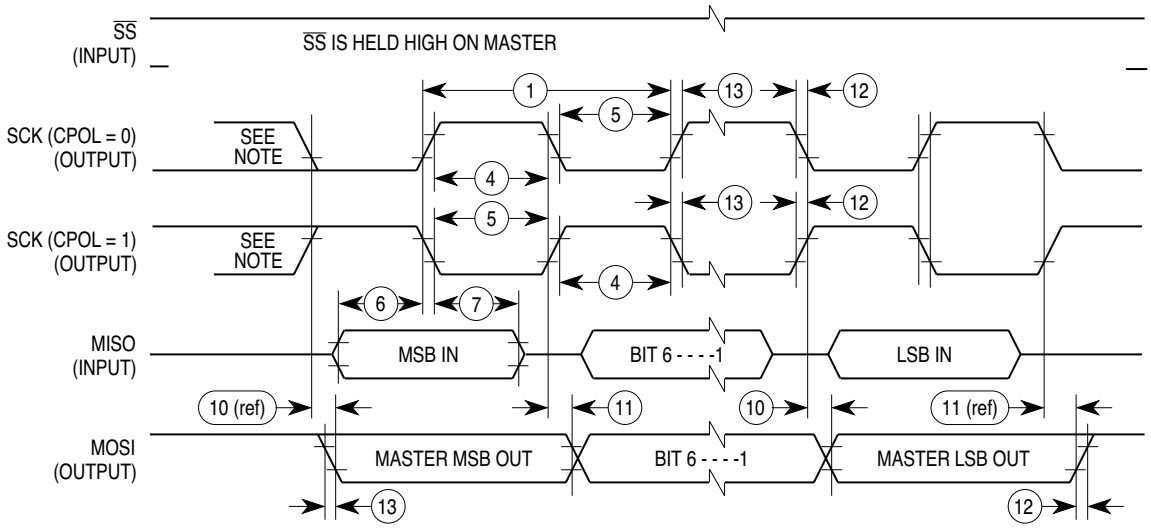
V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Output Voltage (Note 1) All Outputs except XTAL All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA I_{Load} = ± 10.0 µA	V_{OL} V_{OH}	— V_{DD} – 0.1	0.1 —	V V
Output High Voltage (Note 1) All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA I_{Load} = – 0.8 mA, V_{DD} = 4.5 V	V_{OH}	V_{DD} – 0.8	—	V
Output Low Voltage All Outputs Except XTAL I_{Load} = 1.6 mA	V_{OL}	—	0.4	V
Input High Voltage All Inputs Except $\overline{\text{RESET}}$ $\overline{\text{RESET}}$	V_{IH}	0.7 x V_{DD} 0.8 x V_{DD}	V_{DD} + 0.3 V_{DD} + 0.3	V V
Input Low Voltage All Inputs	V_{IL}	V_{SS} – 0.3	0.2 x V_{DD}	V
I/O Ports, Three-State Leakage Ports A, B, C, D, F, G $V_{in} = V_{IH}$ or V_{IL} MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	I_{OZ}	—	±10	µA
Input Leakage Current (Note 2) $V_{in} = V_{DD}$ or V_{SS} $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$ on standard devices $V_{in} = V_{DD}$ or V_{SS} MODB/V_{STBY}, $\overline{\text{XIRQ}}$ on EPROM devices	I_{in}	— —	±1 ±10	µA µA
Input Current with Pull-Up Resistors $V_{in} = V_{IL}$ Ports B, F, and G	I_{ipr}	100	500	µA
RAM Standby Voltage Power down	V_{SB}	4.0	V_{DD}	V
RAM Standby Current Power down	I_{SB}	—	20	µA
Input Capacitance PE[7:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$, EXTAL Ports A, B, C, D, F, G, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	C_{in}	— —	8 12	pF pF
Output Load Capacitance All Outputs Except PD[4:1], 4XOUT, XTAL, MODA/$\overline{\text{LIR}}$ PD[4:1] 4XOUT	C_L	— — —	90 200 30	pF pF pF

Characteristic	Symbol	2 MHz	3 MHz	4 MHz	Unit
Maximum Total Supply Current (Note 3) **RUN:** Expanded Mode	I_{DD} 27	 38	 50	 mA
WAIT: (All Peripheral Functions Shut Down) Expanded Mode	W_{IDD} 15	 20	 25	 mA
STOP: No Clocks, Expanded Mode	S_{IDD} 50	 50	 50	 µA
Maximum Power Dissipation Expanded Mode	P_D 149	 209	 275	 mW

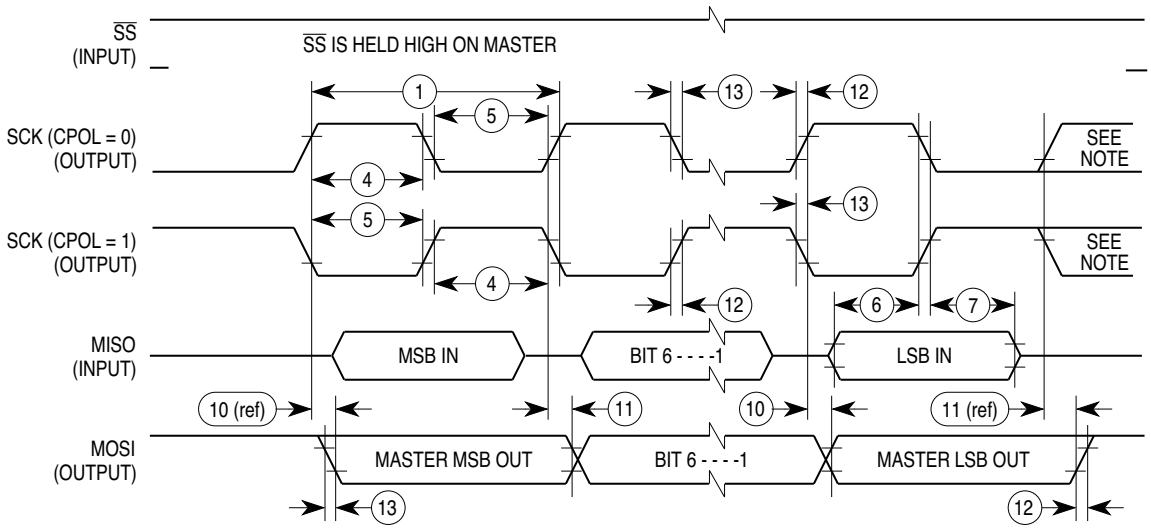
NOTES:

1. V_{OH} specification for $\overline{\text{RESET}}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
2. Refer to A/D specification for leakage current for port E.
3. EXTAL is driven with a square wave, and
   t_{cyc} = 500 ns for 2 MHz rating;
   t_{cyc} = 333 ns for 3 MHz rating;
   t_{cyc} = 250 ns for 4 MHz rating;
   $V_{IL} \le 0.2$ V; $V_{IH} \ge V_{DD} – 0.2$ V; No dc loads.



NOTE: This first clock edge is generated internally but is not seen at the SCK pin.

Figure A-10 SPI Master Timing (CPHA = 0)



NOTE: This last clock edge is generated internally but is not seen at the SCK pin.

Figure A-11 SPI Master Timing (CPHA = 1)

B.3 Ordering Information

Use the information in **Table B-1** to specify the appropriate device when placing an order.

Table B-1 Device Ordering Information

Description	Package	Temperature	Frequency	MC Order Number
NO ROM, 512 Bytes EEPROM, 1024 Bytes RAM	80-Pin LQFP (14 mm X 14 mm, 1.4 mm thick)	– 40° to + 85° C	2 MHz	MC68HC11F1CPU2
			3 MHz	MC68HC11F1CPU3
			4 MHz	MC68HC11F1CPU4
		– 40° to + 105° C	2 MHz	MC68HC11F1VPU2
			3 MHz	MC68HC11F1VPU3
			4 MHz	MC68HC11F1VPU4
		– 40° to + 125° C	2 MHz	MC68HC11F1MPU2
			3 MHz	MC68HC11F1MPU3
	68-Pin PLCC	– 40° to + 85° C	2 MHz	MC68HC11F1CFN2
			3 MHz	MC68HC11F1CFN3
			4 MHz	MC68HC11F1CFN4
		– 40° to + 105° C	2 MHz	MC68HC11F1VFN2
			3 MHz	MC68HC11F1VFN3
			4 MHz	MC68HC11F1VFN4
		– 40° to + 125° C	2 MHz	MC68HC11F1MFN2
			3 MHz	MC68HC11F1MFN3