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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21312-24pvxa

Contents

PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, as illustrated in the "Logic Block Diagram" on page 1, comprises of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow all the device resources to be combined into a complete custom system. Each CY8C21x12 device includes one limited digital block and one CapSense block. Depending on the PSoC package, up to 24 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep, and watchdog timers, and an internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability, such as digital clocks for increased flexibility, I^2C functionality for implementing an I^2C master, slave, or multi-master, an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems, and various system resets supported by the M8C.

The Digital System is composed of a programmable limited digital block and fixed-function digital resources inside the CapSense block. The limited digital block can be configured into a number of digital peripherals. The fixed-function digital resources in the CapSense block provide external modulation signals, measurement timing, and measurement conversion. The digital resources can be connected to the GPIO through a series of global buses that provide very flexible routing options.

The Analog System is composed of a comparator and a filter that are used in the CapSense block to implement capacitive sensing measurement.

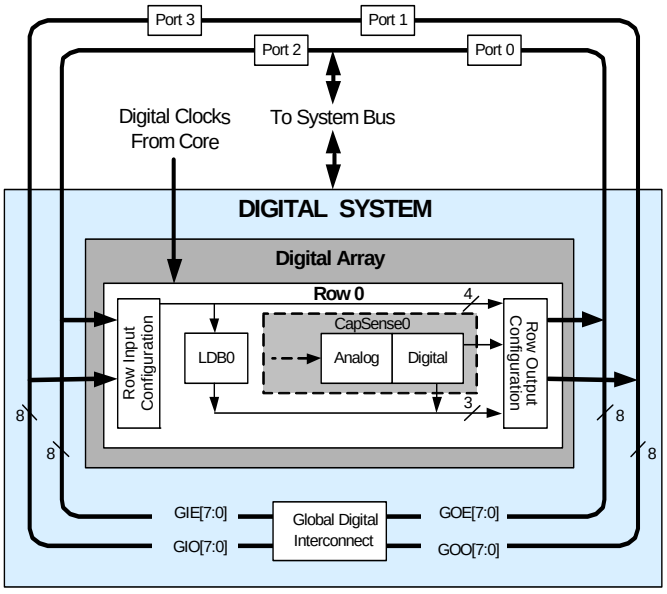
The Digital System

The Digital System is composed of one digital block. This block is an 8-bit resource that can implement various 8-bit digital peripherals. Digital peripheral configurations include those listed.

- PWM (8-bit)
- Counter (8-bit)
- Timer (8-bit)
- Half-duplex 8-bit UART with selectable parity
- SPI slave
- I^2C master, slave, or multi-master (implemented in a dedicated I^2C block)

The digital block can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Figure 1. Digital System Block Diagram

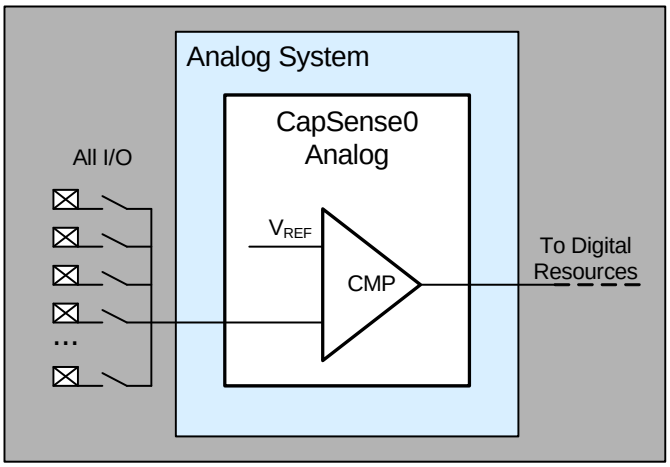


The Analog System

The Analog System is composed of analog resources inside of the CapSense block. These resources are used to implement a flexible capacitive sensing and measurement module. The analog resources in the CapSense block are listed.

- Comparator used in capacitance-to-digital conversion
- Fixed, absolute reference or adjustable, ratiometric reference can be used with the comparator
- Low-pass filter converts a digital bit stream into the adjustable, ratiometric analog reference

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system. Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combination.

Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful for complete systems. Brief statements describing the merits of each system resource are presented.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems.
- The I^2C module provides communication up to 400 kHz over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system.
- Versatile analog multiplexer system.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in Table 1

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66[1]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[2]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94[1]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A[1]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45[1]	up to 38	2	8	up to 38	0	4	6[2]	1 K	16 K
CY8C21x45[1]	up to 24	1	4	up to 24	0	4	6[2]	512	8 K
CY8C21x34[1]	up to 28	1	4	28	0	2	4[2]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[2]	256	4 K
CY8C21x12[1]	up to 24	1	1[2]	24	0	0	1[2]	512	8 K
CY8C20x34[1]	up to 28	0	0	up to 28	0	0	3[2,3]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[2,3]	up to 2 K	up to 32 K

Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Notes
1. Automotive qualified devices available in this group.
2. Limited analog functionality.
3. Two analog blocks and one CapSense® block.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Table 5. Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D			DD	
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
CSCNT_CR1	20	RW	CSCLK_CR0	60	RW		A0		OSC_CR0	E0	RW
CSCNT_CR2	21	RW	CSCLK_CR1	61	RW		A1		OSC_CR1	E1	RW
CSCNT_CR3	22	RW		62			A2		OSC_CR2	E2	RW
	23		CSREF_CR2	63	RW		A3		VLT_CR	E3	RW
CSMOD0_CR1	24	RW	CSCMP_CR7	64	RW		A4		VLT_CMP	E4	R
CSMOD0_CR2	25	RW		65			A5			E5	
CSMOD0_CR3	26	RW	CSREF_CR3	66	RW		A6		CSREF_CR4	E6	RW
	27		CSCMP_CR8	67	RW		A7			E7	
CSMOD1_CR1	28	RW		68			A8		IMO_TR	E8	W
CSMOD1_CR2	29	RW		69			A9		ILO_TR	E9	W
CSMOD1_CR3	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CSCLK_CR2	6B	RW		AB		ECO_TR	EB	W
LDB0_FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
LDB0_IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
LDB0_OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32			72		RDI0IS	B2	RW		F2	
	33			73		RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36			76		RDI0RO1	B6	RW		F6	
	37			77			B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of theCY8C21x12 PSoC device. For the most up-to-date electrical specifications, visit the Cypress website at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C as specified, except where noted. Refer to Table 12 on page 18 for the electrical specifications for the IMO using slow IMO (SLIMO) mode.

Figure 5. Voltage versus CPU Frequency

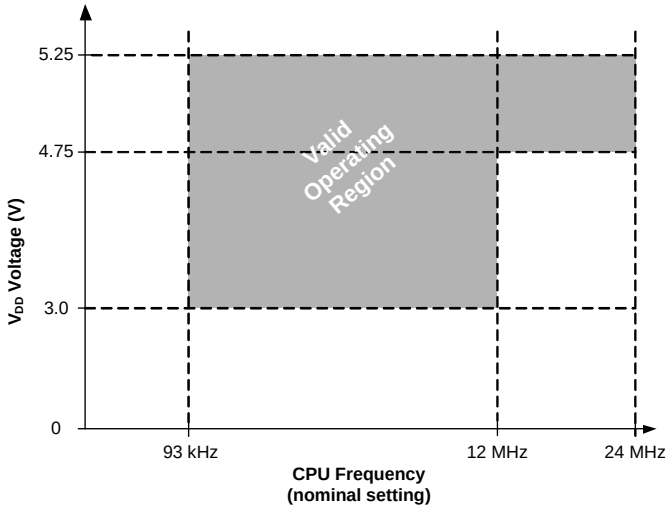
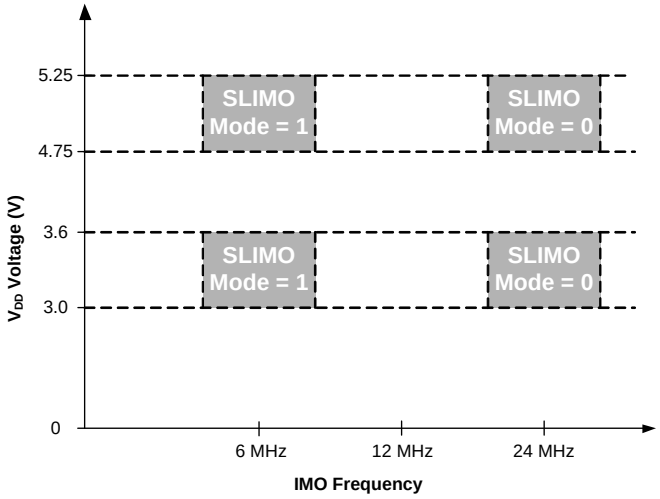


Figure 6. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the $Flash_{DR}$ electrical specification in Table 11 on page 17.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 24. The user must limit the power consumption to comply with this requirement.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 11. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[8, 9]	1,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total)[9, 10]	128,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash data retention	15	–	–	Years	

Notes

8. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

These comparator electrical specifications apply to the comparator in the CapSense block.

Table 14. AC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Response time, 50 mV overdrive	–	75	100	ns	

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 15. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Input clock frequency					
	No capture, $V_{DD} \geq 4.75$ V	–	–	50.4[15]	MHz	
	No capture, $V_{DD} < 4.75$ V	–	–	25.2[15]	MHz	
	With capture	–	–	25.2[15]	MHz	
	Capture pulse width	50[14]	–	–	ns	
Counter	Input clock frequency					
	No enable input, $V_{DD} \geq 4.75$ V	–	–	50.4[15]	MHz	
	No enable input, $V_{DD} < 4.75$ V	–	–	25.2[15]	MHz	
	With enable input	–	–	25.2[15]	MHz	
	Enable input pulse width	50[14]	–	–	ns	
SPIS	Input clock (SCLK) frequency	–	–	4.2[15]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated between transmissions	50[14]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	50.4[15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	25.2[15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2[15]	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	50.4[15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	25.2[15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2[15]	MHz	

Notes
14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).
15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

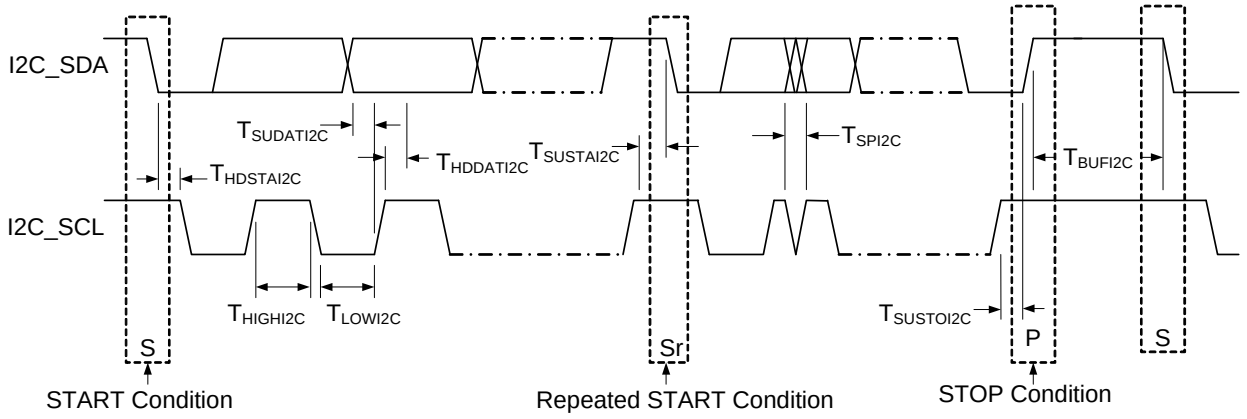
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 19. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100[17]	0	400[17]	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	100[18]	–	ns	
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 8. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

17. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly
18. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the CY8C21x12 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Packaging Dimensions

Figure 9. 20-Pin (210-Mil) SSOP

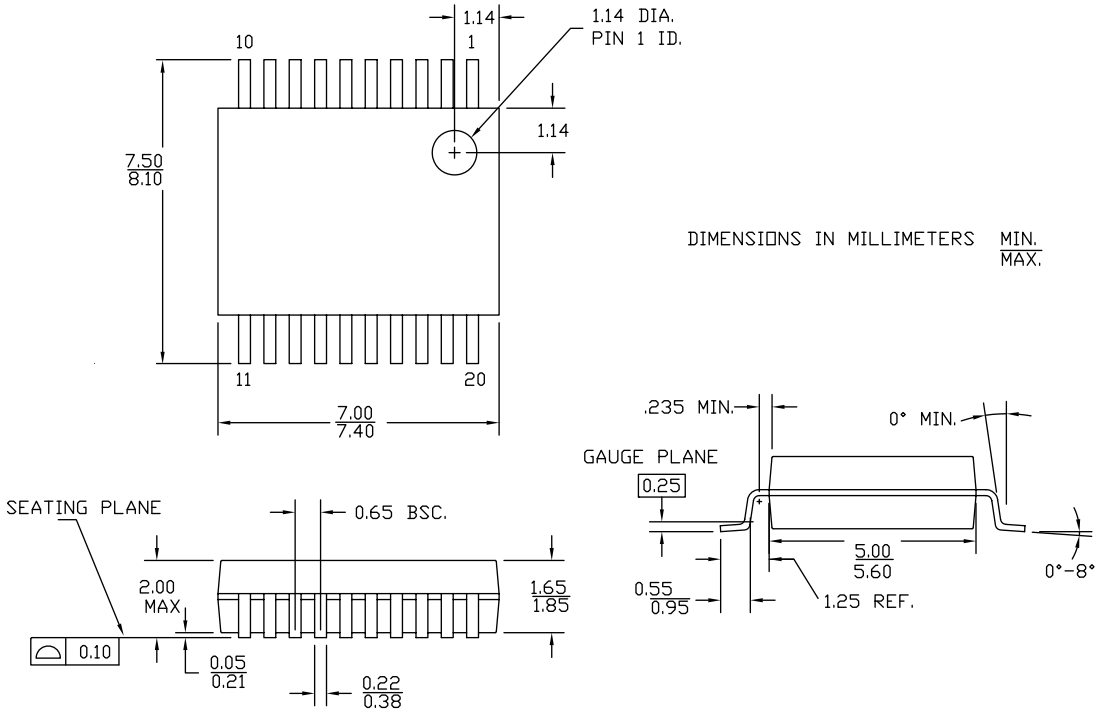


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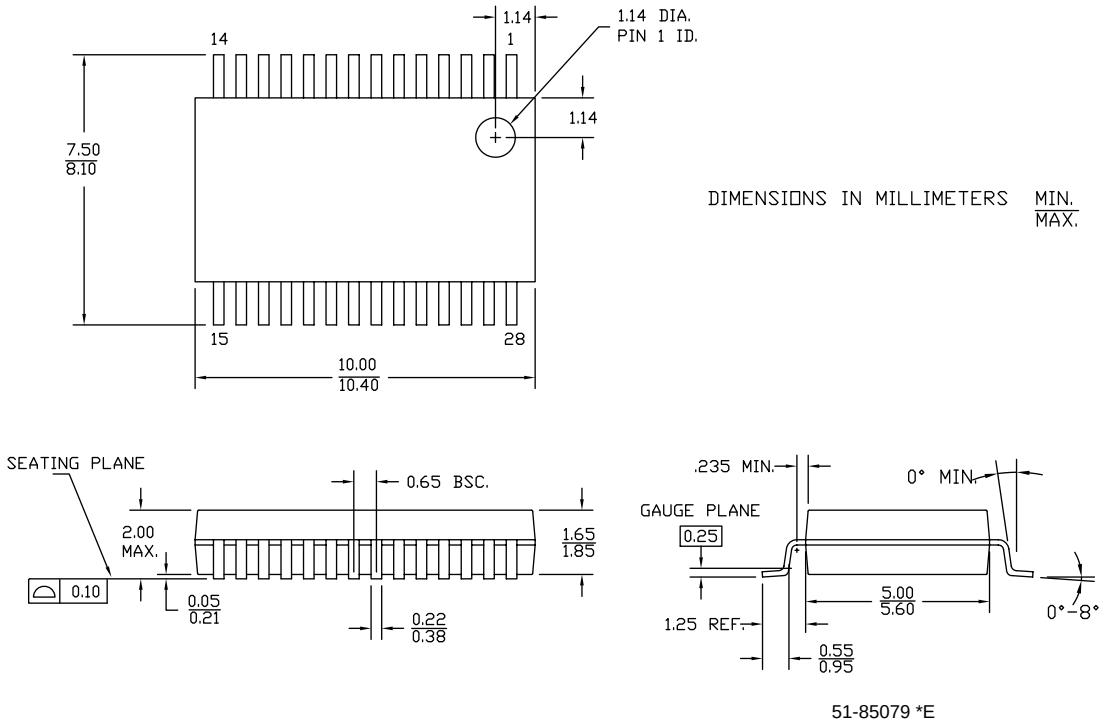
Figure 10. 28-Pin (210-Mil) SSOP



Thermal Impedances

Table 20. Thermal Impedances per Package

Package	Typical θ_{JA} [19]	Typical θ_{JC}
20-Pin SSOP	117 °C/W	41 °C/W
28-Pin SSOP	96 °C/W	39 °C/W

Solder Reflow Specifications

Table 21 shows the solder reflow temperature limits that must not be exceeded.

Table 21. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
20-Pin SSOP	260 °C	30 seconds
28-Pin SSOP	260 °C	30 seconds

Note
19. $T_J = T_A + \text{Power} \times \theta_{JA}$

Development Tool Selection

This section presents the development tools available for the CY8C21x12 family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up-to-date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface allows you to run, halt, and single step the processor, and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube unit
- 28-Pin PDIP emulation pod for CY8C29466-24PXI
- Two 28-Pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC designer software CD
- ISSP cable
- MiniEval socket programming and evaluation board
- Backward compatibility cable (for connecting to legacy pods)
- Universal 110/220 power supply (12 V)
- European plug adapter
- USB 2.0 cable
- Getting Started guide
- Development kit registration form

CY3280-BK1

The CY3280-BK1 Universal CapSense Control Kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The kit comes with a control boards for CY8C20x34 and CY8C21x34 devices as well as a breadboard module and a button(5)/slider module.

The CY8C21x34 on-chip debugger device that is part of this kit is capable of emulating CY8C21x12 devices as well. Therefore, this kit can be used to evaluate and develop projects for CY8C21x12 devices.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-Pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-21X34 Evaluation Pod (EvalPod)

The CY3210-21X34 PSoC EvalPods are pods that connect to the ICE in-circuit emulator (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-21X34 provides evaluation of the CY8C21x34 PSoC device family.

The CY8C21x34 on-chip debugger device that is part of this kit is capable of emulating CY8C21x12 devices as well. Therefore, this kit can be used to evaluate CY8C21x12 devices.

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3217-MiniProg1

The CY3217-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg1 programmer
- USB A to Mini B cable
- CY3217-MiniProg1 kit CD, which has kit documents, PSoC Designer and PSoC Programmer installation files
- Getting Started Guide

Accessories (Emulation and Programming)

Table 23. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit[20]	Foot Kit[21]	Adapter[22]
CY8C21312-24PVXA	20-Pin SSOP	CY3250-21X34	CY3250-20SSOP-FK	Adapters are available at http://www.emulation.com.
CY8C21512-24PVXA	28-Pin SSOP	CY3250-21X34	CY3250-28SSOP-FK	

Notes
20. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
21. Foot kit includes surface mount feet that can be soldered to the target PCB.
22. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are available at http://www.emulation.com.

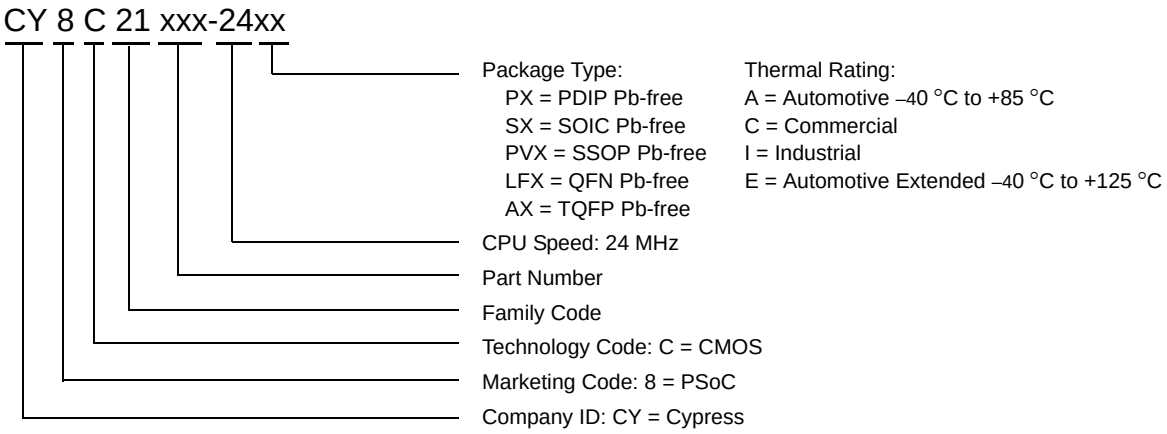
Ordering Information

The following table lists theCY8C21x12 PSoC device's key package features and ordering codes.

Table 24. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Limited Digital Blocks	CapSense Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
20-Pin (210-Mil) SSOP	CY8C21312-24PVXA	8 K	512	–40 °C to +85 °C	1	1	16	16	0	Yes
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21312-24PVXAT	8 K	512	–40 °C to +85 °C	1	1	16	16	0	Yes
28-Pin (210-Mil) SSOP	CY8C21512-24PVXA	8 K	512	–40 °C to +85 °C	1	1	24	24	0	Yes
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21512-24PVXAT	8 K	512	–40 °C to +85 °C	1	1	24	24	0	Yes

Ordering Code Definitions



Glossary *(continued)*

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
flash block	The smallest amount of flash ROM space that may be programmed at one time and the smallest amount of flash space that may be protected.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at the V_{DD} suppy voltage and pulled high with resistors. The bus operates up to100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the CPU receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.

Document History Page

Document Title: CY8C21312, CY8C21512, Automotive PSoC® Programmable System-on-Chip™ Document Number: 001-63745				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3023789	BTK / AESA	09/06/2010	New data sheet.
*A	3094401	BTK	11/23/2010	Added tape and reel packaging information. Refer to CDT 88767.
*B	3157903	BTK / NJF	01/31/2011	Updated I2C timing diagram to improve clarity (CDT 92817). Updated wording, formatting, and notes of the AC Digital Block Specifications table to improve clarify (CDT 92819). Added V_{DDP}, V_{DDLV}, and V_{DDHV} electrical specifications to give more information for programming the device (CDT 92822). Updated solder reflow temperature specifications to give more clarity (CDT 92828). Updated the jitter specifications (CDT 92831). Updated PSoC Device Characteristics table (CDT 92832). Updated the F_{32KU} electrical specification (CDT 92994). Updated DC POR and LVD Specifications to add specs for all POR levels (CDT 86716). Updated note for R_{PD} electrical specification (CDT 90944). Updated Reference Information Section. Package diagram spec 51-51100 revised from *A to *B. Updated note for the T_{STG} electrical specification to add more clarity (CDT 82750).
*C	4111812	JICG	09/02/2013	Updated Packaging Information: spec 51-85077 – Changed revision from *D to *E. spec 51-85079 – Changed revision from *D to *E. Updated Tape and Reel Information: spec 51-51101 – Changed revision from *A to *C. spec 51-51100 – Changed revision from *B to *C. Updated Development Tool Selection Updated Device Programmers: Removed the section “CY3207ISSP In-System Serial Programmer (ISSP)”. Updated the template. Sunset review.
*D	4560572	SNPR	11/04/2014	Replaced CY3210-MiniProg1 with CY3217-MiniProg1 in the Device Programmers section. Changed Tape and Reel Information spec 51-51100 revision from *C to *D.

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