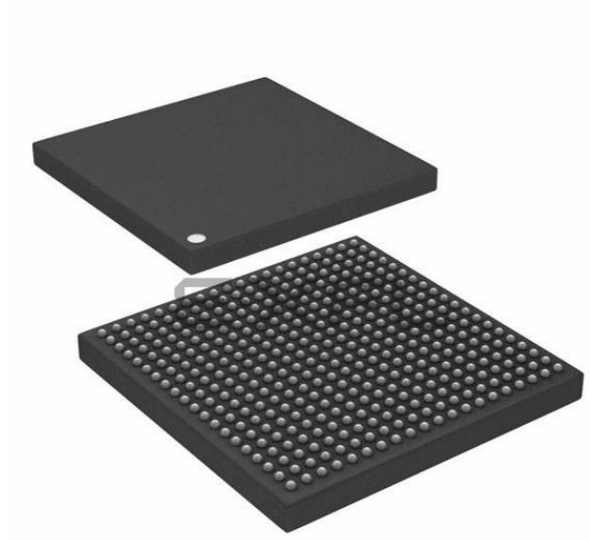

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, I²C, UART
Clock Rate	266MHz
Non-Volatile Memory	ROM (8kB)
On-Chip RAM	208kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc7112vm1000

Bottom View

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	NC	NC	NC	GND	HD0	HD1	HD4	HD6	HD7	HD10	HD12	HD15	$\overline{CK}$	CK	DQS2	DQM1	GND	GND
B	NC	NC	NC	NC	NC	NC	NC	HD2	HD5	HD8	HD11	HD14	$\overline{WE}$	CKE	DQS0	DQS3	DQM2	$\overline{CS0}$	NC	V_{DDM}
C	NC	NC	NC	NC	NC	NC	NC	NC	HD3	HD9	HD13	$\overline{CAS}$	$\overline{RAS}$	DQS1	DQM0	DQM3	$\overline{CS1}$	D25	D30	D24
D	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	GND	D27	D28	V_{DDM}
E	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	V_{DDM}	D31	D26	GND
F	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DD}	V_{DD}	V_{DD}	D29	D15	V_{DDM}
G	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	GND	D13	GND
H	HA1	HA2	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D11	D12	D14
J	$\overline{HREQ}$	$\overline{HACK}$	HA3	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D9	V_{DDM}	D10
K	$\overline{HDS}$	HDDS	HA0	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D8	GND	D0
L	HRW	$\overline{HCS1}$	$\overline{HCS2}$	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D3	GND	D1
M	URXD	UTXD	SDA	V_{DD}	V_{DD}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D5	V_{DDM}	D2
N	V_{SSPLL}	SCL	CLKIN	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{REF}	D6	D4
P	V_{DDPLL}	TPSEL	$\overline{PORESET}$	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D16	D17	D7
R	TEST0	EE0	TDO	V_{DD}	V_{DDIO}	V_{DDIO}	GND	V_{DDIO}	GND	GND	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	V_{DDM}	V_{DDM}	D18	D19	GND
T	$\overline{HRESET}$	TMS	NC	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	D22	D20	V_{DDM}
U	$\overline{TRST}$	TCK	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	D23	D21	GND
V	TDI	NC	GPIA24	GPIA22	GPID6	GPIA28	T1TD	T1RFS	T0TCK	EVNT4	EVNT0	NC	BA0	A2	A5	A10	A11	A13	NC	V_{DDM}
W	H8BIT	GPIA26	GPIA23	GPIA19	GPIA27	GDPD4	T1TFS	T1RD	T0TFS	T0RFS	EVNT2	EVNT1	NC	A3	A6	A7	A8	A12	V_{DDM}	GND
Y	GPIA25	GND	GPIA21	GPIA20	GPID5	GPIA29	T1TCK	T1RCK	TOTD	T0RD	T0RCK	EVNT3	$\overline{NMI}$	BA1	A4	A0	A1	A9	GND	V_{DDM}

Figure 3. MSC7112 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

1.2 Signal List By Ball Location

Table 1 lists the signals sorted by ball number and configuration.

Table 1. MSC7112 Signals by Ball Designator

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
A1	GND					
A2	GND					
A3	DQM1					
A4	DQS2					
A5	CK					
A6	$\overline{CK}$					
A7	GPIC7			GPOC7	HD15	
A8	GPIC4			GPOC4	HD12	
A9	GPIC2			GPOC2	HD10	
A10	reserved				HD7	
A11	reserved				HD6	
A12	reserved				HD4	
A13	reserved				HD1	
A14	reserved				HD0	
A15	GND					
A16 (1L44X)	NC					
A16 (1M88B)	BM3	GPID8		GPOD7	reserved	
A17	NC					
A18	NC					
A19	NC					
A20	NC					
B1	V_{DDM}					
B2	NC					
B3	$\overline{CS0}$					
B4	DQM2					
B5	DQS3					
B6	DQS0					
B7	CKE					
B8	$\overline{WE}$					
B9	GPIC6			GPOC6	HD14	
B10	GPIC3			GPOC3	HD11	
B11	GPIC0			GPOC0	HD8	
B12	reserved				HD5	
B13	reserved				HD2	
B14	NC					
B15 (1L44X)	NC					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D13	V_{DDIO}					
D14	V_{DDIO}					
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H9	GND					
H10	GND					
H11	GND					
H12	GND					
H13	GND					
H14	GND					
H15	V_{DDIO}					
H16	V_{DDIO}					
H17	V_{DDC}					
H18	NC					
H19	reserved				HA2	
H20	reserved				HA1	
J1	D10					
J2	V_{DDM}					
J3	D9					
J4	V_{DDM}					
J5	V_{DDM}					
J6	V_{DDM}					
J7	GND					
J8	GND					
J9	GND					
J10	GND					
J11	GND					
J12	GND					
J13	GND					
J14	GND					
J15	GND					
J16	V_{DDIO}					
J17	V_{DDC}					
J18 (1L44X)	reserved				HA3	
J18 (1M88B)	GPIC11			GPOC11	HA3	
J19	reserved				$\overline{\text{HACK}}$/HACK or $\overline{\text{HRRQ}}$/HRRQ	
J20	HDSP	reserved			$\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ	
K1	D0					
K2	GND					
K3	D8					
K4	V_{DDC}					
K5	V_{DDM}					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
K6	GND					
K7	GND					
K8	GND					
K9	GND					
K10	GND					
K11	GND					
K12	GND					
K13	GND					
K14	GND					
K15	V_{DDIO}					
K16	V_{DDIO}					
K17	V_{DDC}					
K18	reserved				HA0	
K19	reserved				HDDS	
K20	reserved				$\overline{\text{HDS}}$/HDS or $\overline{\text{HWR}}$/HWR	
L1	D1					
L2	GND					
L3	D3					
L4	V_{DDC}					
L5	V_{DDM}					
L6	GND					
L7	GND					
L8	GND					
L9	GND					
L10	GND					
L11	GND					
L12	GND					
L13	GND					
L14	V_{DDIO}					
L15	V_{DDIO}					
L16	V_{DDIO}					
L17	V_{DDC}					
L18 (1L44X)	reserved				$\overline{\text{HCS2}}$/HCS2	
L18 (1M88B)	GPIB11			GPOB11	$\overline{\text{HCS2}}$/HCS2	
L19	reserved				$\overline{\text{HCS1}}$/HCS1	
L20	reserved				HRW or $\overline{\text{HRD}}$/HRD	
M1	D2					
M2	V_{DDM}					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
M3	V_{DDM}					
M4	V_{DDM}					
M5	V_{DDM}					
M6	GND					
M7	GND					
M8	GND					
M9	GND					
M10	GND					
M11	GND					
M12	GND					
M13	GND					
M14	GND					
M15	GND					
M16	V_{DDC}					
M17	V_{DDC}					
M18	GPIA14		$\overline{IRQ15}$		GPOA14	SDA
M19	GPIA12		$\overline{IRQ3}$		GPOA12	UTXD
M20	GPIA13		$\overline{IRQ2}$		GPOA13	URXD
N1	D4					
N2	D6					
N3	V_{REF}					
N4	V_{DDM}					
N5	V_{DDM}					
N6	V_{DDM}					
N7	GND					
N8	GND					
N9	GND					
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$		GPOA15	SCL
N20	V_{SSPLL}					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
P1	D7					
P2	D17					
P3	D16					
P4	V_{DDM}					
P5	V_{DDM}					
P6	V_{DDM}					
P7	GND					
P8	GND					
P9	GND					
P10	GND					
P11	GND					
P12	GND					
P13	GND					
P14	GND					
P15	V_{DDIO}					
P16	V_{DDIO}					
P17	V_{DDC}					
P18	$\overline{\text{PORESET}}$					
P19	TPSEL					
P20	V_{DDPLL}					
R1	GND					
R2	D19					
R3	D18					
R4	V_{DDM}					
R5	V_{DDM}					
R6	V_{DDM}					
R7	GND					
R8	V_{DDM}					
R9	GND					
R10	V_{DDM}					
R11	GND					
R12	GND					
R13	V_{DDIO}					
R14	GND					
R15	V_{DDIO}					
R16	V_{DDIO}					
R17	V_{DDC}					
R18	TDO					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
U17	V_{DDC}					
U18	NC					
U19	TCK					
U20	$\overline{\text{TRST}}$					
V1	V_{DDM}					
V2	NC					
V3	A13					
V4	A11					
V5	A10					
V6	A5					
V7	A2					
V8	BA0					
V9	NC					
V10	reserved				EVNT0	
V11	SWTE	GPIA16	$\overline{\text{IRQ12}}$	GPOA16	EVNT4	
V12	GPIA8		$\overline{\text{IRQ6}}$	GPOA8	T0TCK	
V13	GPIA4		$\overline{\text{IRQ1}}$	GPOA4	T1RFS	
V14	GPIA0		$\overline{\text{IRQ11}}$	GPOA0	T1TD	
V15	GPIA28		$\overline{\text{IRQ17}}$	GPOA28	reserved	reserved
V16	GPID6			GPOD6	reserved	reserved
V17	GPIA22		$\overline{\text{IRQ22}}$	GPOA22	reserved	
V18	GPIA24		$\overline{\text{IRQ24}}$	GPOA24	reserved	
V19	NC					
V20	TDI					
W1	GND					
W2	V_{DDM}					
W3	A12					
W4	A8					
W5	A7					
W6	A6					
W7	A3					
W8	NC					
W9	GPIA17		$\overline{\text{IRQ13}}$	GPOA17	EVNT1	CLKO
W10	BM0	GPIC14		GPOC14	EVNT2	
W11	GPIA10		$\overline{\text{IRQ5}}$	GPOA10	T0RFS	
W12	GPIA7		$\overline{\text{IRQ7}}$	GPOA7	T0TFS	
W13	GPIA3		$\overline{\text{IRQ8}}$	GPOA3	T1RD	
W14	GPIA1		$\overline{\text{IRQ10}}$	GPOA1	T1TFS	

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.14 to 1.26	V
Memory supply voltage	V_{DDM}	2.38 to 2.63	V
PLL supply voltage	V_{DDPLL}	1.14 to 1.26	V
I/O supply voltage	V_{DDIO}	3.14 to 3.47	V
Reference voltage	V_{REF}	1.19 to 1.31	V
Operating temperature range	T_J T_A	maximum: 105 minimum: –40	°C °C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC7112 for the MAP-BGA package.

Table 4. Thermal Characteristics for MAP-BGA Package

Characteristic	Symbol	MAP-BGA 17 × 17 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	39	31	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	23	20	°C/W
Junction-to-board[4]	$R_{\theta JB}$	12		°C/W
Junction-to-case[5]	$R_{\theta JC}$	7		°C/W
Junction-to-package-top[6]	Ψ_{JT}	2		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.1, *Thermal Design Considerations* explains these characteristics in detail.

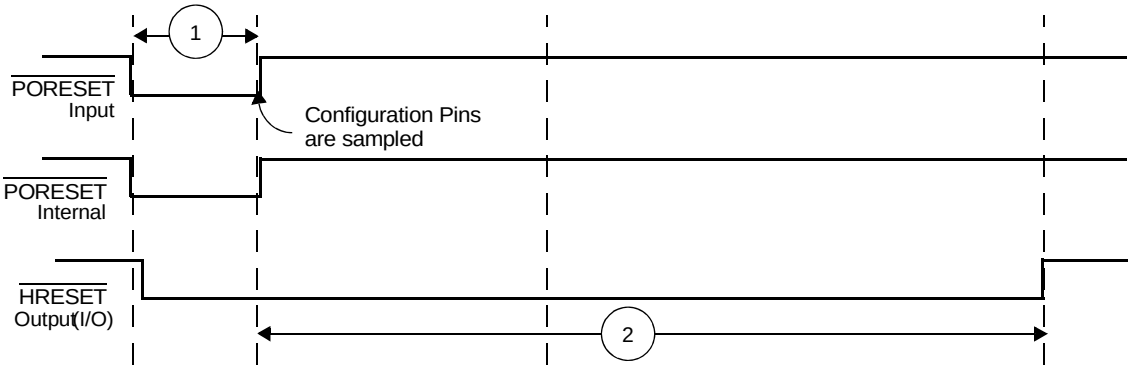


Figure 4. Timing Diagram for a Reset Configuration Write

2.5.4 DDR DRAM Controller Timing

This section provides the AC electrical characteristics for the DDR DRAM interface.

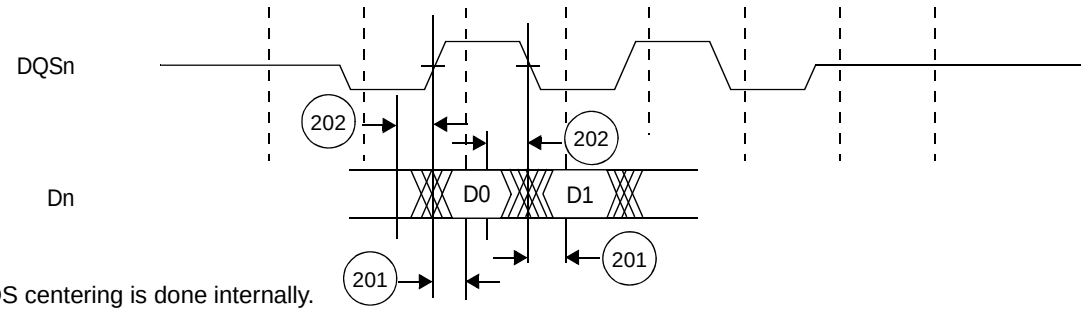
2.5.4.1 DDR DRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR DRAM interface.

Table 18. DDR DRAM Input AC Timing

No.	Parameter	Symbol	Min	Max		Unit
				Mask Set 1L44X	Mask Set 1M88B	
—	AC input low voltage	V_{IL}	—	V_{REF} – 0.31	V_{REF} – 0.31	V
—	AC input high voltage	V_{IH}	V_{REF} + 0.31	V_{DDM} + 0.3	V_{DDM} + 0.3	V
201	Maximum Dn input setup skew relative to DQSn input	—	—	1026	900	ps
202	Maximum Dn input hold skew relative to DQSn input	—	—	386	900	ps

Notes:
1. Maximum possible skew between a data strobe (DQSn) and any corresponding bit of data (D[8n + {0...7}] if 0 ≤ n ≤ 7).
2. See **Table 19** for t_{CK} value.
3. Dn should be driven at the same time as DQSn. This is necessary because the DQSn centering on the DQn data tenure is done internally.



Note: DQS centering is done internally.

Figure 5. DDR DRAM Input Timing Diagram

2.5.4.2 DDR DRAM Output AC Timing Specifications

Table 19 and **Table 20** list the output AC timing specifications and measurement conditions for the DDR DRAM interface.

Table 19. DDR DRAM Output AC Timing

No.	Parameter	Symbol	Min		Max	Unit
			Mask Set 1L44X	Mask Set 1M88B		
200	CK cycle time, (CK/$\overline{CK}$ crossing)[1] • 100 MHz (DDR200) • 133 MHz (DDR266)	t_{CK}	 10 Not applicable	 1.0 7.52	 — —	 ns ns
204	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output setup with respect to CK	t_{DDKHAS}	$0.5 \times t_{CK} - 2250$	$0.5 \times t_{CK} - 1000$	—	ps
205	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output hold with respect to CK	t_{DDKHAX}	$0.5 \times t_{CK} - 1250$	$0.5 \times t_{CK} - 1000$	—	ps
206	$\overline{CSn}$ output setup with respect to CK	t_{DDKHCS}	$0.5 \times t_{CK} - 2250$	$0.5 \times t_{CK} - 1000$	—	ps
207	$\overline{CSn}$ output hold with respect to CK	t_{DDKHCX}	$0.5 \times t_{CK} - 1250$	$0.5 \times t_{CK} - 1000$	—	ps
208	CK to DQSn[2]	t_{DDKHMH}	–600	–600	600	ps
209	Dn/DQMn output setup with respect to DQSn[3]	t_{DDKHDS}, t_{DDKLDS}	$0.25 \times t_{MCK} - 1050$	$0.25 \times t_{CK} - 750$	—	ps
210	Dn/DQMn output hold with respect to DQSn[3]	t_{DDKHDX}, t_{DDKLDX}	$0.25 \times t_{CK} - 1050$	$0.25 \times t_{CK} - 750$	—	ps
211	DQSn preamble start[4]	t_{DDKHMP}	$-0.25 \times t_{CK}$	$-0.25 \times t_{CK}$	—	ps
212	DQSn epilogue end[5]	t_{DDKHME}	–600	–600	600	ps

Notes:
1. All CK/$\overline{CK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
2. t_{DDKHMH} can be modified through the TCFG2[WRDD] DQSS override bits. The DRAM requires that the first write data strobe arrives 75–125% of a DRAM cycle after the write command is issued. Any skew between DQSn and CK must be considered when trying to achieve this 75%–125% goal. The TCFG2[WRDD] bits can be used to shift DQSn by 1/4 DRAM cycle increments. The skew in this case refers to an internal skew existing at the signal connections. By default, the CK/$\overline{CK}$ crossing occurs in the middle of the control signal (An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE) tenure. Setting TCFG2[ACSM] bit shifts the control signal assertion 1/2 DRAM cycle earlier than the default timing. This means that the signal is asserted no earlier than 410 ps before the CK/$\overline{CK}$ crossing and no later than 677 ps after the crossing time; the device uses 1087 ps of the skew budget (the interval from –410 to +677 ps). Timing is verified by referencing the falling edge of CK. See Chapter 10 of the *MSC711x Reference Manual* for details.
3. Determined by maximum possible skew between a data strobe (DQS) and any corresponding bit of data. The data strobe should be centered inside of the data eye.
4. Please note that this spec is in reference to the DQSn first rising edge. It could also be referenced from CK(r), but due to programmable delay of the write strobes (TCFG2[WRDD]), there pre-amble may be extended for a full DRAM cycle. For this reason, we reference from DQSn.
5. All outputs are referenced to the rising edge of CK. Note that this is essentially the CK/DQSn skew in spec 208. In addition there is no real “maximum” time for the epilogue end. JEDEC does not require this is as a device limitation, but simply for the chip to guarantee fast enough write to read turn-around times. This is already guaranteed by the memory controller operation.

Table 21. TDM Timing

No.	Characteristic	Expression	Min	Max	Units
307	TDMxTCK High to TDMxTD output valid		—	14.0	ns
308	TDMxTD hold time		2.0	—	ns
309	TDMxTCK High to TDMxTD output high impedance		—	10.0	ns
310	TDMXTFS/TDMxRFS output valid		—	13.5	ns
311	TDMxTFS/TDMxRFS output hold time		2.5	—	ns

Notes:
1. Output values are based on 30 pF capacitive load.
2. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. Refer to the *MSC711x Reference Manual* for details. TDMxTCK and TDMxRCK are shown using the rising edge.

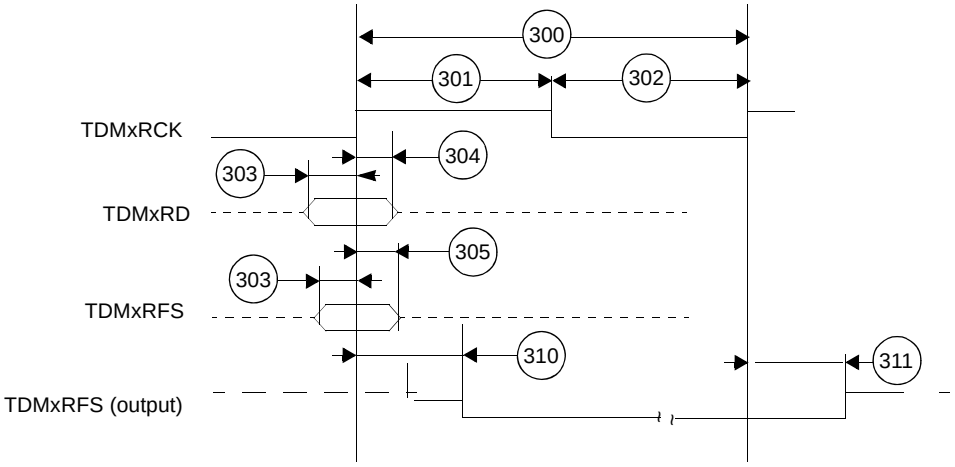


Figure 8. TDM Receive Signals

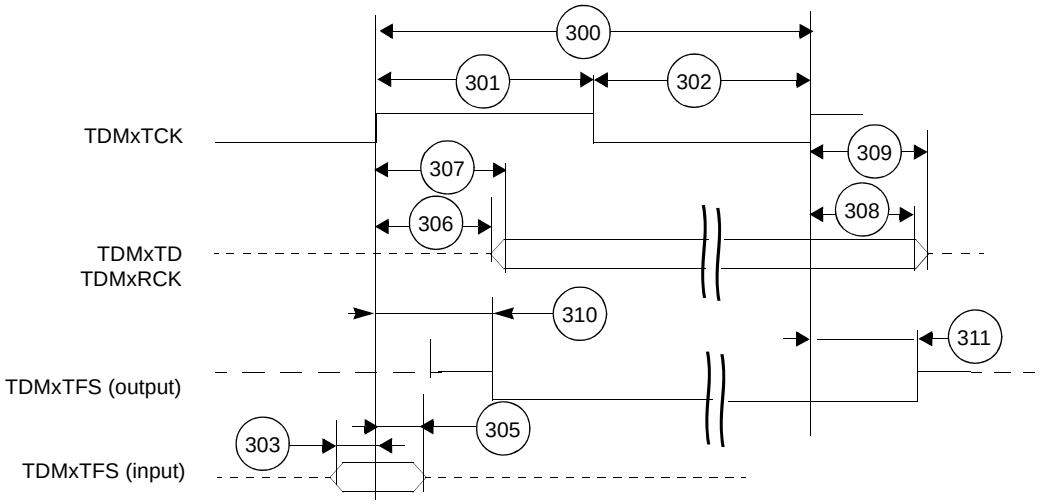


Figure 9. TDM Transmit Signals

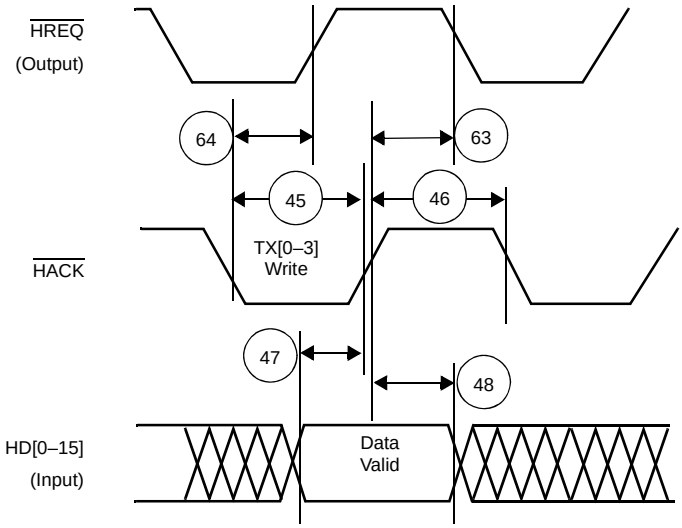


Figure 15. Host DMA Write Timing Diagram, HPCR[OAD] = 0

2.5.7 I²C Timing

Table 23. I²C Timing

No.	Characteristic	Fast		Unit
		Min	Max	
450	SCL clock frequency	0	400	kHz
451	Hold time START condition	(Clock period/2) – 0.3	—	µs
452	SCL low period	(Clock period/2) – 0.3	—	µs
453	SCL high period	(Clock period/2) – 0.1	—	µs
454	Repeated START set-up time (not shown in figure)	$2 \times 1/F_{BCK}$	—	µs
455	Data hold time	0	—	µs
456	Data set-up time	250	—	ns
457	SDA and SCL rise time	—	700	ns
458	SDA and SCL fall time	—	300	ns
459	Set-up time for STOP	(Clock period/2) – 0.7	—	µs
460	Bus free time between STOP and START	(Clock period/2) – 0.3	—	µs
Note:	SDA set-up time is referenced to the rising edge of SCL. SDA hold time is referenced to the falling edge of SCL. Load capacitance on SDA and SCL is 400 pF.			

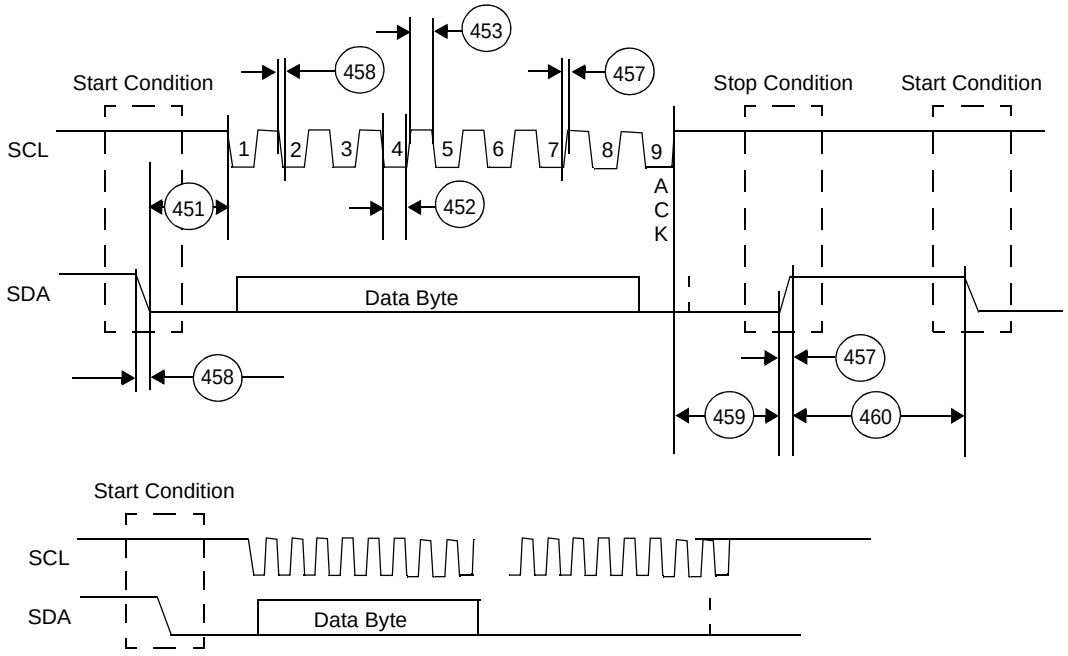


Figure 16. I²C Timing Diagram

2.5.12 JTAG Signals

Table 28. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/($T_C \times 3$); maximum 22 MHz)	0.0	40.0	MHz
701	TCK cycle time	25.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V	11.0	—	ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	14.0	—	ns
706	TCK low to output data valid	0.0	20.0	ns
707	TCK low to output high impedance	0.0	20.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	25.0	—	ns
710	TCK low to TDO data valid	0.0	24.0	ns
711	TCK low to TDO high impedance	0.0	10.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns

Note: All timings apply to OCE module data transfers as the OCE module uses the JTAG port as an interface.

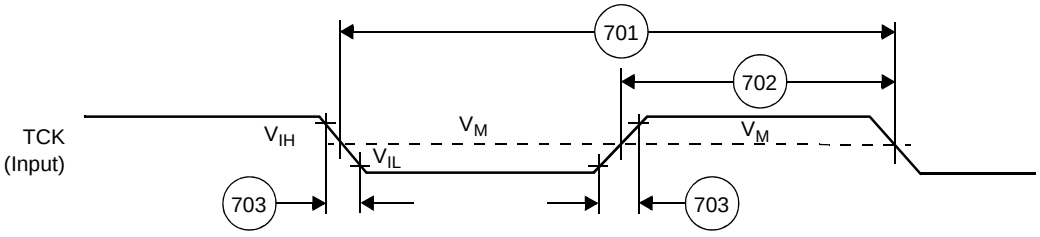


Figure 22. Test Clock Input Timing Diagram

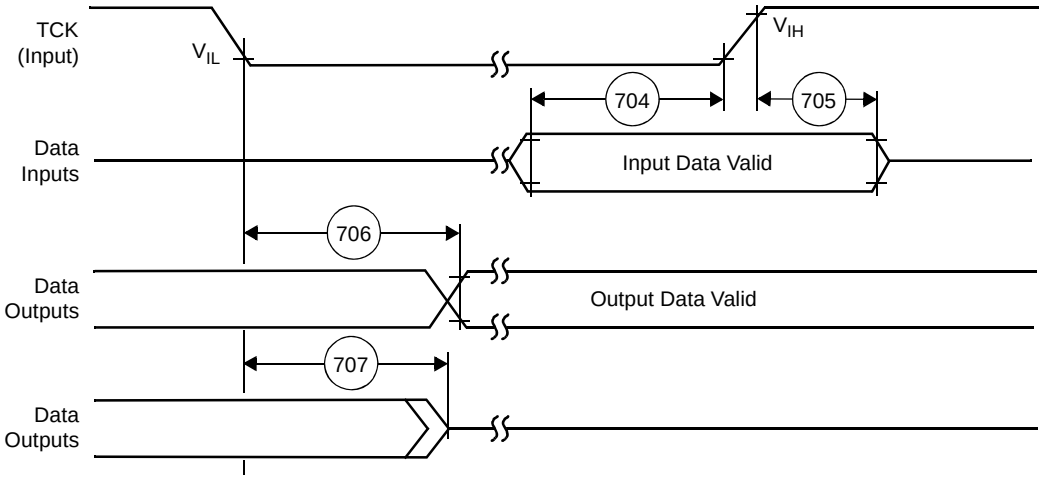


Figure 23. Boundary Scan (JTAG) Timing Diagram

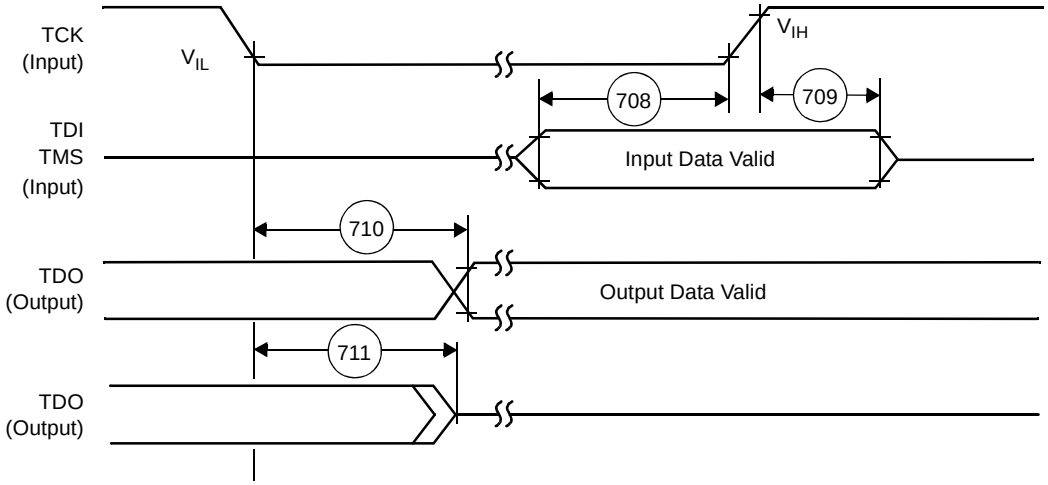


Figure 24. Test Access Port Timing Diagram

Figure 25. $\overline{\text{TRST}}$ Timing Diagram

3.2.2.3 Case 3

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) and V_{REF} (1.25 V) supplies simultaneously (third).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDM} (2.5 V) and V_{REF} (1.25 V) supplies simultaneously (first).
2. Turn off the V_{DDC} (1.2 V) supply second.
3. Turn of the V_{DDIO} (3.3 V) supply third (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down for V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 28** for relative timing for Case 3.

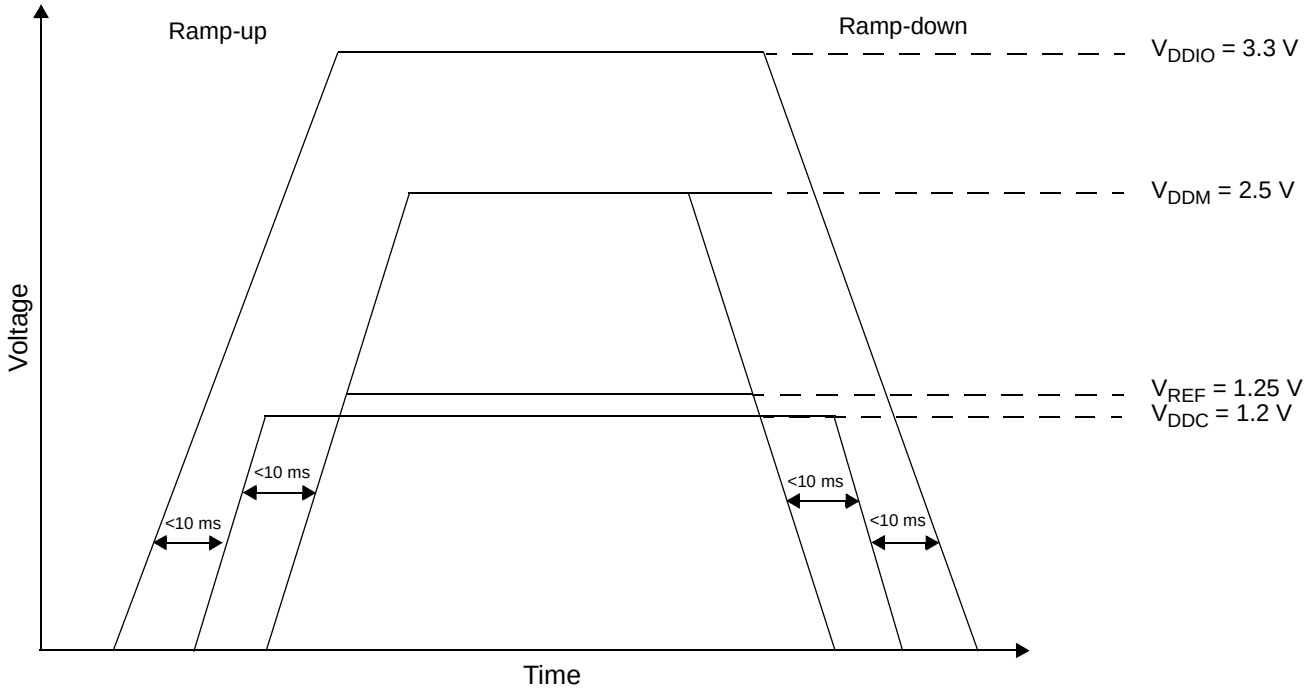


Figure 28. Voltage Sequencing Case 3

3.2.7 Power Supply Design

One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3 V supply can be used. However, a separate adjustable linear regulator supply for the core voltage V_{DDC} should be implemented. For the memory power supply, regulators are available that take care of all DDR power requirements.

Table 30. Recommended Power Supply Ratings

Supply	Symbol	Nominal Voltage	Current Rating
Core	V_{DDC}	1.2 V	1.5 A per device
Memory	V_{DDM}	2.5 V	0.5 A per device
Reference	V_{REF}	1.25 V	10 µA per device
I/O	V_{DDIO}	3.3 V	1.0 A per device

3.3 Estimated Power Usage Calculations

The following equations permit estimated power usage to be calculated for individual design conditions. Overall power is derived by totaling the power used by each of the major subsystems:

$$P_{TOTAL} = P_{CORE} + P_{PERIPHERALS} + P_{DDRIO} + P_{IO} + P_{LEAKAGE} \quad \textit{Eqn. 3}$$

This equation combines dynamic and static power. Dynamic power is determined using the generic equation:

$$C \times V^2 \times F \times 10^{-3}\ mW \quad \textit{Eqn. 4}$$

where,

C = load capacitance in pF

V = peak-to-peak voltage swing in V

F = frequency in MHz

3.3.1 Core Power

Estimation of core power is straightforward. It uses the generic dynamic power equation and assumes that the core load capacitance is 750 pF, core voltage swing is 1.2 V, and the core frequency is 200 MHz or 266 MHz. This yields:

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 200\ MHz \times 10^{-3} = 216\ mW \quad \textit{Eqn. 5}$$

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 266\ MHz \times 10^{-3} = 287\ mW \quad \textit{Eqn. 6}$$

This equation allows for adjustments to voltage and frequency if necessary.

3.6 Connectivity Guidelines

This section summarizes the connections and special conditions, such as pull-up or pull-down resistors, for the MSC7112 device. Following are guidelines for signal groups and configuration settings:

- *Clock and reset signals*.
  - SWTE is used to configure the MSC7112 device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{DDC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$, this signal can be left floating.
  - BM[0–1] configure the MSC7112 device and are sampled until $\overline{\text{PORESET}}$ is deasserted, so they should be tied to V_{DDIO} or GND either directly or through pull-up or pull-down resistors.
  - $\overline{\text{HRESET}}$ should be pulled up.
- *Interrupt signals*. When used, $\overline{\text{IRQ}}$ pins must be pulled up.
- *HDI16 signals*.
  - When they are configured for open-drain, the $\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ signals require a pull-up resistor. However, these pins are also sampled at power-on reset to determine the HDI16 boot mode and may need to be pulled down. When these pins must be pulled down on reset and pulled up otherwise, a buffer can be used with the $\overline{\text{HRESET}}$ signal as the enable.
  - When the device boots through the HDI16, the HDDS, HDSP and H8BIT pins should be pulled up or down, depending on the required boot mode settings.
- *I^2C signals*. The SCL and SDA signals, when programmed for I^2C, requires an external pull-up resistor.
- *General-purpose I/O (GPIO) signals*. An unused GPIO pin can be disconnected. After boot, program it as an output pin.
- Other signals.
  - The $\overline{\text{TEST0}}$ pin must be connected to ground.
  - The $\overline{\text{TPSEL}}$ pin should be pulled up to enable debug access via the EOnCE port and pulled down for boundary scan.
  - Pins labelled NO CONNECT (NC) must not be connected.
  - When a 16-pin double data rate (DDR) interface is used, the 16 unused data pins should be no connects (floating) if the used lines are terminated.
  - Do not connect DBREQ to DONE (as you would for the MSC8101 device). Connect DONE to one of the EVNT pins, and DBREQ to HRRQ.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
MSC7112 (mask 1L44X	1.2 V core 2.5 V mem. 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	200	Lead-free	MSC7112VM800
					Lead-bearing	MSC7112VF800
MSC7112 (mask 1M88B)	1.2 V core 2.5 V mem 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	266	Lead-free	MSC7112VM1000
					Lead-bearing	MSC7112VF1000

5 Package Information

Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

CASE 1568-01

Figure 34. MSC7112 Mechanical Information, 400-pin MAP-BGA Package

6 Product Documentation

- *MSC711x Reference Manual* (MSC711xRM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC7112 device.
- *SC140/SC1400 DSP Core Reference Manual*. Covers the SC140 and SC1400 core architecture, control registers, clock registers, program control, and instruction set.