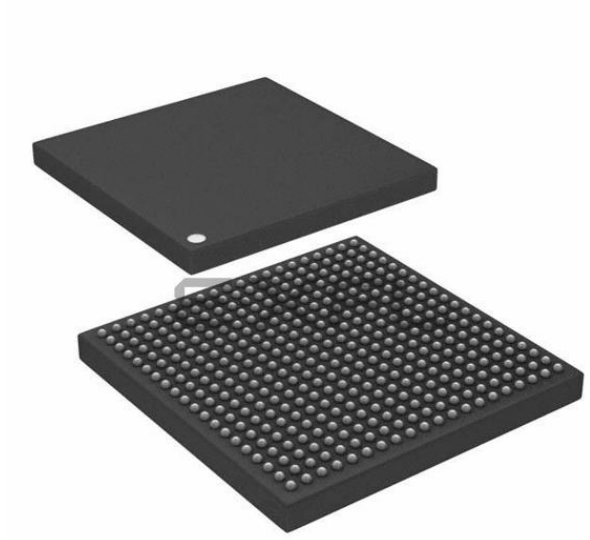

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC1400 Core
Interface	Host Interface, I²C, UART
Clock Rate	200MHz
Non-Volatile Memory	External
On-Chip RAM	208kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc7112vm800

Table of Contents

List of Figures

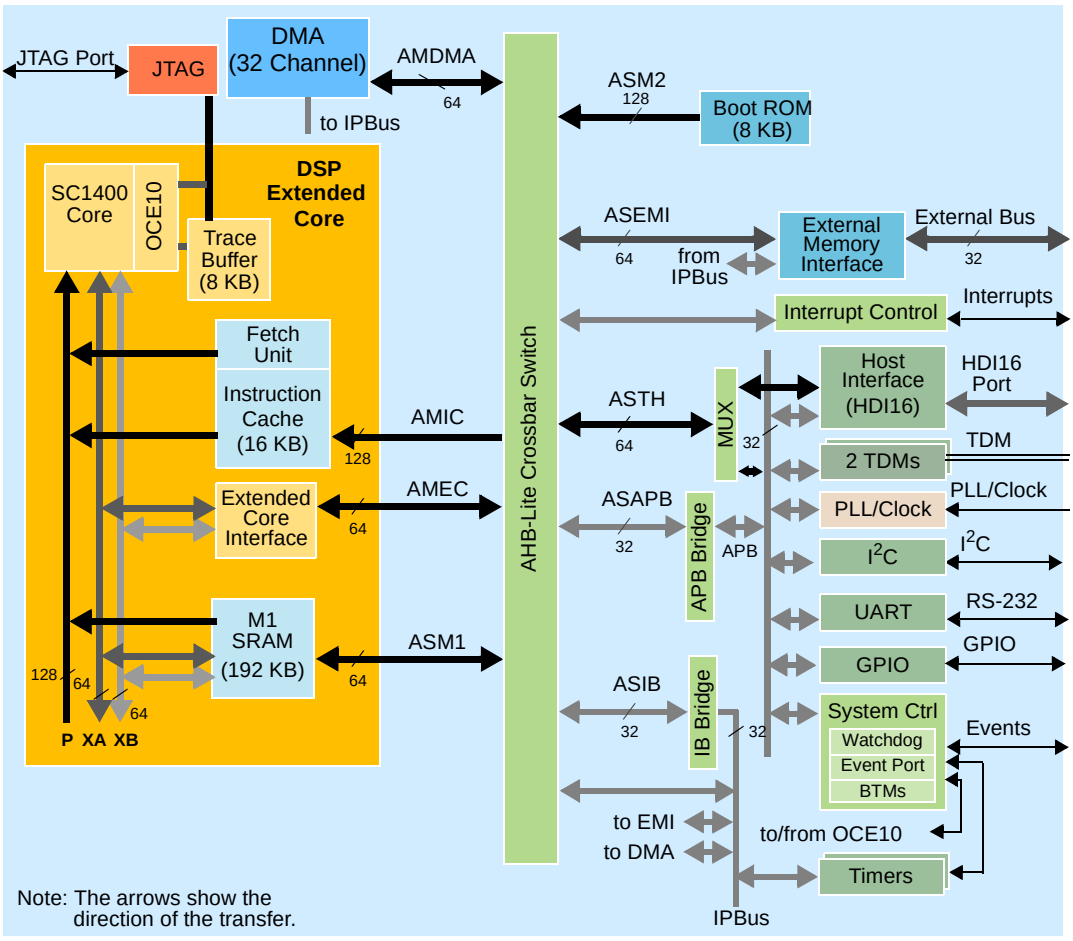


Figure 1. MSC7112 Block Diagram

1.2 Signal List By Ball Location

Table 1 lists the signals sorted by ball number and configuration.

Table 1. MSC7112 Signals by Ball Designator

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
A1	GND					
A2	GND					
A3	DQM1					
A4	DQS2					
A5	CK					
A6	$\overline{CK}$					
A7	GPIC7			GPOC7	HD15	
A8	GPIC4			GPOC4	HD12	
A9	GPIC2			GPOC2	HD10	
A10	reserved				HD7	
A11	reserved				HD6	
A12	reserved				HD4	
A13	reserved				HD1	
A14	reserved				HD0	
A15	GND					
A16 (1L44X)	NC					
A16 (1M88B)	BM3	GPID8		GPOD7	reserved	
A17	NC					
A18	NC					
A19	NC					
A20	NC					
B1	V_{DDM}					
B2	NC					
B3	$\overline{CS0}$					
B4	DQM2					
B5	DQS3					
B6	DQS0					
B7	CKE					
B8	$\overline{WE}$					
B9	GPIC6			GPOC6	HD14	
B10	GPIC3			GPOC3	HD11	
B11	GPIC0			GPOC0	HD8	
B12	reserved				HD5	
B13	reserved				HD2	
B14	NC					
B15 (1L44X)	NC					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D13	V_{DDIO}					
D14	V_{DDIO}					
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H9	GND					
H10	GND					
H11	GND					
H12	GND					
H13	GND					
H14	GND					
H15	V_{DDIO}					
H16	V_{DDIO}					
H17	V_{DDC}					
H18	NC					
H19	reserved				HA2	
H20	reserved				HA1	
J1	D10					
J2	V_{DDM}					
J3	D9					
J4	V_{DDM}					
J5	V_{DDM}					
J6	V_{DDM}					
J7	GND					
J8	GND					
J9	GND					
J10	GND					
J11	GND					
J12	GND					
J13	GND					
J14	GND					
J15	GND					
J16	V_{DDIO}					
J17	V_{DDC}					
J18 (1L44X)	reserved				HA3	
J18 (1M88B)	GPIC11			GPOC11	HA3	
J19	reserved				$\overline{\text{HACK}}$/HACK or $\overline{\text{HRRQ}}$/HRRQ	
J20	HDSP	reserved			$\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ	
K1	D0					
K2	GND					
K3	D8					
K4	V_{DDC}					
K5	V_{DDM}					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
K6	GND					
K7	GND					
K8	GND					
K9	GND					
K10	GND					
K11	GND					
K12	GND					
K13	GND					
K14	GND					
K15	V_{DDIO}					
K16	V_{DDIO}					
K17	V_{DDC}					
K18	reserved				HA0	
K19	reserved				HDDS	
K20	reserved				$\overline{\text{HDS}}$/HDS or $\overline{\text{HWR}}$/HWR	
L1	D1					
L2	GND					
L3	D3					
L4	V_{DDC}					
L5	V_{DDM}					
L6	GND					
L7	GND					
L8	GND					
L9	GND					
L10	GND					
L11	GND					
L12	GND					
L13	GND					
L14	V_{DDIO}					
L15	V_{DDIO}					
L16	V_{DDIO}					
L17	V_{DDC}					
L18 (1L44X)	reserved				$\overline{\text{HCS2}}$/HCS2	
L18 (1M88B)	GPIB11			GPOB11	$\overline{\text{HCS2}}$/HCS2	
L19	reserved				$\overline{\text{HCS1}}$/HCS1	
L20	reserved				HRW or $\overline{\text{HRD}}$/HRD	
M1	D2					
M2	V_{DDM}					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
M3	V_{DDM}					
M4	V_{DDM}					
M5	V_{DDM}					
M6	GND					
M7	GND					
M8	GND					
M9	GND					
M10	GND					
M11	GND					
M12	GND					
M13	GND					
M14	GND					
M15	GND					
M16	V_{DDC}					
M17	V_{DDC}					
M18	GPIA14		$\overline{IRQ15}$		GPOA14	SDA
M19	GPIA12		$\overline{IRQ3}$		GPOA12	UTXD
M20	GPIA13		$\overline{IRQ2}$		GPOA13	URXD
N1	D4					
N2	D6					
N3	V_{REF}					
N4	V_{DDM}					
N5	V_{DDM}					
N6	V_{DDM}					
N7	GND					
N8	GND					
N9	GND					
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$		GPOA15	SCL
N20	V_{SSPLL}					

Table 1. MSC7112 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
U17	V_{DDC}					
U18	NC					
U19	TCK					
U20	$\overline{\text{TRST}}$					
V1	V_{DDM}					
V2	NC					
V3	A13					
V4	A11					
V5	A10					
V6	A5					
V7	A2					
V8	BA0					
V9	NC					
V10	reserved				EVNT0	
V11	SWTE	GPIA16	$\overline{\text{IRQ12}}$	GPOA16	EVNT4	
V12	GPIA8		$\overline{\text{IRQ6}}$	GPOA8	T0TCK	
V13	GPIA4		$\overline{\text{IRQ1}}$	GPOA4	T1RFS	
V14	GPIA0		$\overline{\text{IRQ11}}$	GPOA0	T1TD	
V15	GPIA28		$\overline{\text{IRQ17}}$	GPOA28	reserved	reserved
V16	GPID6			GPOD6	reserved	reserved
V17	GPIA22		$\overline{\text{IRQ22}}$	GPOA22	reserved	
V18	GPIA24		$\overline{\text{IRQ24}}$	GPOA24	reserved	
V19	NC					
V20	TDI					
W1	GND					
W2	V_{DDM}					
W3	A12					
W4	A8					
W5	A7					
W6	A6					
W7	A3					
W8	NC					
W9	GPIA17		$\overline{\text{IRQ13}}$	GPOA17	EVNT1	CLKO
W10	BM0	GPIC14		GPOC14	EVNT2	
W11	GPIA10		$\overline{\text{IRQ5}}$	GPOA10	T0RFS	
W12	GPIA7		$\overline{\text{IRQ7}}$	GPOA7	T0TFS	
W13	GPIA3		$\overline{\text{IRQ8}}$	GPOA3	T1RD	
W14	GPIA1		$\overline{\text{IRQ10}}$	GPOA1	T1TFS	

2 Specifications

This chapter covers power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC711x Reference Manual*.

Note: The MSC7112 electrical specifications are preliminary and many are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC7112.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.5	V
Memory supply voltage	V_{DDM}	4.0	V
PLL supply voltage	V_{DDPLL}	1.5	V
I/O supply voltage	V_{DDIO}	–0.2 to 4.0	V
Input voltage	V_{IN}	(GND – 0.2) to 4.0	V
Reference voltage	V_{REF}	4.0	V
Maximum operating temperature	T_J	105	°C
Minimum operating temperature	T_A	–40	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.1**, *Thermal Design Considerations* includes a formula for computing the chip junction temperature (T_J).

Table 13. Resulting Ranges Permitted for the Core Clock

CLKCTRL[CKSEL]	CLKCTRL[RNG]	Resulting Division Factor	Allowed Range of Core Clock	Comments
11	1	1	Reserved	Reserved
11	0	2	150 ≤ Core_Clk ≤ 200 MHz	Limited by range of PLL
01	1	2	150 ≤ Core_Clk ≤ 200 MHz	Limited by range of PLL
01	0	4	75 ≤ Core_Clk ≤ 150 MHz	Limited by range of PLL
Note: This table results from the allowed range for F_{OUT}, which depends on clock selected via CLKCTRL[CKSEL].				

2.5.2.5 Core Clock Frequency Range When Using DDR Memory

The core clock can also be limited by the frequency range of the DDR devices in the system. **Table 14** summarizes this restriction.

Table 14. Core Clock Ranges When Using DDR

DDR Type	Allowed Frequency Range for DDR CK	Corresponding Range for the Core Clock	Comments
DDR 200 (PC-1600)	83–100 MHz	166 ≤ core clock ≤ 200 MHz	Core limited to 2 × maximum DDR frequency
DDR 266 (PC-2100)	83–133 MHz	166 ≤ core clock ≤ 266 MHz	Core limited to 2 × maximum DDR frequency
DDR 333 (PC-2600)	83–150 MHz	166 ≤ core clock ≤ 300 MHz	Core limited to 2 × maximum DDR frequency

2.5.3 Reset Timing

The MSC7112 device has several inputs to the reset logic. All MSC7112 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 15** describes the reset sources.

Table 15. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC7112 and configures various attributes of the MSC7112. On PORESET, the entire MSC7112 device is reset. SPLL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted.
External Hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC7112. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset.
Software watchdog reset	Internal	When the MSC7112 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC7112 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
JTAG EXTEST, CLAMP, or HIGHZ command	Internal	When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence.

Table 16 summarizes the reset actions that occur as a result of the different reset sources.

Figure 6 shows the DDR DRAM output timing diagram.

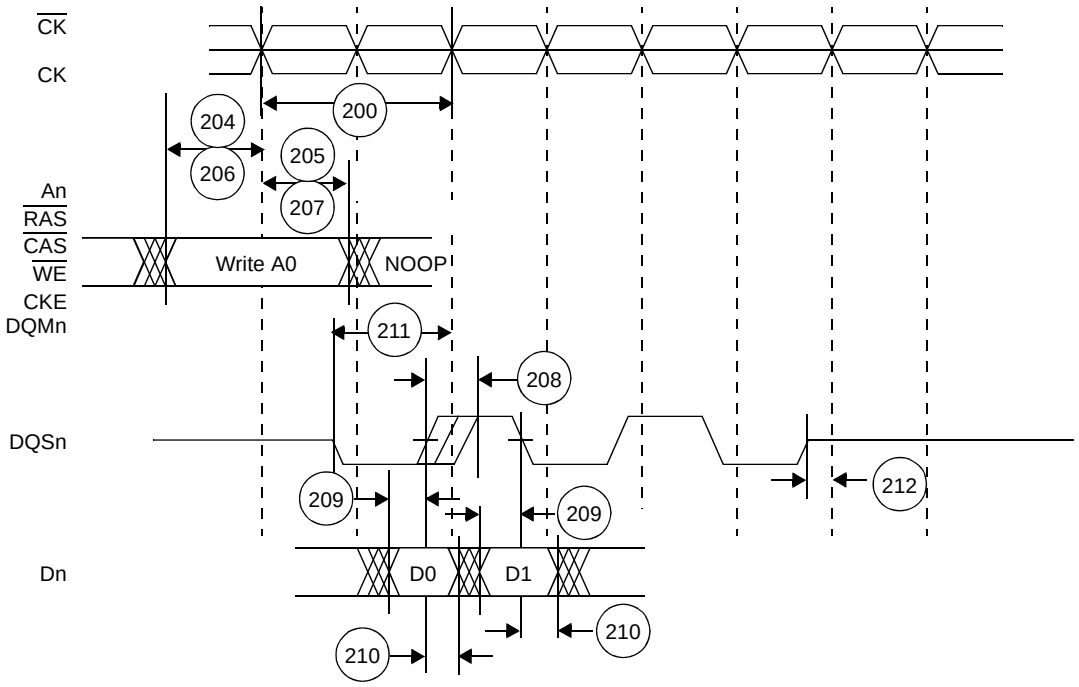


Figure 6. DDR DRAM Output Timing Diagram

Figure 7 provides the AC test load for the DDR DRAM bus.

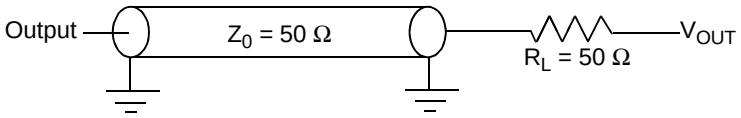


Figure 7. DDR DRAM AC Test Load

Table 20. DDR DRAM Measurement Conditions

Symbol	DDR DRAM	Unit
V_{TH}[1]	V_{REF} ± 0.31 V	V
V_{OUT}[2]	0.5 × V_{DDM}	V

Notes: **1.** Data input threshold measurement point.
2. Data output measurement point.

2.5.5 TDM Timing

Table 21. TDM Timing

No.	Characteristic	Expression	Min	Max	Units
300	TDMxRCK/TDMxTCK	TC	20.0	—	ns
301	TDMxRCK/TDMxTCK High Pulse Width	0.4 × TC	8.0	—	ns
302	TDMxRCK/TDMxTCK Low Pulse Width	0.4 × TC	8.0	—	ns
303	TDM all input Setup time		3.0	—	ns
304	TDMxRD Hold time		3.5	—	ns
305	TDMxTFS/TDMxRFS input Hold time		2.0	—	ns
306	TDMxTCK High to TDMxTD output active		4.0	—	ns

2.5.8 UART Timing

Table 24. UART Timing

No.	Characteristics	Expression	Mask Set 1L44X		Mask Set 1M88B		Unit
			Min	Max	Min	Max	
—	Internal bus clock (APBCLK)	$F_{CORE}/2$	—	100	—	133	MHz
—	Internal bus clock period (1/APBCLK)	T_{APBCLK}	10.0	—	7.52	—	ns
400	URXD and UTXD inputs high/low duration	$16 \times T_{APBCLK}$	160.0	—	120.3	—	ns
401	URXD and UTXD inputs rise/fall time		—	5	—	5	ns
402	UTXD output rise/fall time		—	5	—	5	ns

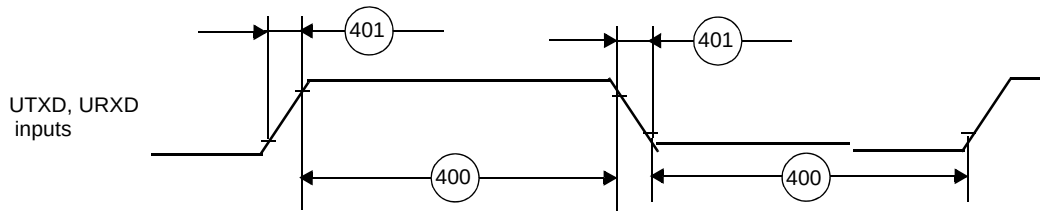


Figure 17. UART Input Timing

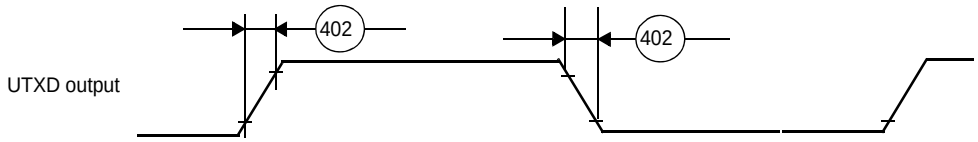


Figure 18. UART Output Timing

2.5.9 EE Timing

Table 25. EE0 Timing

Number	Characteristics	Type	Min
65	EE0 input to the core	Asynchronous	4 core clock periods
66	EE0 output from the core	Synchronous to core clock	1 core clock period

Notes:
1. The core clock is the SC1400 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Configure the direction of the EE pin in the EE_CTRL register (see the *SC1400 Core Reference Manual* for details.
3. Refer to **Table 15** for details on EE pin functionality.

Figure 19 shows the signal behavior of the EE pin.

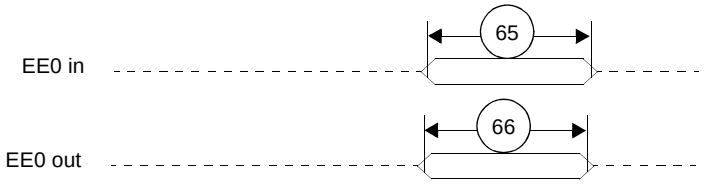


Figure 19. EE Pin Timing

3 Hardware Design Considerations

This section described various areas to consider when incorporating the MSC7112 device into a system design.

3.1 Thermal Design Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)

$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)

$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC7112 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip.

You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case. Use the following equation to determine T_J:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

3.2.2.1 Case 1

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 26** for relative timing for power sequencing case 1.

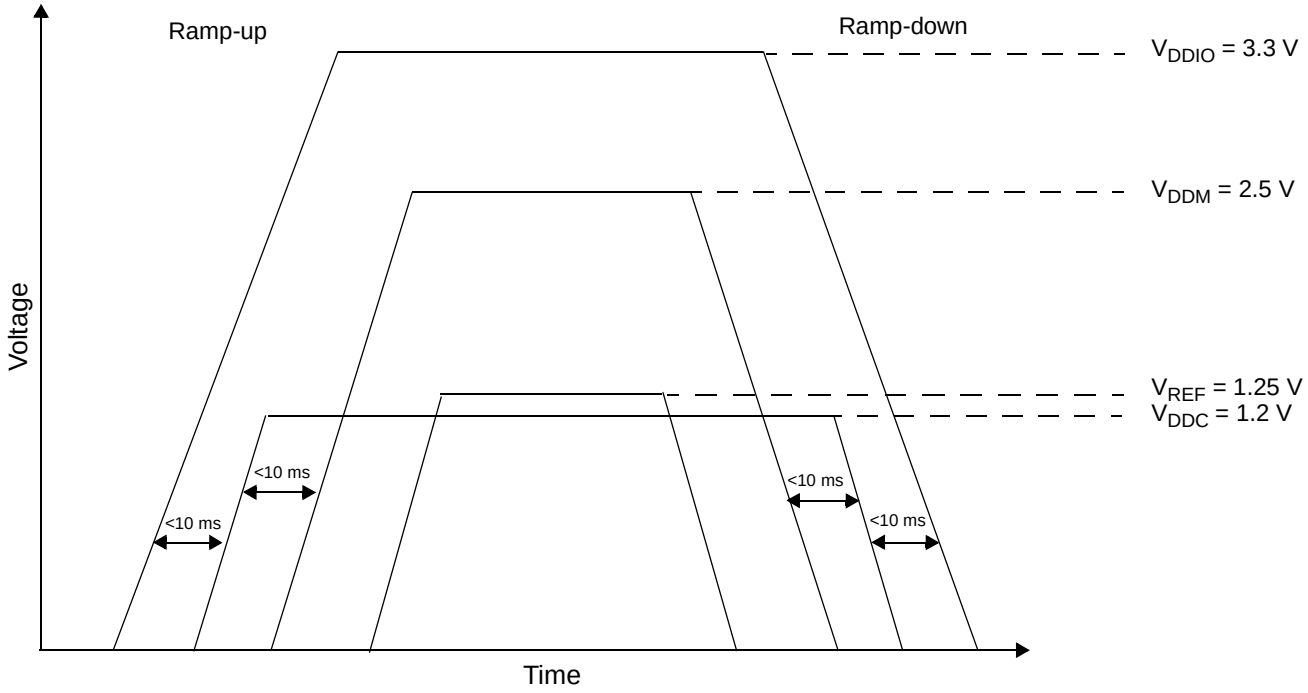


Figure 26. Voltage Sequencing Case 1

3.2.2.3 Case 3

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) and V_{REF} (1.25 V) supplies simultaneously (third).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDM} (2.5 V) and V_{REF} (1.25 V) supplies simultaneously (first).
2. Turn off the V_{DDC} (1.2 V) supply second.
3. Turn of the V_{DDIO} (3.3 V) supply third (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down for V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 28** for relative timing for Case 3.

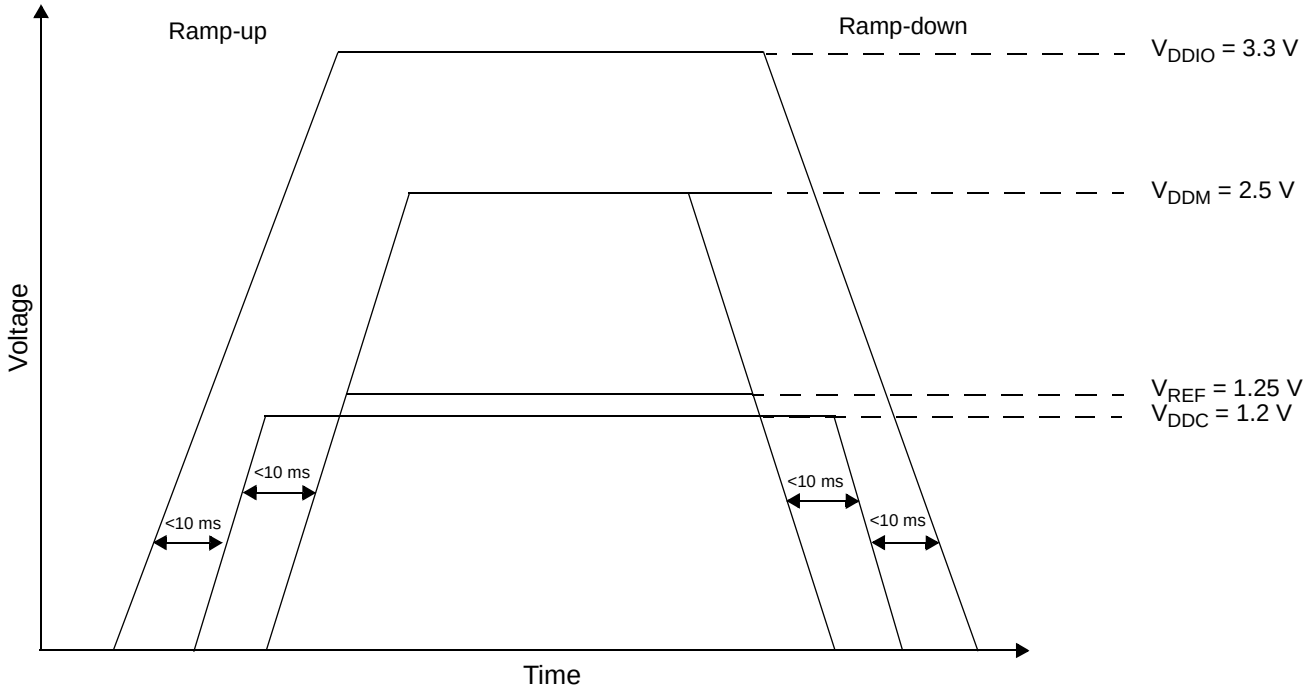


Figure 28. Voltage Sequencing Case 3

3.2.2.4 Case 4

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V), V_{DDM} (2.5 V), and V_{REF} (1.25 V) supplies simultaneously (second).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDC} (1.2 V), V_{REF} (1.25 V), and V_{DDM} (2.5 V) supplies simultaneously (first).
2. Turn of the V_{DDIO} (3.3 V) supply last.

Use the following guidelines:

- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 29** for relative timing for Case 4.

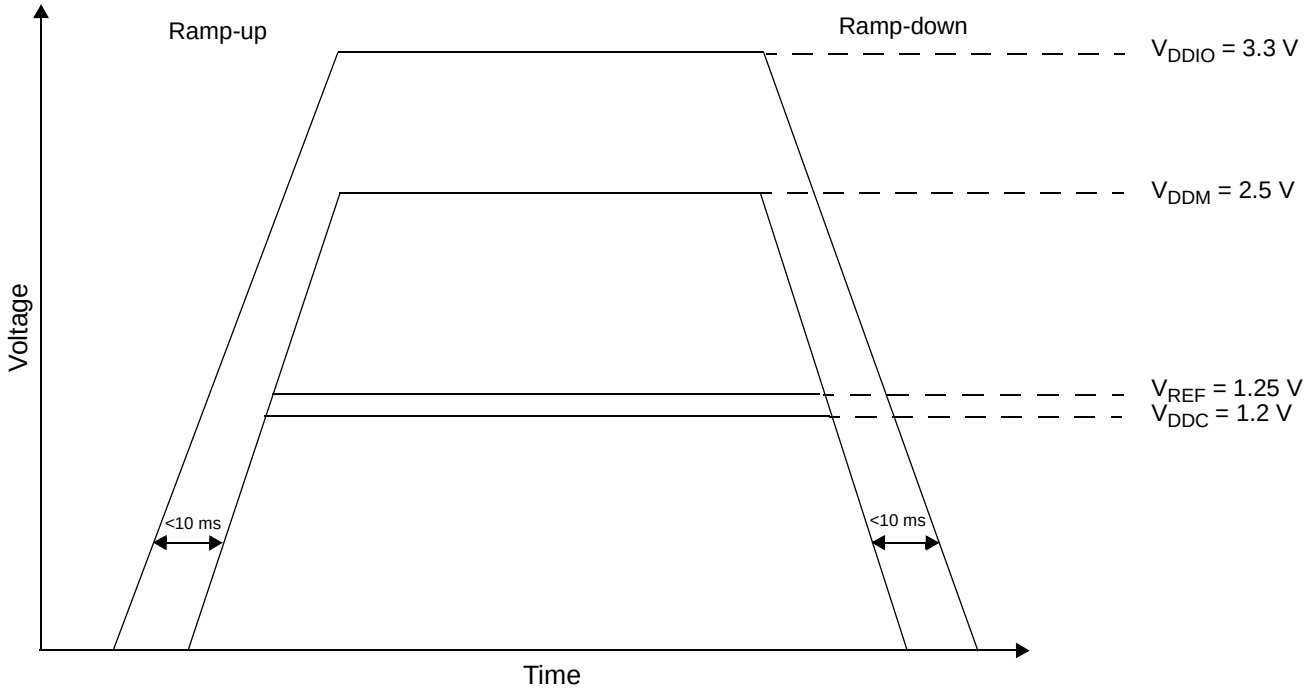


Figure 29. Voltage Sequencing Case 4

3.4.3.2 I²C Boot

When the MSC7112 device is configured to boot from the I²C port, the boot program configures the GPIO pins shared with the I²C pins as I²C pins. The I²C interface is configured as follows:

- I²C in master mode.
- EPROM in slave mode.

For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

3.5 DDR Memory System Guidelines

MSC7112 devices contain a memory controller that provides a glueless interface to external double data rate (DDR) SDRAM memory modules with Class 2 Series Stub Termination Logic 2.5 V (SSTL_2). There are two termination techniques, as shown in Figure 32. Technique B is the most popular termination technique.

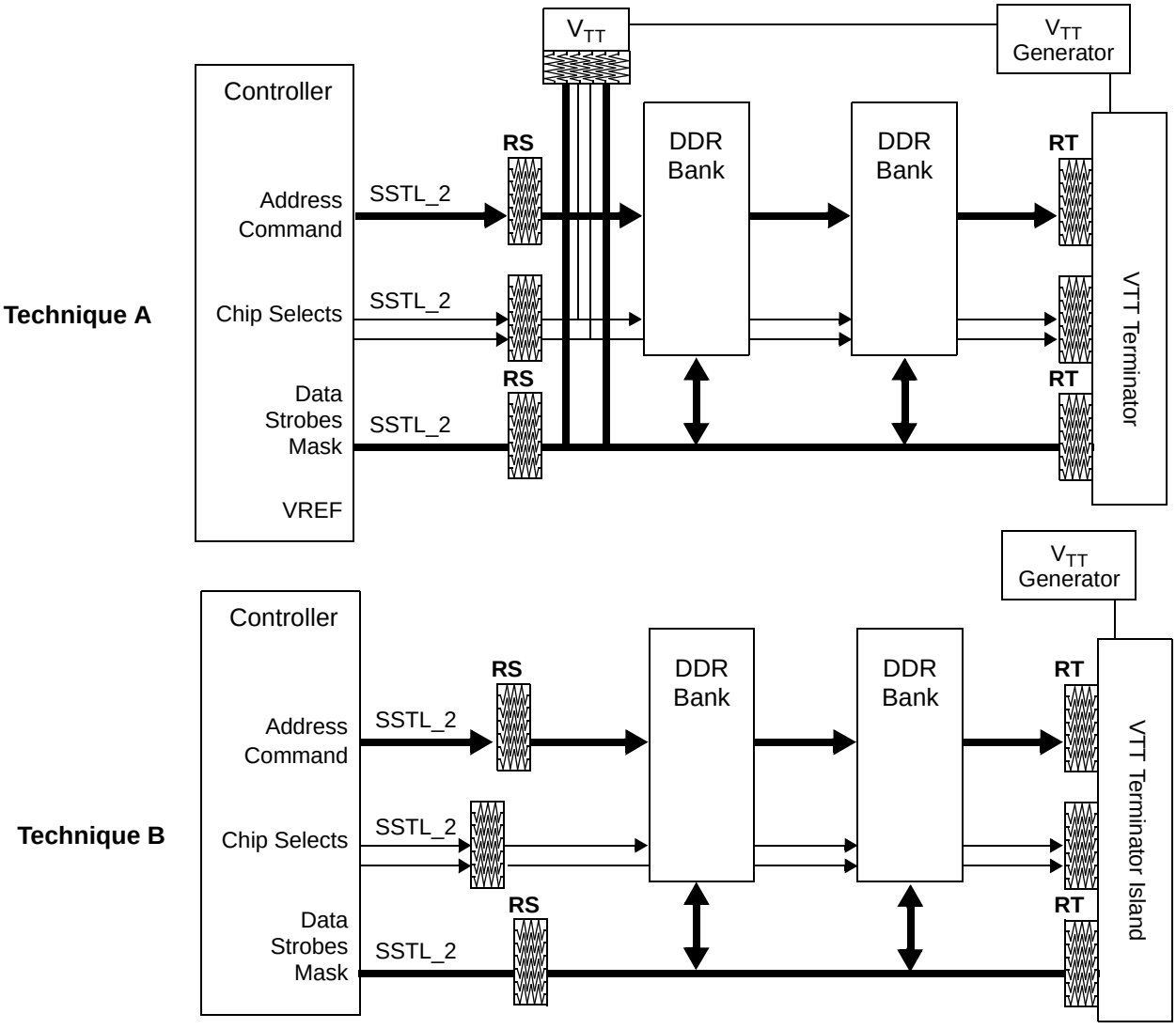


Figure 32. SSTL Termination Techniques

Figure 33 illustrates the power wattage for the resistors. Typical values for the resistors are as follows:

- RS = 22 Ω
- RT = 24 Ω

3.6 Connectivity Guidelines

This section summarizes the connections and special conditions, such as pull-up or pull-down resistors, for the MSC7112 device. Following are guidelines for signal groups and configuration settings:

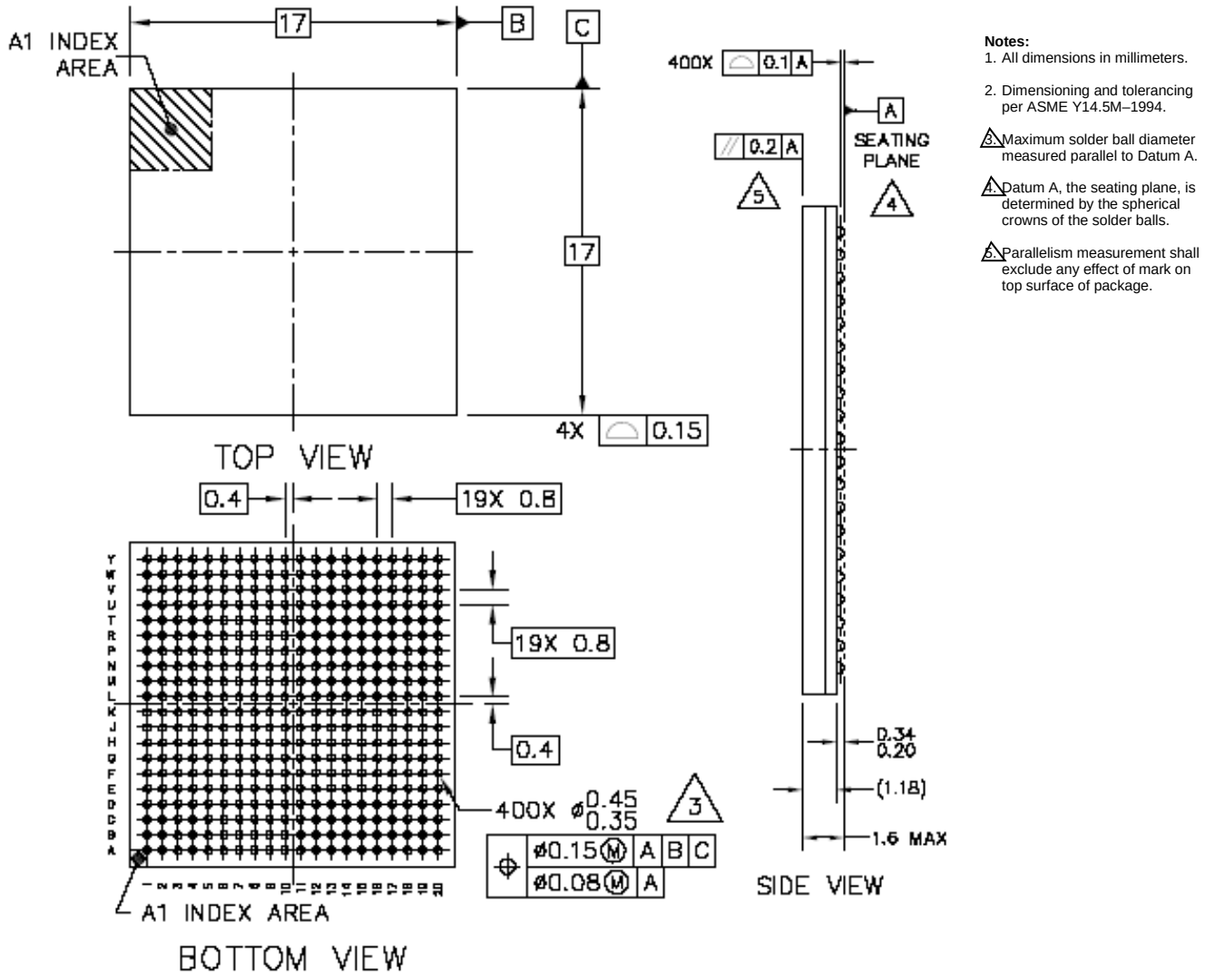
- *Clock and reset signals*.
  - SWTE is used to configure the MSC7112 device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{DDC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$, this signal can be left floating.
  - BM[0–1] configure the MSC7112 device and are sampled until $\overline{\text{PORESET}}$ is deasserted, so they should be tied to V_{DDIO} or GND either directly or through pull-up or pull-down resistors.
  - $\overline{\text{HRESET}}$ should be pulled up.
- *Interrupt signals*. When used, $\overline{\text{IRQ}}$ pins must be pulled up.
- *HDI16 signals*.
  - When they are configured for open-drain, the $\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ signals require a pull-up resistor. However, these pins are also sampled at power-on reset to determine the HDI16 boot mode and may need to be pulled down. When these pins must be pulled down on reset and pulled up otherwise, a buffer can be used with the $\overline{\text{HRESET}}$ signal as the enable.
  - When the device boots through the HDI16, the HDDS, HDSP and H8BIT pins should be pulled up or down, depending on the required boot mode settings.
- *I^2C signals*. The SCL and SDA signals, when programmed for I^2C, requires an external pull-up resistor.
- *General-purpose I/O (GPIO) signals*. An unused GPIO pin can be disconnected. After boot, program it as an output pin.
- Other signals.
  - The $\overline{\text{TEST0}}$ pin must be connected to ground.
  - The $\overline{\text{TPSEL}}$ pin should be pulled up to enable debug access via the EOnCE port and pulled down for boundary scan.
  - Pins labelled NO CONNECT (NC) must not be connected.
  - When a 16-pin double data rate (DDR) interface is used, the 16 unused data pins should be no connects (floating) if the used lines are terminated.
  - Do not connect DBREQ to DONE (as you would for the MSC8101 device). Connect DONE to one of the EVNT pins, and DBREQ to HRRQ.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
MSC7112 (mask 1L44X	1.2 V core 2.5 V mem. 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	200	Lead-free	MSC7112VM800
					Lead-bearing	MSC7112VF800
MSC7112 (mask 1M88B)	1.2 V core 2.5 V mem 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	266	Lead-free	MSC7112VM1000
					Lead-bearing	MSC7112VF1000

5 Package Information



CASE 1568-01

Figure 34. MSC7112 Mechanical Information, 400-pin MAP-BGA Package

6 Product Documentation

- *MSC711x Reference Manual* (MSC711xRM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes.* Cover various programming topics related to the StarCore DSP core and the MSC7112 device.
- *SC140/SC1400 DSP Core Reference Manual*. Covers the SC140 and SC1400 core architecture, control registers, clock registers, program control, and instruction set.

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