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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	12MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lv55-12ji

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3. Block Diagram





4.6 Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89LV55, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INTO (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Port 3 also receives the highest-order address bit and some control signals for Flash programming and verification.

4.7 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

4.8 ALE/PROG

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

4.9 PSEN

Program Store Enable is the read strobe to external program memory.

When the AT89LV55 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.





AT89LV55

6

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000			PCON 0XXX0000	87H

Table 5-1. AT89LV55 SFR Map and Reset Values

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in

XTAL1

4.11

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

4.12 XTAL2

Output from the inverting oscillator amplifier.

Special Function Registers 5.

Table 5-1.

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, \overline{EA} will be internally latched on reset.

 \overline{EA} should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during 12-volt Flash programming.

4.10 EA/V_{PP}

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 5-2) and T2MOD (shown in Table 8-2) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 5-2.	T2CON –	Timer/Counter 2	Control	Register

T2CON Address = 0C8H Reset Value = 0000 0000B								
Bit Addressable								
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/ <u>T2</u>	Timer or counter select for Timer 2. $C/T2 = 0$ for timer function. $C/T2 = 1$ for external event counter (falling edge triggered).
CP/RL2	Capture/Reload select. $CP/\overline{RL2} = 1$ causes captures to occur on negative transitions at T2EX if EXEN2 = 1. $CP/\overline{RL2} = 0$ causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.



RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	Х	1	Baud Rate Generator
X	Х	0	(Off)

 Table 8-1.
 Timer 2 Operating Modes

8.1 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 8-1.





8.2 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 8-2). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 8-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 8-3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.





A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.





Table 8-2. T2MOD—Timer 2 Mode Control Register

T2MOD Address = 0C9H Reset Value = XXXX XX00						XXXX XX00B		
Not B	Not Bit Addressable							
	_	_	_	_	_	_	T20E	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
-	Not implemented, reserved for future use.
T20E	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.





Figure 8-4. Timer 2 in Baud Rate Generator Mode







15. Power-down Mode

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 15-1. Oscillator Connections



Note: C1, C2 = 30 pF \pm 10 pF for Crystals = 40 pF \pm 10 pF for Ceramic Resonators





Table 15-1.	Status of External Pins During Idle and Power-down Modes
-------------	--

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
ldle	Internal	1	1	Data	Data	Data	Data
ldle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

16. Program Memory Lock Bits

The AT89LV55 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 16-1:

Program Lock Bits			3	
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features.
2	Ρ	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the Flash memory is disabled.
3	Р	Р	U	Same as mode 2, but verify is also disabled.
4	Р	Р	Р	Same as mode 3, but external execution is also disabled.

Table 16-1.Lock Bit Protection Modes

When lock bit 1 is programmed, the logic level at the \overline{EA} pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of \overline{EA} must agree with the current logic level at that pin in order for the device to function properly.

The AT89LV55 code memory array is programmed byte-by-byte. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

17. Programming the Flash

The AT89LV55 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed.

Programming Algorithm: Before programming the AT89LV55, the address, data and control signals should be set up according to Table 18-1, "Flash Programming Modes," on page 19 and Figure 18-1. To program the AT89LV55, take the following steps:

- 1. Input the desired memory location on the address lines.
- 2. Input the appropriate data byte on the data lines.
- 3. Activate the correct combination of control signals.
- 4. Raise EA/V_{PP} to 12V
- 5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The bytewrite cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89LV55 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on PO.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BUSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.





Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.





*Programming address line A14 (P3.0) is not the same as the external memory address line A14 (P2.6)

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all 1s. The chip erase operation must be executed before the code memory can be reprogrammed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 65H indicates 89LV55
- (032H) = FFH indicates 12V programming

18. Programming Interface

Every code byte in the Flash array can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Figure 18-1. Verifying the Flash Memory



Mode		RST	PSEN	ALE/PROG	EA/V _{PP}	P2.6	P2.7	P3.6
Write Code Data		н	L		12V	L	Н	Н
Read Code Data		н	L	Н	Н	L	L	Н
Write Lock	Bit-1	Н	L		12V	Н	Н	Н
	Bit-2	н	L		12V	н	н	L
	Bit-3	н	L		12V	н	L	Н
Chip Erase		Н	L		12V	Н	L	L
Read Signature Byte		Н	L	Н	Н	L	L	L
			00					

Table 18-1. Flash Programming Modes

Note: 1. Chip Erase requires a 10 ms PROG pulse.



P3.7

н

Н

н

L

L

L

L



19. Flash Programming and Verification Characteristics

 T_{A} = 0°C to 70°C, V_{CC} = 5.0V $\pm 10\%$

Symbol	Parameter	Min	Max	Units
V _{PP}	Programming Enable Voltage	11.5	12.5	V
I _{PP}	Programming Enable Current		1.0	mA
1/t _{CLCL}	Oscillator Frequency	3	12	MHz
t _{AVGL}	Address Setup to PROG Low	48t _{CLCL}		
t _{GHAX}	Address Hold After PROG	48t _{CLCL}		
t _{DVGL}	Data Setup to PROG Low	48t _{CLCL}		
t _{GHDX}	Data Hold After PROG	48t _{CLCL}		
t _{EHSH}	P2.7 (ENABLE) High to V _{PP}	48t _{CLCL}		
t _{SHGL}	V _{PP} Setup to PROG Low	10		μs
t _{GHSL}	V _{PP} Hold After PROG	10		μs
t _{GLGH}	PROG Width	1	110	μs
t _{AVQV}	Address to Data Valid		48t _{CLCL}	
t _{ELQV}	ENABLE Low to Data Valid		48t _{CLCL}	
t _{EHQZ}	Data Float After ENABLE	0	48t _{CLCL}	
t _{GHBL}	PROG High to BUSY Low		1.0	μs
t _{wc}	Byte Write Cycle Time		2.0	ms

20. Flash Programming and Verification Waveforms ($V_{PP} = 12V$)



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21. Absolute Maximum Ratings*

Voltage on Any Pin with Respect to Ground	1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

22. DC Characteristics

The values shown in this table are valid for $T_A = -40^{\circ}$ C to 85° C and $V_{CC} = 2.7$ V to 6.0V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V _{IL}	Input Low Voltage	(Except EA)	-0.5	0.2 V _{CC} - 0.1	V
V _{IL1}	Input Low Voltage (EA)		-0.5	0.2 V _{CC} - 0.3	V
V _{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V _{CC} + 0.9	V _{CC} + 0.5	V
V _{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V _{CC}	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage ⁽¹⁾ (Ports 1, 2, 3)	I _{OL} = 1.6 mA		0.45	v
V _{OL1}	Output Low Voltage ⁽¹⁾ (Port 0, ALE, PSEN)	I _{OL} = 3.2 mA		0.45	V
		$I_{OH} = -60 \ \mu A, \ V_{CC} = 5V \pm 10\%$	2.4		V
V _{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN)	I _{OH} = -25 μA	0.75 V _{CC}		V
		I _{OH} = -10 μA	0.9 V _{CC}		V
V _{OH1}		I_{OH} = -800 $\mu A,V_{CC}$ = 5V $\pm10\%$	2.4		V
	Output High Voltage (Port 0 in External Bus Mode)	I _{OH} = -300 μA	0.75 V _{CC}		V
		I _{OH} = -80 μA	0.9 V _{CC}		V
I	Logical 0 Input Current (Ports 1, 2, 3)	V _{IN} = 0.45V		-50	μA
I _{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V _{IN} = 2V		-650	μA
I _{LI}	Input Leakage Current (Port 0, EA)	$0.45 < V_{IN} < V_{CC}$		±10	μA
RRST	Reset Pulldown Resistor		50	300	kΩ
C _{IO}	Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^{\circ}C$		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
'CC	Power down Mode ⁽¹⁾	V _{CC} = 6V		100	μA
		$V_{CC} = 3V$		40	μA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA

Maximum I_{OL} per 8-bit port:

Port 0: 26 mA, Ports 1, 2, 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power-down is 2V.



24. External Program Memory Read Cycle



25. External Data Memory Read Cycle









26. External Data Memory Write Cycle

27. External Clock Drive Waveforms









- Notes: 1. XTAL1 tied to GND for $I_{\rm CC}$ (power-down)
 - 2. Lock bits programmed





33. Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
		AT89LV55-12AC	44A	Commercial
		AT89LV55-12JC	44J	$(0^{\circ} \text{C to } 70^{\circ} \text{C})$
		AT89LV55-12PC	40P6	
12	AT89LV55-12 AT89LV55-12 AT89LV55-12 AT89LV55-12	AT89LV55-12AI	44A	Industrial
		AT89LV55-12JI	44J	
		AT89LV55-12PI	40P6	(-40° C to 85° C)

Package Type				
44 A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)			
44J	44-lead, Plastic J-Leaded Chip Carrier (PLCC)			
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)			

34. Package Information

34.1 44A – TQFP





34.3 40P6 – PDIP







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