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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c12b0agn20000

- Sub clock: 32.768 kHz
- Built-in high-speed CR clock: 8 MHz
- Built-in low-speed CR clock: 100 kHz
- Main PLL clock 8MHz to 16MHz (Input), 75MHz to 150MHz (Output)

■ Resets
- Reset request from the INITX pin
- Power on reset
- Software reset
- Watchdog timer reset
- Low-voltage detection reset
- Clock supervisor reset

Clock Supervisor (CSV)
The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

■ If an external clock failure (clock stop) is detected, a reset is asserted.

■ If an external frequency anomaly is detected, an interrupt or a reset is asserted.

Low-Voltage Detector (LVD)
This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

■ LVD1: monitor V_{CC} and error reporting via an interrupt

■ LVD2: auto-reset operation

Low Power Consumption Mode
This series has six low power consumption modes.

■ Sleep

■ Timer

■ RTC

■ Stop

■ Deep standby RTC (selectable between keeping the value of RAM and not)

■ Deep standby Stop (selectable between keeping the value of RAM and not)

Peripheral Clock Gating
The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Debug

■ Serial Wire Debug Port (SW-DP)

■ Micro Trace Buffer (MTB)

Unique ID
A 41-bit unique value of the device has been set.

Power Supply

■ Wide voltage range: VCC = 1.65V to 3.6 V

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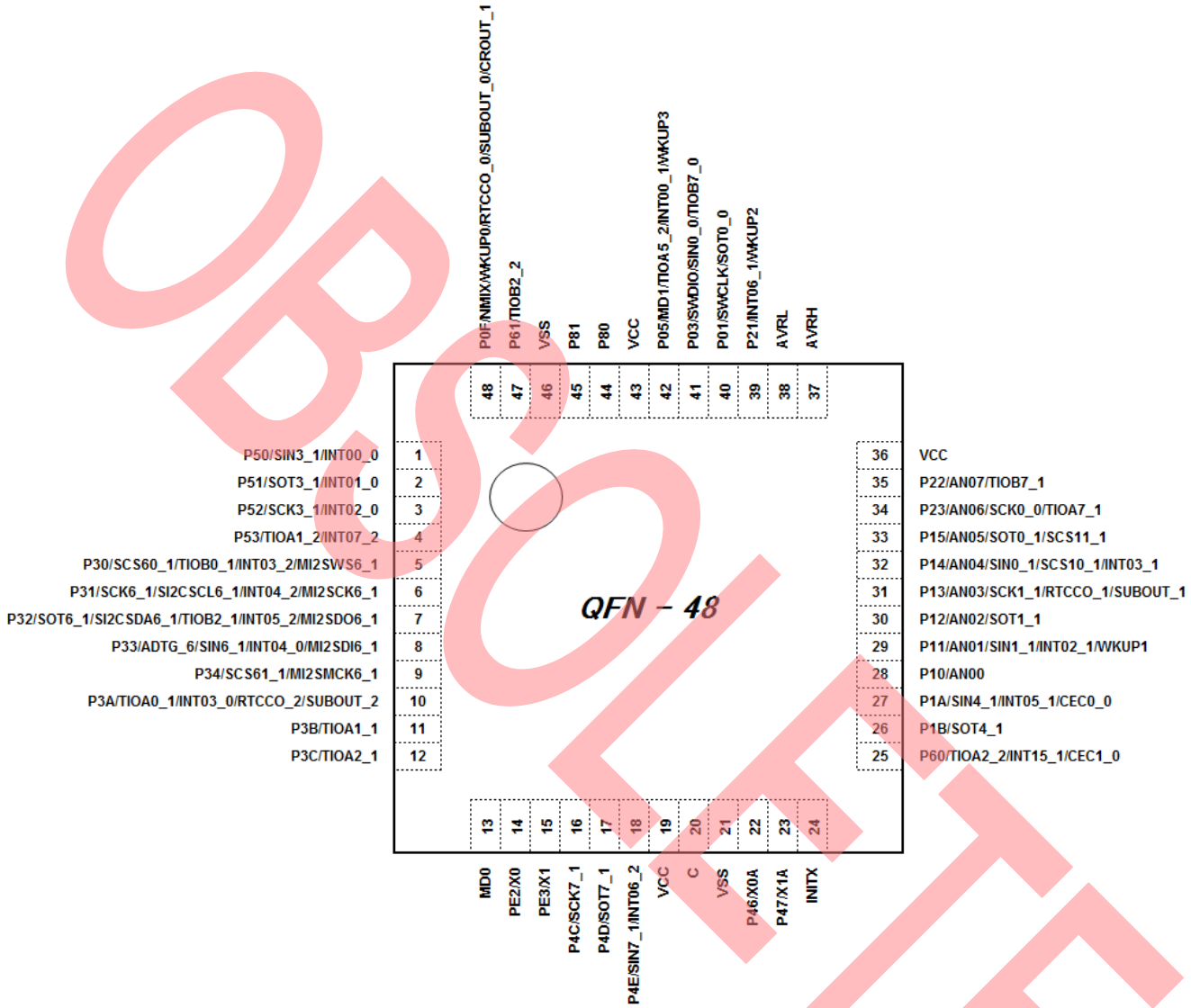
WNY048

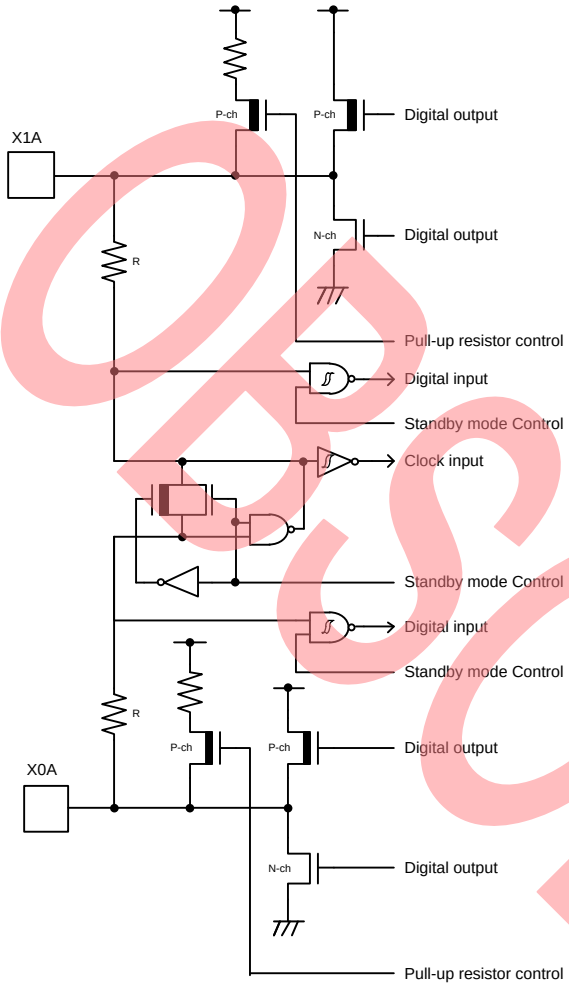
(TOP VIEW)



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
Multi-function Serial 4	SIN4_1	Multi-function serial interface ch.4 input pin	38	27	-
	SOT4_1 (SDA4_1)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I2C pin (operation mode 4).	37	26	-
	SCK4_1 (SCL4_1)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I2C pin (operation mode 4).	36	-	-
	CTS4_1	Multi-function serial interface ch4 CTS input pin	35	-	-
	RTS4_1	Multi-function serial interface ch4 RTS output pin	34	-	-
Multi-function Serial 6	SIN6_1	Multi-function serial interface ch.6 input pin	8	8	7
	SOT6_1 (SDA6_1)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA6 when used as an I2C pin (operation mode 4).	7	7	6
	SCK6_1 (SCL6_1)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when used as a CSIO (operation mode 2) and as SCL6 when used as an I2C pin (operation mode 4).	6	6	5
	SCS60_1	Multi-function serial interface ch.6 serial chip select 0 input/output pin.	5	5	-
	SCS61_1	Multi-function serial interface ch.6 serial chip select 1 output pin.	9	9	-
	SCS62_1	Multi-function serial interface ch.6 serial chip select 2 output pin.	10	-	-
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	26	18	-
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA7 when used as an I2C pin (operation mode 4).	25	17	-
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when used as a CSIO (operation mode 2) and as SCL7 when used as an I2C pin (operation mode 4).	24	16	-

Type	Circuit	Remarks
C		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33kΩ I_{OH}= -4mA, I_{OL}= 4mA

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

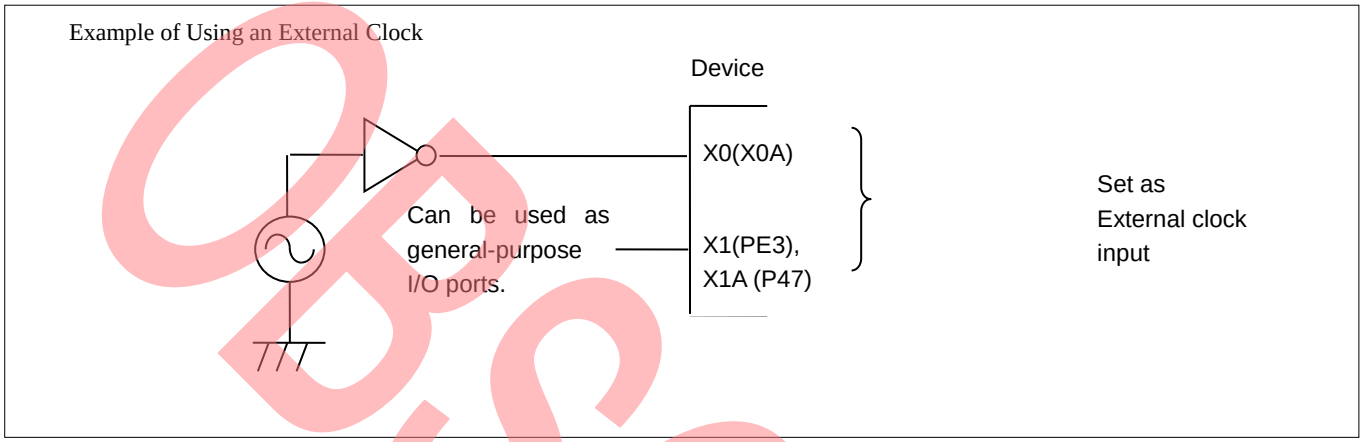
(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

However in the Deep Standby mode, an external clock as an input of the sub clock cannot be used.



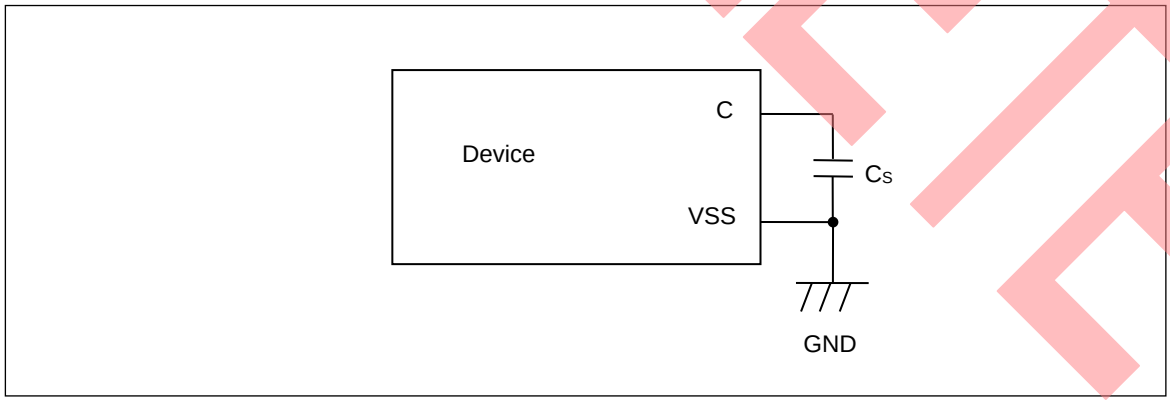
Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.

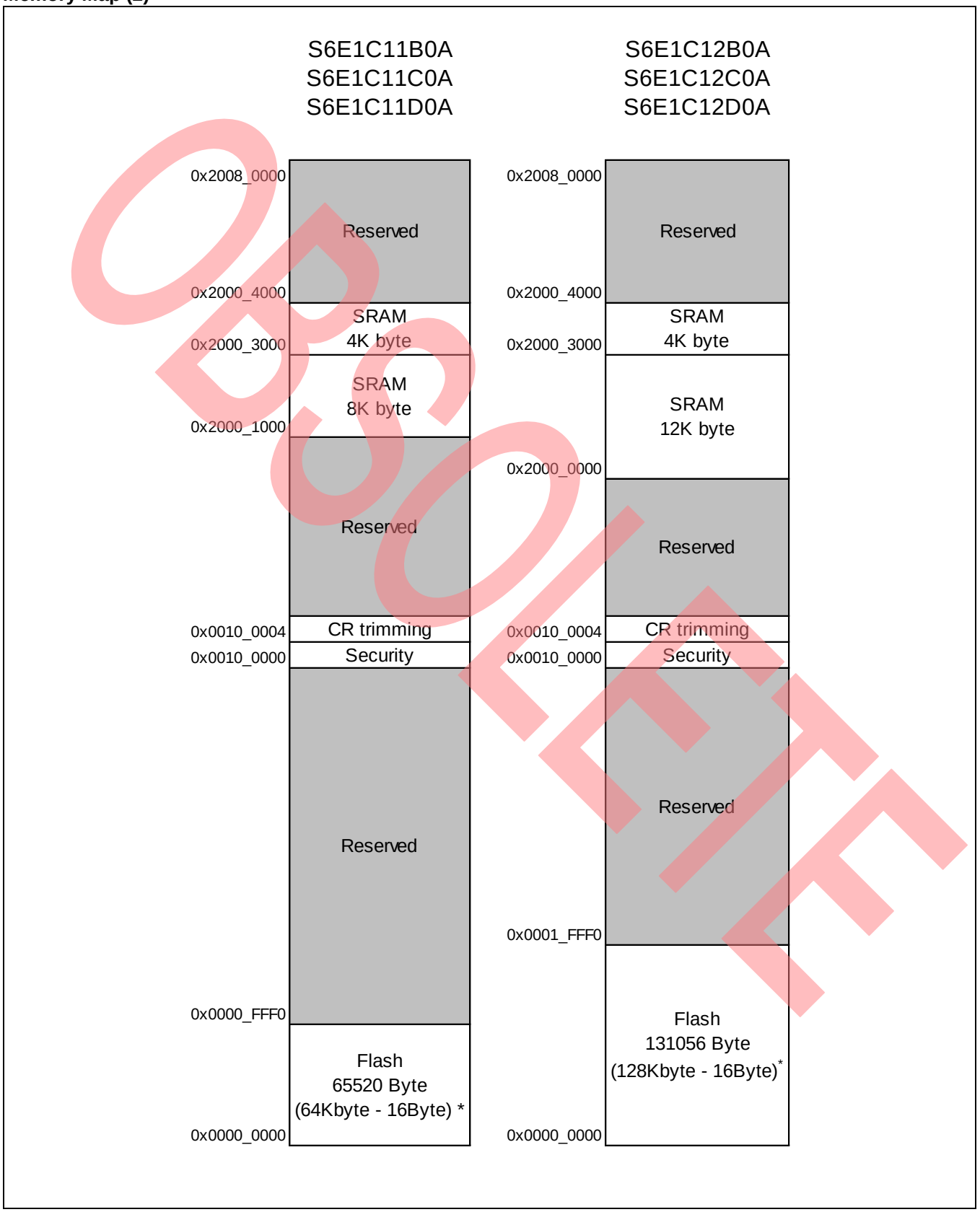
Incidentally, the C pin becomes floating in Deep standby mode.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Memory Map (2)



*: See "S6E1C1/C3 Series Flash Programming Manual" to check details of the Flash memory.

Type
This indicates a pin status type that is shown in “pin list table” in “4. List of Pin Functions”

Selected Pin function
This indicates a pin function that is selected by user program.

CPU state
This indicates a state of the CPU that is shown below.

(1) Reset state.
CPU is initialized by Power-on reset or a reset due to low Power voltage supply.

(2) Reset state.
CPU is initialized by INITX input signal or system initialization after power on reset.

(3) Run mode or SLEEP mode state.

(4) Timer mode, RTC mode or STOP mode state.
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0".

(5) Timer mode, RTC mode or STOP mode state.
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1".

(6) Deep standby STOP mode or Deep standby RTC mode state,
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0"

(7) Deep standby STOP mode or Deep standby RTC mode state,
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1"

(8) Run mode state after returning from Deep Standby mode.
(I/O state hold function(CONTX) is fixed at 1)

Each pin status
The meaning of the symbols in the pin status table is as follows.

IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off by fixed 0.
IE	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is not shut off.
IP	Digital output is disabled. (Hi-Z) Pull up register is defined by the value of the PCR register. Digital input is not shut off.
IE/IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off in case of the OSC stop. Digital input is not shut off in case of the OSC operation.
OE	The OSC is in operation state. However, it may be stopped in some operation mode of the CPU. For detail, see chapter “Low Power Consumption Mode” in peripheral manual.
OS	The OSC is in stop state. (Hi-Z)
PC	Digital output and pull up register is controlled by the register in the GPIO or peripheral function. Digital input is not shut off
CP	Digital output is controlled by the register in the GPIO or peripheral function. Pull up register is off. Digital input is not shut off.
HC	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is not shut off
HS	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is shut off
GS	Digital output and pull up register is copied the GPIO status that is immediately prior to entering the current CPU state and the status is maintained. Digital input is shut off

Additional note

Additional note is described below.

*1 In this type, when internal oscillation function is selected, digital output is disabled. (Hi-Z) pull up register is off, digital input is shut off by fixed 0.

*2 In this type, when Digital I/O function is selected, internal oscillation function is disabled.

*3 In this type, when analog input function is selected, digital output is disabled, (Hi-Z). pull up register is off, digital input is shut off by fixed 0.

*4 In this type, when Digital I/O function is selected, analog input function is not available.

*5 In this case, PCR register is initialized to “1”. Pull up register is on.

*6 This pin does not have pull up register.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 4.6	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	Vcc + 0.5 (≤ 4.6 V)	V	
L level maximum output current*4	I_{OL}	-	10	mA	4 mA type
L level average output current*5	I_{OLAV}	-	4	mA	4 mA type
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	I_{OH}	-	- 10	mA	4 mA type
H level average output current*5	I_{OHAV}	-	- 4	mA	4 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	200	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that V_{SS}= 0 V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not to exceed V_{CC} + 0.5 V at power-on.

*4: The maximum output current is the peak value for a single pin.

*5: The average output is the average current for a single pin over a period of 100 ms.

*6: The total average output current is the average current for all pins over a period of 100 ms.

<WARNING>

- *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

Parameter	Symbol (Pin Name)	Conditions			Value		Unit	Remarks
					Typ	Max		
Power supply current	I_{CCHD} (VCC)	Deep standby Stop mode	RAM off	Ta=25°C Vcc=3.3 V	0.58	1.85	µA	*1, *2
				Ta=25°C Vcc=1.65 V	0.56	1.83	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	46	µA	*1, *2
			RAM on	Ta=25°C Vcc=3.3 V	0.78	6.6	µA	*1, *2
				Ta=25°C Vcc=1.65 V	0.76	6.6	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	88	µA	*1, *2
	I_{CCRD} (VCC)	Deep standby RTC mode	RAM off	Ta=25°C Vcc=3.3 V	1.16	2.4	µA	*1, *2
				Ta=25°C Vcc=1.65 V	1.15	2.4	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	46	µA	*1, *2
			RAM on	Ta=25°C Vcc=3.3 V	1.37	7.2	µA	*1, *2
				Ta=25°C Vcc=1.65 V	1.35	7.2	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	88	µA	*1, *2

*1: All ports are fixed. LVD off.
*2: When CALDONE bit(CAL_CTL:CALDONE) is “1”. In case of “0”, Bipolar Vref current is added.

11.3.2 Pin Characteristics

(V_{CC} = 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	V_{CC} +0.3	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	V_{SS} +5.5	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V		-	$V_{CC} \times 0.3$		
H level output voltage	V_{OH}	4 mA type	$V_{CC} \geq 2.7$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 2.7$ V, I_{OH} = - 2 mA	V_{CC} - 0.45				
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 2.7$ V, I_{OL} 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 2.7$ V, I_{OL}=2 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq 2.7$ V	21	33	48	kΩ	
			$V_{CC} < 2.7$ V	-	-	88		
Input capacitance	C_{IN}	Other than VCC, VSS, AVRH	-	-	5	15	pF	

11.4.4 Operating Conditions of Main PLL (In the Case of Using the Main Clock as the Input Clock of the PLL)

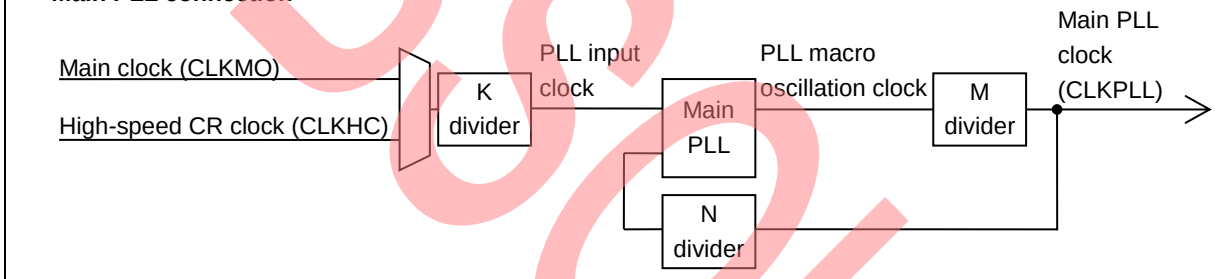
(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	50	-	-	µs	
PLL input clock frequency	F_{PLLI}	8	-	16	MHz	
PLL multiple rate	-	5	-	18	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

Main PLL connection



11.4.5 Operating Conditions of Main PLL (In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

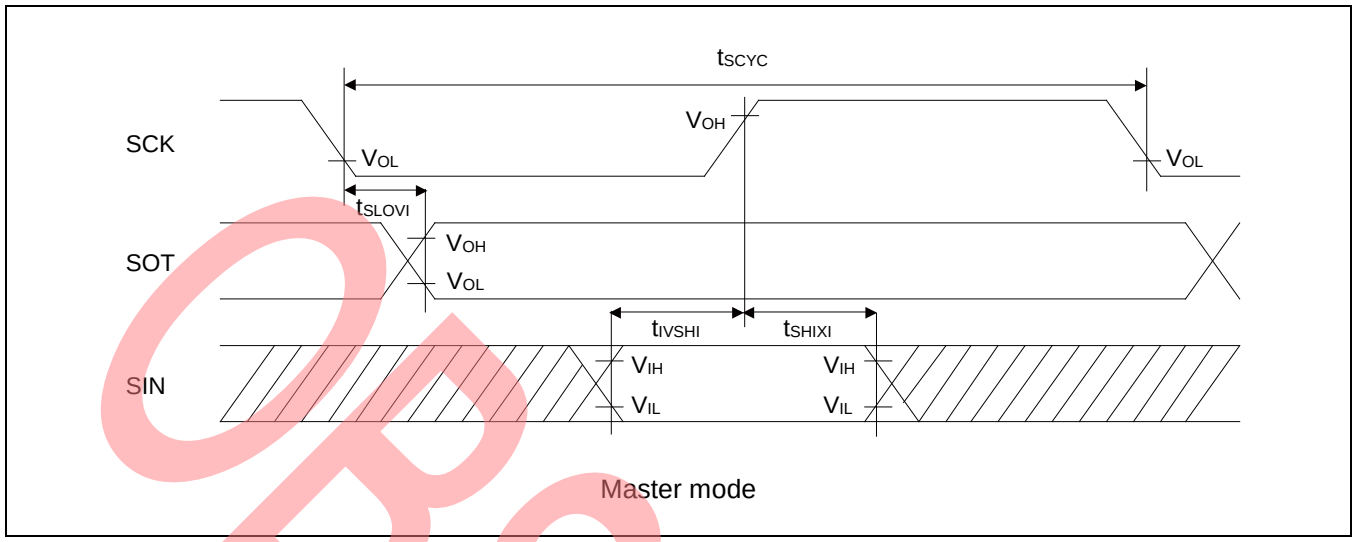
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	50	-	-	µs	
PLL input clock frequency	F_{PLLI}	7.84	8	8.16	MHz	
PLL multiple rate	-	9	-	18	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40.8	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

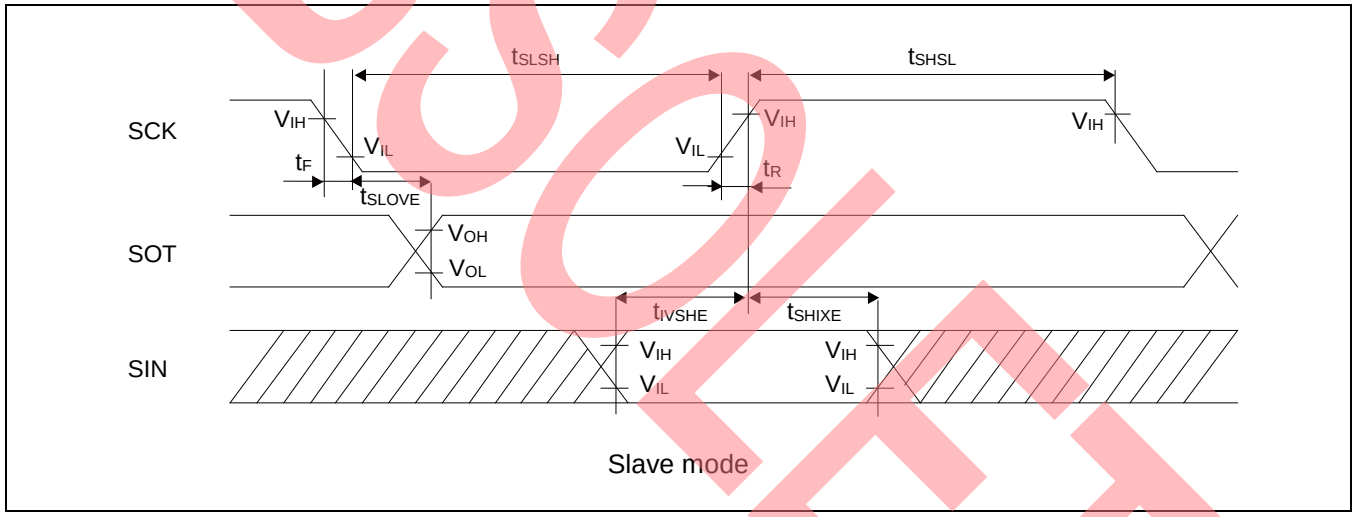
*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

Note:

- *For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency and temperature have been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.*



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

11.4.13 Smart Card Interface Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output rising time	t_R	ICx_VCC, ICx_RST, ICx_CLK, ICx_DATA	C_L=30 pF	4	20	ns	
Output falling time	t_F			4	20	ns	
Output clock frequency	f_{CLK}	ICx_CLK		-	20	MHz	
Duty cycle	Δ			45%	55%		

■External pull-up resistor (20 kΩ to 50 kΩ) must be applied to ICx_CIN pin when it's used as smart card reader function.

11.6 Low-Voltage Detection Characteristics

11.6.1 Low-Voltage Detection Reset

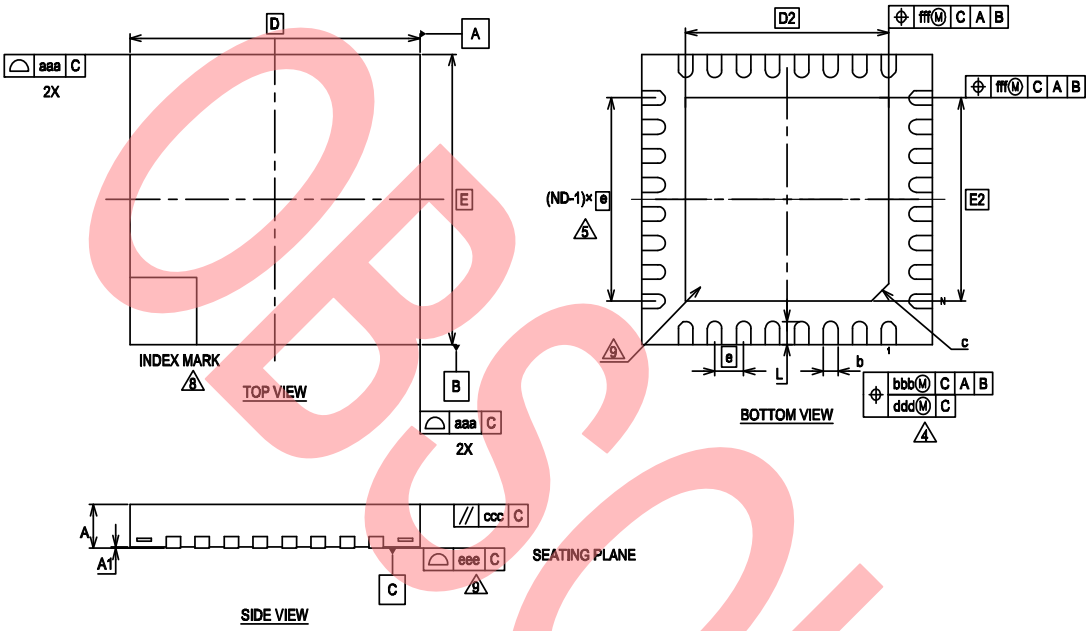
(T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	Fixed[*1]	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160× t_{CYCP}[*2]	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*1: The value of low voltage detection reset is always fixed.

*2: t_{CYCP} indicates the APB1 bus clock cycle time.

WNU032 VERY THIN PLASTIC QUAD FLAT NO LEAD PACKAGES



SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.80	PROFILE
A_1	0.00	—	0.05	TERMINAL HEIGHT
D		5.00 BSC		BODY SIZE
E		5.00 BSC		BODY SIZE
b	0.20	0.25	0.30	TERMINAL WIDTH
D_2		3.20 BSC		EXPOSED PAD SIZE
E_2		3.20 BSC		EXPOSED PAD SIZE
e		0.50 BSC		TERMINAL PITCH
c		0.25 REF		EXPOSED PAD CHAMFER
L	0.35	0.40	0.45	TERMINAL LENGTH

N	32	TERMINAL COUNT
aaa	0.10	
bbb	0.10	
ccc	0.10	
ddd	0.05	
eee	0.08	
fff	0.10	

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Rev. 0A

Document History

Document Title: S6E1C1 Series 32-bit ARM® Cortex®-M0+ FM0+ Microcontroller
Document Number: 002-00234

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4896074	TEKA	08/31/2015	New Spec.
*A	4955136	TEKA	10/9/2015	AC/DC characteristics updated. Typo fixed in “List of Pin Functions”.
*B	5158709	YUKT	03/04/2016	Added the frequency value of “Ta = - 10°C to + 105°C” on “11.4.3 Built-in CR Oscillation Characteristics”. Added the remark of “VCC < 0.2V” on “11.4.7 Power-on Reset Timing”. Added the measure condition(*9) of ICC on “11.3.1 Current Rating”. Changed the package outlines to cypress format on “13. Package Dimensions”. Changed the package codes to cypress codes on “3. Pin Assignment” and “12. Ordering Information”.
*C	5760029	MBGR	06/01/2017	Consolidated the S6E1C datasheets in a single specification 002-00233, Rev. *D.