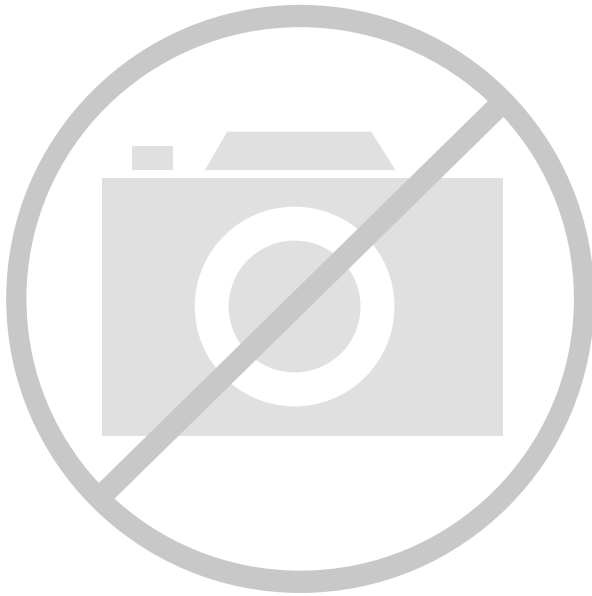




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## Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

### Details

|                                 |                                                                                                                                                                                         |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                  | Obsolete                                                                                                                                                                                |
| Core Processor                  | MIPS-II                                                                                                                                                                                 |
| Number of Cores/Bus Width       | 1 Core, 32-Bit                                                                                                                                                                          |
| Speed                           | 133MHz                                                                                                                                                                                  |
| Co-Processors/DSP               | -                                                                                                                                                                                       |
| RAM Controllers                 | SDRAM                                                                                                                                                                                   |
| Graphics Acceleration           | No                                                                                                                                                                                      |
| Display & Interface Controllers | -                                                                                                                                                                                       |
| Ethernet                        | -                                                                                                                                                                                       |
| SATA                            | -                                                                                                                                                                                       |
| USB                             | -                                                                                                                                                                                       |
| Voltage - I/O                   | 2.5V, 3.3V                                                                                                                                                                              |
| Operating Temperature           | 0°C ~ 70°C (TA)                                                                                                                                                                         |
| Security Features               | -                                                                                                                                                                                       |
| Package / Case                  | 208-BFQFP                                                                                                                                                                               |
| Supplier Device Package         | 208-PQFP (28x28)                                                                                                                                                                        |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t332-133dh">https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t332-133dh</a> |

- ◆ **Serial Peripheral Interface (SPI) master mode interface**
- ◆ **UART Interface**
  - 16550 compatible UART
  - Baud rate support up to 1.5 Mb/s
- ◆ **Memory & Peripheral Controller**
  - 6 banks, up to 8MB per bank
  - Supports 8-, 16-, and 32-bit interfaces
  - Supports Flash ROM, SRAM, dual-port memory, and peripheral devices
  - Supports external wait-state generation
  - 8-bit boot PROM support
  - Flexible I/O timing protocols
- ◆ **4 DMA Channels**
  - 4 general purpose DMA, each with endianness swappers and byte lane data alignment
  - Supports scatter/gather, chaining via linked lists of records
  - Supports memory-to-memory, memory-to-I/O, memory-to-PCI, PCI-to-PCI, and I/O-to-I/O transfers
  - Supports unaligned transfers
  - Supports burst transfers
  - Programmable DMA bus transactions burst size (up to 16 bytes)
- ◆ **PCI Bus Interface**
  - 32-bit PCI, up to 50 MHz
  - Revision 2.2 compatible
  - Target or master
  - Host or satellite
  - Two slot PCI arbiter
  - Serial EEPROM support, for loading configuration registers
- ◆ **Off-the-shelf development tools**
- ◆ **JTAG Interface (IEEE Std. 1149.1 compatible)**
- ◆ **208 QFP Package**

- ◆ **3.3V or 2.5V core supply with 3.3V I/O supply**
  - 3.3V core supply is 5V I/O tolerant
- ◆ **EJTAG in-circuit emulator interface**

## CPU Execution Core

The RC32332 integrates the RISCore 32300, the same CPU core found in the award-winning RC32364 microprocessor. The RISCore 32300 implements the Enhanced MIPS-II ISA. Thus, it is upwardly compatible with applications written for a wide variety of MIPS architecture processors, and it is kernel compatible with the modern operating systems that support IDT's 64-bit RISController product family. The RISCore 32300 was explicitly defined and designed for integrated processor products such as the RC32332. Key attributes of the execution core found within this product include:

- ◆ High-speed, 5-stage scalar pipeline executes to 150MHz. This high performance enables the RC32332 to perform a variety of performance intensive tasks, such as routing, DSP algorithms, etc.
- ◆ 32-bit architecture with enhancements of key capabilities. Thus, the RC32332 can execute existing 32-bit programs, while enabling designers to take advantage of recent advances in CPU architecture.
- ◆ Count leading-zeroes/ones. These instructions are common to a wide variety of tasks, including modem emulation, voice over IP compression and decompression, etc.
- ◆ Cache PREFetch instruction support, including a specialized form intended to help memory coherency. System programmers can allocate and stage the use of memory bandwidth to achieve maximum performance.
- ◆ 8KB of 2-way set associative instruction cache

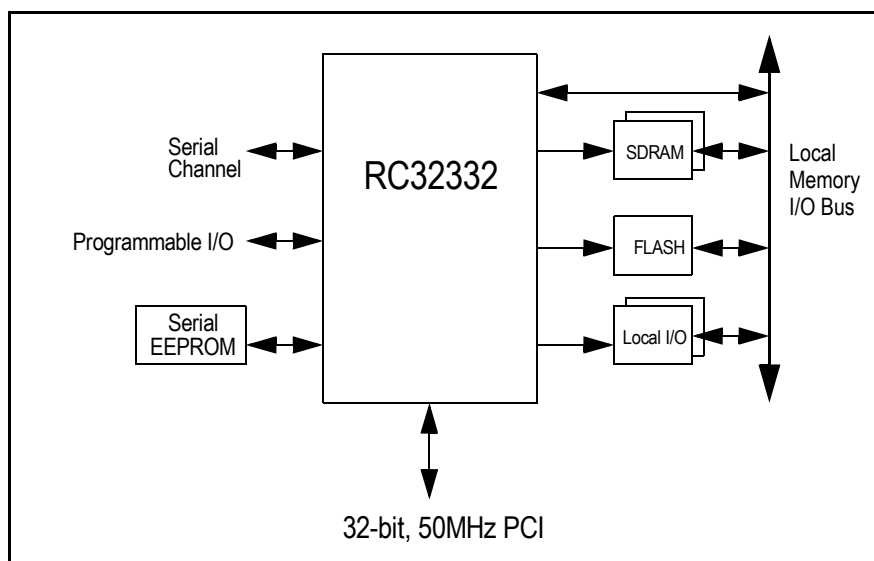


Figure 2 RC32332 Based System Diagram

Secondly, the RC32332 implements additional reporting signals intended to simplify the task of system debugging when using a logic analyzer. This product allows the logic analyzer to differentiate transactions initiated by DMA from those initiated by the CPU and further allows CPU transactions to be sorted into instruction fetches vs. data fetches.

Finally, the RC32332 implements a full boundary scan capability, allowing board manufacturing diagnostics and debug.

## Packaging

The RC32332 is packaged using a 208 Quad Flat Pack (QFP) package.

## Thermal Considerations

The RC32332 consumes less than 2.0 W peak power. The device is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices; -40° to +85° C for industrial temperature devices.

## Revision History

**November 15, 2000:** Initial publication.

**December 12, 2000:** Changed Max values for `cpu_masterclock` period in Table 5 and added footnote. In Table 1, added 2nd alternate function for `spi_mosi`, `spi_miso`, `spi_sck`. In Table 11, added "2" in Alt column for pins 186, 187, 188. In RC32332 Alternate Signal Functions table, added pin names in Alt #2 column for pins 186, 187, 188.

**January 4, 2001:** In Table 6 under Interrupt Handling, changed `Tdoh9` to `Thld13` and moved the values for `Tsu9` from the Max to the Min column.

**February 23, 2001:** In Table 1, changed alternate function for `uart_tx[0]` from `PIO[3]` to `PIO[1]`. In Table 11, changed the number of alternate pins for Pin 156 from 1 to 2. In Table 12, added `PIO[7]` to Alt #2 column for Pin 156 and changed `PIO[3]` to `PIO[1]` for Pin 207.

**March 13, 2001:** Changed upper ambient temperature for industrial and commercial uses from +70° C to +85° C.

**June 7, 2001:** In the Clock Parameters table, added footnote 3 to `output_clk` category and added NA to Min and Max columns. In Figure 3 (Reset Specification), enhanced signal line for `cpu_masterclk`. In Local System Interface section of AC Timing Characteristics table, changed values in Min column for last category of signals (`Tdoh3`) from 1.5 to 2.5 for both speeds. In SDRAM Controller section of same table, changed values in Min column for last category of signals (9 signals) from 1 to 2.5 for both speeds.

**September 14, 2001:** In the Reset category of Table 6: switched `mem_addr[19:17]` from `Tsu22` and `Thld22` to `Tsu10` and `Thld10`; switched `mem_addr[22:20]` from `Tsu10` and `Thld10` to `Tsu22` and `Thld22`; moved `ejtag_pcst[2:0]` from Reset to Debug Interface category under `Tsu20` and `Thld20`.

**November 1, 2001:** Added Input Voltage Undershoot parameter and 2 footnotes to Table 10. Changed to DH package.

**May 2, 2002:** Changed from PCI 2.1 to 2.2 compliant. Added 512 MB SDRAM support. Changed upper ambient temperature for commercial uses back from +85° C to +70° C (changed erroneously from 70 to 85 on March 13, 2001). Added Reset State Status column to Table 1. Revised description of `jtag_trst_n` in Table 1 and changed this pin to a pull-down instead of a pull-up.

**July 3, 2002:** This data sheet now describes revision Y silicon and is no longer applicable to revision Z.

**July 12, 2002:** Added 150MHz speed grade. In Table 6: DMA section, changed `Thld9` Min values from 2 to 1; in PIO section, changed `Thld9` Min values from 2 to 1. Changed revision Y data sheet from Preliminary to Final.

**September 18, 2002:** Added `cpu_coldreset_n` rise time to Table 5, Clock Parameters. Added `mem_addr[16]` and `sdram_addr[16]` to Tables 1 and 12. Changed Logic Diagram to include `sdram_addr[16]`.

**December 18, 2002:** In the Reset section of Table 6, AC Timing Characteristics, setup and hold time categories for `cpu_coldreset_n` have been deleted.

**September 2, 2003:** Added 2.5V version of device. Changed tables to include 2.5V values where appropriate. Added a Power Consumption table, Temperature and Voltage table, and Power Curves for the 2.5V device. In the PCI category of Table 6, created separate sections for 3.3V and 2.5V devices and in 2.5V section changed time to 4 ns for `pci_cbe_n[3:0]`, `pci_frame_n`, `pci_trdy_n`, and `pci_irdy_n`. In Table 8, added 3 new categories (Input Pads, PCI Input Pads, and All Pads) and added footnotes 2 and 3. In Table 13, pins 181 and 184 were changed from Vcc Core to Vcc I/O.

**March 24, 2004:** In Table 1, changed description in Satellite Mode for `pci_rst_n`. Specified "cold" reset on pages 12 and 13. Changed several values in Table 12, Absolute Maximum Ratings, and changed footnote 1 to that table.

**May 4, 2004:** Revised values in Table 9, Power Consumption.

## Pin Description Table

The following table lists the pins provided on the RC32332. Note that those pin names followed by “\_n” are active-low signals. All external pull-ups and pull-downs require 10 kΩ resistor.

| Name                          | Type                   | Reset State Status   | Drive Strength Capability  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
|-------------------------------|------------------------|----------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-------------|--|--|--|--|-------------|-------------|-------------|-------------|--------------|-------------|-------------|-------------|-------------|--------|-------------|-------------|-------------|-------------|--------|------------------------|-------------|-----------------------|-----------------------|-------|------------------------|-------------|-------------|-------------------|
| <b>Local System Interface</b> |                        |                      |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_data[31:0]                | I/O                    | Z                    | High                       | <b>Local system data bus</b><br>Primary data bus for memory. I/O and SDRAM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_addr[22:2]                | I/O                    | [22:10] Z<br>[9:2] L | [22:17] Low<br>[16:2] High | <b>Memory Address Bus</b><br>These signals provide the Memory or DRAM address, during a Memory or DRAM bus transaction. During each word data, the address increments either in linear or sub-block ordering, depending on the transaction type. The table below indicates how the memory write enable signals are used to address discreet memory port width types. <table border="1"> <thead> <tr> <th>Port Width</th><th colspan="4">Pin Signals</th></tr> <tr> <th></th><th>mem_we_n[3]</th><th>mem_we_n[2]</th><th>mem_we_n[1]</th><th>mem_we_n[0]</th></tr> </thead> <tbody> <tr> <td>DMA (32-bit)</td><td>mem_we_n[3]</td><td>mem_we_n[2]</td><td>mem_we_n[1]</td><td>mem_we_n[0]</td></tr> <tr> <td>32-bit</td><td>mem_we_n[3]</td><td>mem_we_n[2]</td><td>mem_we_n[1]</td><td>mem_we_n[0]</td></tr> <tr> <td>16-bit</td><td>Byte High Write Enable</td><td>mem_addr[1]</td><td>Not Used (Driven Low)</td><td>Byte Low Write Enable</td></tr> <tr> <td>8-bit</td><td>Not Used (Driven High)</td><td>mem_addr[1]</td><td>mem_addr[0]</td><td>Byte Write Enable</td></tr> </tbody> </table><br>mem_addr[22] Alternate function: reset_boot_mode[1].<br>mem_addr[21] Alternate function: reset_boot_mode[0].<br>mem_addr[20] Alternate function: reset_pci_host_mode.<br>mem_addr[19] Alternate function: modebit [9].<br>mem_addr[18] Alternate function: modebit [8].<br>mem_addr[17] Alternate function: modebit [7].<br>mem_addr[16] Alternate function: sdram_addr[16].<br>mem_addr[15] Alternate function: sdram_addr[15].<br>mem_addr[14] Alternate function: sdram_addr[14].<br>mem_addr[13] Alternate function: sdram_addr[13].<br>mem_addr[11] Alternate function: sdram_addr[11].<br>mem_addr[10] Alternate function: sdram_addr[10].<br>mem_addr[9] Alternate function: sdram_addr[9].<br>mem_addr[8] Alternate function: sdram_addr[8].<br>mem_addr[7] Alternate function: sdram_addr[7].<br>mem_addr[6] Alternate function: sdram_addr[6].<br>mem_addr[5] Alternate function: sdram_addr[5].<br>mem_addr[4] Alternate function: sdram_addr[4].<br>mem_addr[3] Alternate function: sdram_addr[3].<br>mem_addr[2] Alternate function: sdram_addr[2]. | Port Width | Pin Signals |  |  |  |  | mem_we_n[3] | mem_we_n[2] | mem_we_n[1] | mem_we_n[0] | DMA (32-bit) | mem_we_n[3] | mem_we_n[2] | mem_we_n[1] | mem_we_n[0] | 32-bit | mem_we_n[3] | mem_we_n[2] | mem_we_n[1] | mem_we_n[0] | 16-bit | Byte High Write Enable | mem_addr[1] | Not Used (Driven Low) | Byte Low Write Enable | 8-bit | Not Used (Driven High) | mem_addr[1] | mem_addr[0] | Byte Write Enable |
| Port Width                    | Pin Signals            |                      |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
|                               | mem_we_n[3]            | mem_we_n[2]          | mem_we_n[1]                | mem_we_n[0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| DMA (32-bit)                  | mem_we_n[3]            | mem_we_n[2]          | mem_we_n[1]                | mem_we_n[0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| 32-bit                        | mem_we_n[3]            | mem_we_n[2]          | mem_we_n[1]                | mem_we_n[0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| 16-bit                        | Byte High Write Enable | mem_addr[1]          | Not Used (Driven Low)      | Byte Low Write Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| 8-bit                         | Not Used (Driven High) | mem_addr[1]          | mem_addr[0]                | Byte Write Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_cs_n[5:0]                 | Output                 | H                    | Low                        | <b>Memory Chip Select Negated</b> Recommend an external pull-up.<br>Signals that a Memory Bank is actively selected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_oe_n                      | Output                 | H                    | High                       | <b>Memory Output Enable Negated</b> Recommend an external pull-up.<br>Signals that a Memory Bank can output its data lines onto the cpu_ad bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_we_n[3:0]                 | Output                 | H                    | High                       | <b>Memory Write Enable Negated Bus</b><br>Signals which bytes are to be written during a memory transaction. Bits act as Byte Enable and mem_addr[1:0] signals for 8-bit or 16-bit wide addressing.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |            |             |  |  |  |  |             |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |

Table 1 Pin Descriptions (Part 1 of 6)

| Name           | Type   | Reset State Status | Drive Strength Capability | Description                                                                                                                                                                                                                                                                                        |
|----------------|--------|--------------------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| mem_wait_n     | Input  |                    | —                         | <b>Memory Wait Negated</b> Requires an external pull-up.<br>SRAM/IOI/IOM modes: Allows external wait-states to be injected during the last cycle before data is sampled.<br>DPM (dual-port) mode: Allows dual-port busy signal to restart memory transaction.<br>Alternate function: sdram_wait_n. |
| mem_245_oe_n   | Output | H                  | Low                       | <b>Memory FCT245 Output Enable Negated</b><br>Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to a memory or I/O bank.                                                                                                                        |
| mem_245_dt_r_n | Output | Z                  | High                      | <b>Memory FCT245 Direction Xmit/Rcv Negated</b> Recommend an external pull-up.<br>Alternate function: cpu_dt_r_n. See CPU Core Specific Signals below.                                                                                                                                             |
| output_clk     | Output | cpu_masterclk      | High                      | <b>Output Clock</b><br>Optional clock output.                                                                                                                                                                                                                                                      |

**PCI Interface**

|                |                    |   |     |                                                                                                                                                                                                                             |
|----------------|--------------------|---|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| pci_ad[31:0]   | I/O                | Z | PCI | <b>PCI Multiplexed Address/Data Bus</b><br>Address driven by Bus Master during initial frame_n assertion, and then the Data is driven by the Bus Master during writes; or the Data is driven by the Bus Slave during reads. |
| pci_cbe_n[3:0] | I/O                | Z | PCI | <b>PCI Multiplexed Command/Byte Enable Bus</b><br>Command (not negated) Bus driven by the Bus Master during the initial frame_n assertion. Byte Enable Negated Bus driven by the Bus Master during the data phase(s).       |
| pci_par        | I/O                | Z | PCI | <b>PCI Parity</b><br>Even parity of the pci_ad[31:0] bus. Driven by Bus Master during Address and Write Data phases. Driven by the Bus Slave during the Read Data phase.                                                    |
| pci_frame_n    | I/O                | Z | PCI | <b>PCI Frame Negated</b><br>Driven by the Bus Master. Assertion indicates the beginning of a bus transaction. De-assertion indicates the last datum.                                                                        |
| pci_trdy_n     | I/O                | Z | PCI | <b>PCI Target Ready Negated</b><br>Driven by the Bus Slave to indicate the current datum can complete.                                                                                                                      |
| pci_irdy_n     | I/O                | Z | PCI | <b>PCI Initiator Ready Negated</b><br>Driven by the Bus Master to indicate that the current datum can complete.                                                                                                             |
| pci_stop_n     | I/O                | Z | PCI | <b>PCI Stop Negated</b><br>Driven by the Bus Slave to terminate the current bus transaction.                                                                                                                                |
| pci_idsel_n    | Input              |   | —   | <b>PCI Initialization Device Select</b><br>Uses pci_req_n[2] pin. See the PCI subsection.                                                                                                                                   |
| pci_perr_n     | I/O                | Z | PCI | <b>PCI Parity Error Negated</b><br>Driven by the receiving Bus Agent 2 clocks after the data is received, if a parity error occurs.                                                                                         |
| pci_serr_n     | I/O Open-collector | Z | PCI | <b>System Error</b> Requires an external pull-up.<br>Driven by any agent to indicate an address parity error, data parity during a Special Cycle command, or any other system error.                                        |
| pci_clk        | Input              |   | —   | <b>PCI Clock</b><br>Clock for PCI Bus transactions. Uses the rising edge for all timing references.                                                                                                                         |
| pci_rst_n      | Input              | L | —   | <b>PCI Reset Negated</b><br>Host mode: Resets all PCI related logic.<br>Satellite mode: Resets all PCI related logic and also warm resets the 32332.                                                                        |
| pci_devsel_n   | I/O                | Z | PCI | <b>PCI Device Select Negated</b><br>Driven by the target to indicate that the target has decoded the present address as a target address.                                                                                   |

Table 1 Pin Descriptions (Part 2 of 6)

| Name                                                     | Type                  | Reset State Status                    | Drive Strength Capability | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------------------------------------------|-----------------------|---------------------------------------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| pci_req_n[2]                                             | Input                 | Z                                     | —                         | <b>PCI Bus Request #2 Negated</b> Requires an external pull-up.<br>Host mode: pci_req_n[2] is an input indicating a request from an external device.<br>Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write.<br>Alternate function: pci_idsel (satellite).                                                                                                                                                                                   |
| pci_req_n[0]                                             | I/O                   | Z                                     | High                      | <b>PCI Bus Request #0 Negated</b> Requires an external pull-up for burst mode.<br>Host mode: pci_req_n[0] is an input indicating a request from an external device.<br>Satellite mode: pci_req_n[0] is an output indicating a request from this device.                                                                                                                                                                                                                                       |
| pci_gnt_n[2]                                             | Output                | Z <sup>1</sup>                        | High                      | <b>PCI Bus Grant #2 Negated</b> Recommend an external pull-up.<br>Host mode: pci_gnt_n[2] is an output indicating a grant to an external device.<br>Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin. External pull-up is required.<br>Alternate function: pci_inta_n (satellite).                                                                                                                                                                                           |
| pci_gnt_n[1]<br>(can only be used as alternate function) | I/O                   | X for 1 pci clock then H <sup>2</sup> | High                      | <b>PCI Bus Grant #1 Negated</b> Recommend external pull-up.<br>Host mode: not used as pci_gnt_n[1]. Must be used as alternate function PIO[7].<br>Satellite mode: Not used as pci_gnt_n[1]. Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32332 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time.<br>1st Alternate function: pci_eeprom_cs (satellite).<br>2nd Alternate function: PIO[7]. |
| pci_gnt_n[0]                                             | I/O                   | Z                                     | High                      | <b>PCI Bus Grant #0 Negated</b><br>Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up.<br>Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Requires external pull-up.                                                                                                                                                                                                                                       |
| pci_inta_n                                               | Output Open-collector | Z                                     | PCI                       | <b>PCI Interrupt #A Negated</b><br>Uses pci_gnt_n[2]. See the PCI subsection.                                                                                                                                                                                                                                                                                                                                                                                                                 |
| pci_lock_n                                               | Input                 |                                       | —                         | <b>PCI Lock Negated</b><br>Driven by the Bus Master to indicate that an exclusive operation is occurring.                                                                                                                                                                                                                                                                                                                                                                                     |

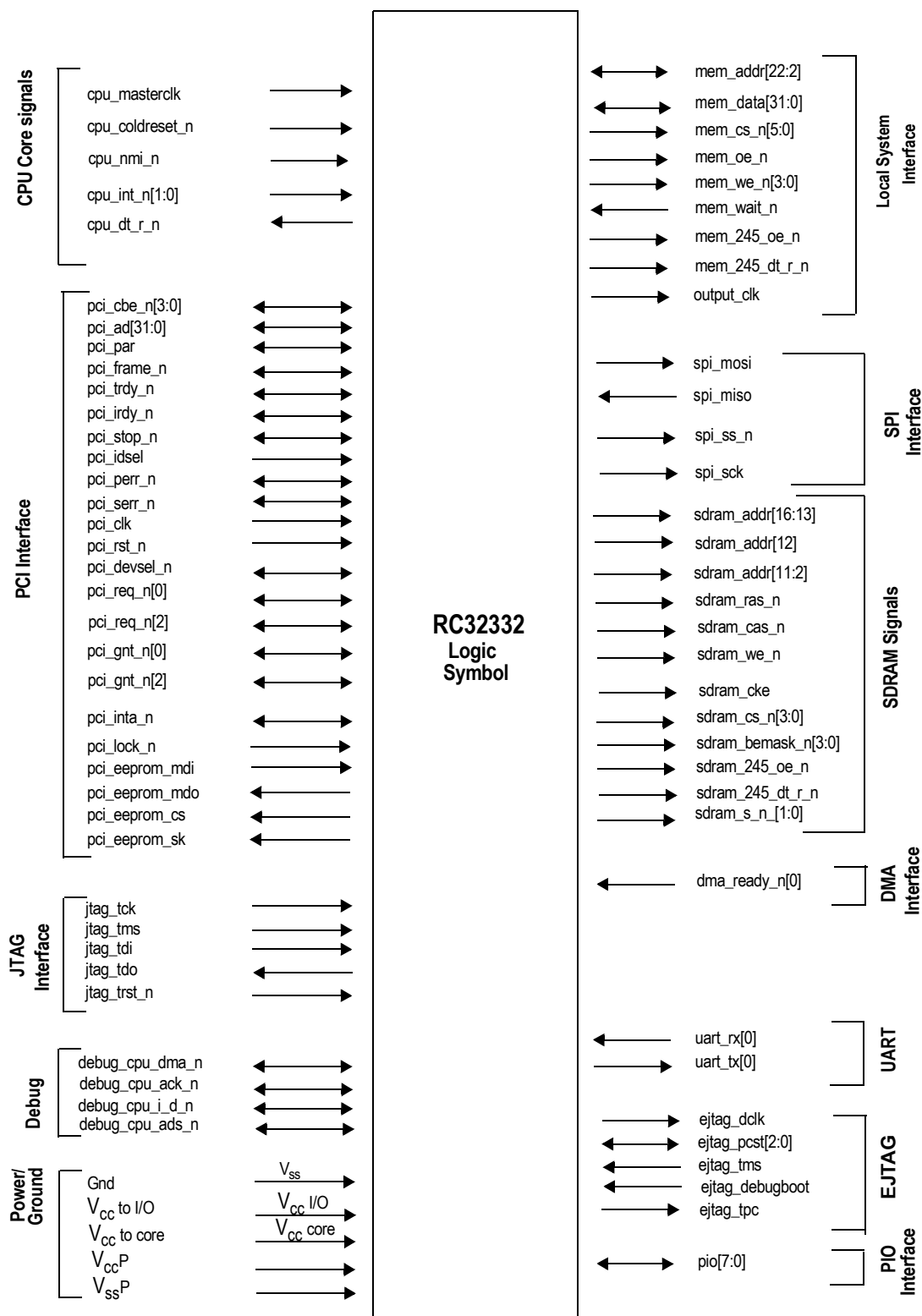
<sup>1</sup> Z in host mode; L in satellite non-boot mode; Z in satellite boot mode.  
<sup>2</sup> H in host mode, L in satellite non-boot and boot modes. X = unknown.

**SDRAM Control Interface**

|                 |        |   |      |                                                                                                                                                                                                          |
|-----------------|--------|---|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| sdram_addr_12   | Output | L | High | <b>SDRAM Address Bit 12 and Precharge All</b><br>SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command. |
| sdram_ras_n     | Output | H | High | <b>SDRAM RAS Negated</b><br>SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks.                                                                                                            |
| sdram_cas_n     | Output | H | High | <b>SDRAM CAS Negated</b><br>SDRAM mode: Provides SDRAM CAS control signal to all SDRAM banks.                                                                                                            |
| sdram_we_n      | Output | H | High | <b>SDRAM WE Negated</b><br>SDRAM mode: Provides SDRAM WE control signal to all SDRAM banks.                                                                                                              |
| sdram_cke       | Output | H | High | <b>SDRAM Clock Enable</b><br>SDRAM mode: Provides clock enable to all SDRAM banks.                                                                                                                       |
| sdram_cs_n[3:0] | Output | H | High | <b>SDRAM Chip Select Negated Bus</b> Recommend an external pull-up.<br>SDRAM mode: Provides chip select to each SDRAM bank.<br>SODIMM mode: Provides upper select byte enables [7:4].                    |
| sdram_s_n[1:0]  | Output | H | High | <b>SDRAM SODIMM Select Negated Bus</b><br>SDRAM mode: Not used.<br>SDRAM SODIMM mode: Upper and lower chip selects.                                                                                      |

Table 1 Pin Descriptions (Part 3 of 6)

# Logic Diagram — RC32332



## Mode Bit Settings to Configure Controller on Reset

The following table lists the mode bit settings to configure the controller on cold reset.

| Pin             | Mode Bit    | Description                                                                                       | Value | Mode Setting             |
|-----------------|-------------|---------------------------------------------------------------------------------------------------|-------|--------------------------|
| ejtag_pcst[2:0] | 2:0 MSB (2) | Clock Multiplier<br><b>MasterClock</b> is multiplied internally to generate PClock                | 0     | Multiply by 2            |
|                 |             |                                                                                                   | 1     | Multiply by 3            |
|                 |             |                                                                                                   | 2     | Multiply by 4            |
|                 |             |                                                                                                   | 3     | Reserved                 |
|                 |             |                                                                                                   | 4     | Reserved                 |
|                 |             |                                                                                                   | 5     | Reserved                 |
|                 |             |                                                                                                   | 6     | Reserved                 |
|                 |             |                                                                                                   | 7     | Reserved                 |
| debug_cpu_i_d_n | 3           | EndBit                                                                                            | 0     | Little-endian ordering   |
|                 |             |                                                                                                   | 1     | Big-endian ordering      |
| debug_cpu_ack_n | 4           | Reserved                                                                                          | 0     |                          |
| debug_cpu_ads_n | 5           | Reserved                                                                                          | 0     |                          |
| debug_cpu_dma_n | 6           | TmrIntEn<br>Enables/Disables the timer interrupt on Int*[5]                                       | 0     | Enables timer interrupt  |
|                 |             |                                                                                                   | 1     | Disables timer interrupt |
| mem_addr[17]    | 7           | Reserved for future use                                                                           | 1     |                          |
| mem_addr[19:18] | 9:8 MSB (9) | Boot-Prom Width specifies the memory port width of the memory space which contains the boot prom. | 00    | 8 bits                   |
|                 |             |                                                                                                   | 01    | 16 bits                  |
|                 |             |                                                                                                   | 10    | 32 bits                  |
|                 |             |                                                                                                   | 11    | Reserved                 |

Table 2 Boot-Mode Configuration Settings

### reset\_boot\_mode Settings

By using the non-boot mode cold reset initialization mode the user can change the internal register addresses from base 1800\_0000 to base 1900\_0000, as required. The RC32332 cold reset-boot mode initialization setting values and mode descriptions are listed below.

| Pin             | Reset Boot Mode | Description                                                                                                                                                    | Value | Mode Settings      |
|-----------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------------|
| mem_addr[22:21] | 1:0 MSB (1)     | Tri-state memory bus and EEPROM bus during coldreset_n assertion                                                                                               | 11    | Tri-state_bus_mode |
|                 |                 | Reserved                                                                                                                                                       | 10    |                    |
|                 |                 | <b>PCI-boot mode</b> (pci_host_mode must be in satellite mode) RC32332 will reset either from a cold reset or from a PCI reset. Boot code is provided via PCI. | 01    | PCI_boot_mode      |
|                 |                 | <b>Standard-boot mode</b> Boot from the RC32332's memory controller (typical system).                                                                          | 00    | standard_boot_mode |

Table 3 RC32332 reset\_boot\_mode Initialization Settings



## pci\_host\_mode Settings

During cold reset initialization, the RC32332's PCI interface can be set to the Satellite or Host mode settings. When set to the Host mode, the CPU must configure the RC32332's PCI configuration registers, including the read-only registers. If the RC32332's PCI is in the PCI-boot mode Satellite mode, read-only configuration registers are loaded by the serial EEPROM.

| Pin          | Reset Boot Mode | Description                          | Value | Mode Settings |
|--------------|-----------------|--------------------------------------|-------|---------------|
| mem_addr[20] | PCI host mode   | PCI is in satellite mode             | 1     | PCI_satellite |
|              |                 | PCI is in host mode (typical system) | 0     | PCI_host      |

Table 4 RC32332 pci\_host\_mode Initialization Settings

## Clock Parameters — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V<sub>cc</sub> Core = +3.3V±5%; V<sub>cc</sub> I/O = +3.3V±5%

2.5V version: V<sub>cc</sub> Core = +2.5V±5%; V<sub>cc</sub> I/O = +3.3V±5%

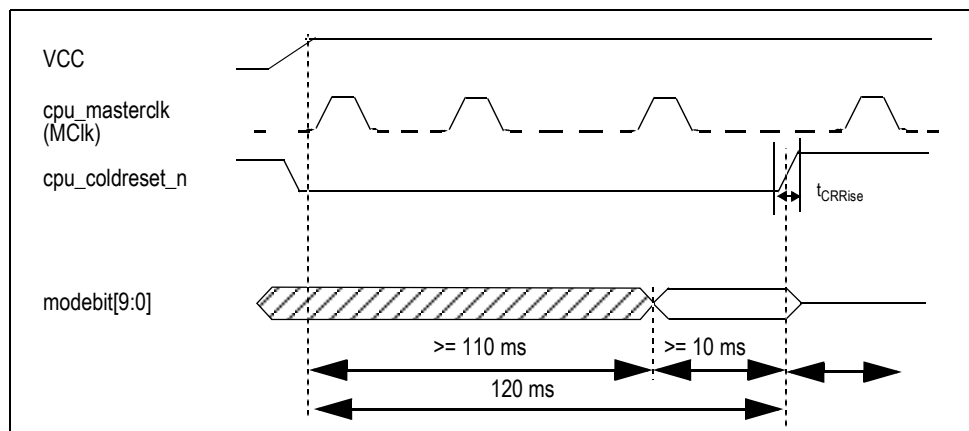
| Parameter                                       | Symbol                                                                              | Test Conditions   | RC32332<br>100MHz |       | RC32332<br>133MHz |       | RC32332<br>150MHz |       | Units |
|-------------------------------------------------|-------------------------------------------------------------------------------------|-------------------|-------------------|-------|-------------------|-------|-------------------|-------|-------|
|                                                 |                                                                                     |                   | Min               | Max   | Min               | Max   | Min               | Max   |       |
| cpu_masterclock HIGH                            | t <sub>MCHIGH</sub>                                                                 | Transition ≤ 2ns  | 8                 | —     | 6.75              | —     | 6                 | —     | ns    |
| cpu_masterclock LOW                             | t <sub>MCLOW</sub>                                                                  | Transition ≤ 2ns  | 8                 | —     | 6.75              | —     | 6                 | —     | ns    |
| cpu_masterclock period <sup>1</sup> - 3.3V ver. | t <sub>MCP</sub>                                                                    | —                 | 20                | 66.6  | 15                | 66.6  | 13.33             | 66.6  | ns    |
| cpu_masterclock period <sup>1</sup> - 2.5V ver. | t <sub>MCP</sub>                                                                    | —                 | 20                | 40.0  | 15                | 40.0  | 13.33             | 40.0  | ns    |
| cpu_masterclock Rise & Fall Time <sup>2</sup>   | t <sub>MCRise</sub> , t <sub>MCFall</sub>                                           | —                 | —                 | 3     | —                 | 3     | —                 | 3     | ns    |
| cpu_masterclock Jitter                          | t <sub>JITTER</sub>                                                                 | —                 | —                 | ± 250 | —                 | ± 250 | —                 | ± 200 | ps    |
| pci_clk Rise & Fall Time                        | t <sub>PCRise</sub> , t <sub>PCFall</sub>                                           | PCI 2.2           | —                 | 1.6   | —                 | 1.6   | —                 | 1.6   | ns    |
| pci_clk Period <sup>1</sup>                     | t <sub>PCP</sub>                                                                    | —                 | 20                | —     | 20                | —     | 20                | —     | ns    |
| jtag_tck Rise & Fall Time                       | t <sub>JCRise</sub> , t <sub>JCFall</sub>                                           | —                 | —                 | 5     | —                 | 5     | —                 | 5     | ns    |
| ejtag_dck period                                | t <sub>DCK</sub> , t <sub>t1</sub>                                                  | —                 | 10                | —     | 10                | —     | 10                | —     | ns    |
| jtag_tck clock period                           | t <sub>TCK</sub> , t <sub>t3</sub>                                                  | —                 | 100               | —     | 100               | —     | 100               | —     | ns    |
| ejtag_dclk High, Low Time                       | t <sub>DCK High</sub> , t <sub>t9</sub><br>t <sub>DCK Low</sub> , t <sub>t10</sub>  | —                 | 4                 | —     | 4                 | —     | 4                 | —     | ns    |
| ejtag_dclk Rise, Fall Time                      | t <sub>DCK Rise</sub> , t <sub>t9</sub><br>t <sub>DCK Fall</sub> , t <sub>t10</sub> | —                 | —                 | 1     | —                 | 1     | —                 | 1     | ns    |
| output_clk <sup>3</sup>                         | t <sub>DO21</sub>                                                                   | —                 | N/A               | N/A   | N/A               | N/A   | N/A               | N/A   | —     |
| cpu_coldreset_n<br>Asserted during power-up     | —                                                                                   | power-on sequence | 120               | —     | 120               | —     | 120               | —     | ms    |
| cpu_coldreset_n Rise Time                       | t <sub>CRRise</sub>                                                                 | —                 | —                 | 5     | —                 | 5     | —                 | 5     | ns    |

Table 5 Clock Parameters - RC32332

<sup>1</sup> cpu\_masterclock frequency should never be below pci\_clk frequency if PCI interface is used.

<sup>2</sup> Rise and Fall times are measured between 10% and 90%.

<sup>3</sup> Output\_clk should not be used in a system. Only the cpu\_masterclock or its derivative must be used to drive all the subsystems with designs based on the RC32334/RC32332. Refer to the RC32334/RC32332 Device Errata for more information.

**Reset Specification****Figure 3 Mode Configuration Interface Cold Reset Sequence**

**AC Timing Characteristics — RC32332**

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V<sub>cc</sub> Core = +3.3V±5%; V<sub>cc</sub> I/O = +3.3V±5%2.5V version: V<sub>cc</sub> Core = +2.5V±5%; V<sub>cc</sub> I/O = +3.3V±5%

| Signal                                                                                                                                                            | Symbol | Reference Edge       | 100MHz <sup>1</sup> |                 | 133MHz <sup>1</sup> |                 | 150MHz <sup>1</sup> |                  | Units | User Manual Timing Diagram Reference  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------|---------------------|-----------------|---------------------|-----------------|---------------------|------------------|-------|---------------------------------------|
|                                                                                                                                                                   |        |                      | Min                 | Max             | Min                 | Max             | Min                 | Max              |       |                                       |
| Local System Interface                                                                                                                                            |        |                      |                     |                 |                     |                 |                     |                  |       |                                       |
| mem_data[31:0] (data phase)                                                                                                                                       | Tsu2   | cpu_masterclk rising | 6                   | —               | 5                   | —               | 4.8                 | —                | ns    | Chapter 9, Figures 9.2 and 9.3        |
| mem_data[31:0] (data phase)                                                                                                                                       | Thld2  | cpu_masterclk rising | 1.5                 | —               | 1.5                 | —               | 1.5                 | —                | ns    |                                       |
| cpu_dt_r_n                                                                                                                                                        | Tdo3   | cpu_masterclk rising | —                   | 15              | —                   | 12              | —                   | 10               | ns    |                                       |
| mem_data[31:0]                                                                                                                                                    | Tdo4   | cpu_masterclk rising | —                   | 12              | —                   | 10              | —                   | 9.3              | ns    | Chapter 10, Figures 10.6 through 10.8 |
| mem_data[31:0] output hold time                                                                                                                                   | Tdoh1  | cpu_masterclk rising | 1                   | —               | 1                   | —               | 1                   | —                | ns    |                                       |
| mem_data[31:0] (tristate disable time)                                                                                                                            | Tdz    | cpu_masterclk rising | —                   | 12 <sup>2</sup> | —                   | 10 <sup>2</sup> | —                   | 9.3 <sup>2</sup> | ns    |                                       |
| mem_data[31:0] (tristate to data time)                                                                                                                            | Tzd    | cpu_masterclk rising | —                   | 12 <sup>2</sup> | —                   | 10 <sup>2</sup> | —                   | 9.3 <sup>2</sup> | ns    |                                       |
| mem_wait_n                                                                                                                                                        | Tsu6   | cpu_masterclk rising | 9                   | —               | 7                   | —               | 6                   | —                | ns    |                                       |
| mem_wait_n                                                                                                                                                        | Thld8  | cpu_masterclk rising | 1                   | —               | 1                   | —               | 1                   | —                | ns    |                                       |
| mem_addr[22:2]                                                                                                                                                    | Tdo5   | cpu_masterclk rising | —                   | 12              | —                   | 9               | —                   | 8                | ns    |                                       |
| mem_cs_n[5:0]                                                                                                                                                     | Tdo6   | cpu_masterclk rising | —                   | 12              | —                   | 9               | —                   | 8                | ns    |                                       |
| mem_oe_n, mem_245_oe_n                                                                                                                                            | Tdo7   | cpu_masterclk rising | —                   | 12              | —                   | 9               | —                   | 8                | ns    |                                       |
| mem_we_n[3:0]                                                                                                                                                     | Tdo7a  | cpu_masterclk rising | —                   | 15              | —                   | 12              | —                   | 10               | ns    |                                       |
| mem_245_dt_r_n                                                                                                                                                    | Tdo8   | cpu_masterclk rising | —                   | 15              | —                   | 12              | —                   | 10               | ns    |                                       |
| mem_addr[25:2]<br>mem_cs_n[5:0]<br>mem_oe_n, mem_we_n[3:0],<br>mem_245_dt_r_n,<br>mem_245_oe_n                                                                    | Tdoh3  | cpu_masterclk rising | 1.5                 | —               | 1.5                 | —               | 1.5                 | —                | ns    |                                       |
| PCI for 3.3V Device <sup>3</sup>                                                                                                                                  |        |                      |                     |                 |                     |                 |                     |                  |       |                                       |
| pci_ad[31:0], pci_cbe_n[3:0],<br>pci_par, pci_frame_n, pci_trdy_n,<br>pci_irdy_n, pci_stop_n, pci_perr_n,<br>pci_serr_n, pci_devsel_n,<br>pci_lock_n              | Tsu    | pci_clk rising       | 3                   | —               | 3                   | —               | 3                   | —                | ns    |                                       |
| pci_idsel, pci_req_n[2],<br>pci_req_n[1], pci_req_n[0],<br>pci_gnt_n[0], pci_inta_n                                                                               | Tsu    | pci_clk rising       | 5                   | —               | 5                   | —               | 5                   | —                | ns    |                                       |
| pci_gnt_n[0]                                                                                                                                                      | Tsu    | pci_clk rising       | 5                   | —               | 5                   | —               | 5                   | —                | ns    |                                       |
| pci_ad[31:0], pci_cbe_n[3:0],<br>pci_par, pci_frame_n, pci_trdy_n,<br>pci_irdy_n, pci_stop_n, pci_perr_n,<br>pci_serr_n, pci_devsel_n,<br>pci_lock_n <sup>4</sup> | Thld   | pci_clk rising       | 0                   | —               | 0                   | —               | 0                   | —                | ns    |                                       |

Table 6 AC Timing Characteristics - RC32332 (Part 1 of 4)

| Signal | Symbol | Reference Edge | 100MHz <sup>1</sup> |     | 133MHz <sup>1</sup> |     | 150MHz <sup>1</sup> |     | Units | User Manual Timing Diagram Reference |
|--------|--------|----------------|---------------------|-----|---------------------|-----|---------------------|-----|-------|--------------------------------------|
|        |        |                | Min                 | Max | Min                 | Max | Min                 | Max |       |                                      |

**Reset**

|                 |        |                        |    |   |    |   |    |   |    |                                   |
|-----------------|--------|------------------------|----|---|----|---|----|---|----|-----------------------------------|
| mem_addr[19:17] | Tsu10  | cpu_coldreset_n rising | 10 | — | 10 | — | 10 | — | ms | Chapter 19, Figures 19.8 and 19.9 |
| mem_addr[19:17] | Thld10 | cpu_coldreset_n rising | 1  | — | 1  | — | 1  | — | ns |                                   |
| mem_addr[22:20] | Tsu22  | cpu_masterclk rising   | 9  | — | 7  | — | 6  | — | ns |                                   |
| mem_addr[22:20] | Thld22 | cpu_masterclk rising   | 1  | — | 1  | — | 1  | — | ns |                                   |

**Debug Interface**

|                                                                                              |        |                        |    |    |    |    |    |    |    |                                                   |
|----------------------------------------------------------------------------------------------|--------|------------------------|----|----|----|----|----|----|----|---------------------------------------------------|
| debug_cpu_dma_n,<br>debug_cpu_ack_n,<br>debug_cpu_ads_n,<br>debug_cpu_i_d_n, ejtag_pcst[2:0] | Tsu20  | cpu_coldreset_n rising | 10 | —  | 10 | —  | 10 | —  | ms | Chapter 19, Figure 19.9 and Chapter 9, Figure 9.2 |
| debug_cpu_dma_n,<br>debug_cpu_ack_n,<br>debug_cpu_ads_n,<br>debug_cpu_i_d_n, ejtag_pcst[2:0] | Thld20 | cpu_coldreset_n rising | 1  | —  | 1  | —  | 1  | —  | ns |                                                   |
| debug_cpu_dma_n,<br>debug_cpu_ack_n,<br>debug_cpu_ads_n,<br>debug_cpu_i_d_n                  | Tdo20  | cpu_masterclk rising   | —  | 15 | —  | 12 | —  | 10 | ns |                                                   |
| debug_cpu_dma_n,<br>debug_cpu_ack_n,<br>debug_cpu_ads_n,<br>debug_cpu_i_d_n                  | Tdoh20 | cpu_masterclk rising   | 1  | —  | 1  | —  | 1  | —  | ns |                                                   |

**JTAG Interface**

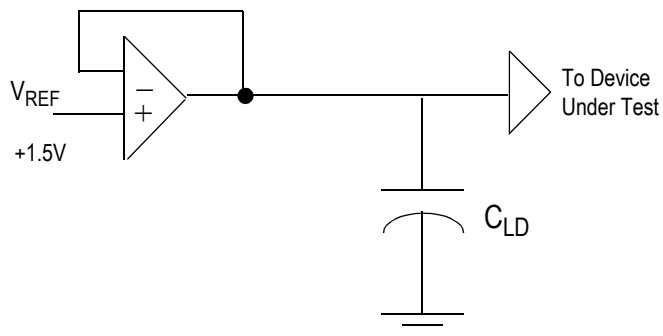
|                                 |                |                  |    |    |    |    |    |    |    |                     |
|---------------------------------|----------------|------------------|----|----|----|----|----|----|----|---------------------|
| jtag_tms, jtag_tdi, jtag_trst_n | t <sub>5</sub> | jtag_tck rising  | 10 | —  | 10 | —  | 10 | —  | ns | See Figure 4 below. |
| jtag_tms, jtag_tdi, jtag_trst_n | t <sub>6</sub> | jtag_tck rising  | 10 | —  | 10 | —  | 10 | —  | ns |                     |
| jtag_tdo                        | t <sub>4</sub> | jtag_tck falling | —  | 10 | —  | 10 | —  | 10 | ns |                     |

**EJTAG Interface**

|                              |                                        |                   |     |   |     |   |     |   |    |                     |
|------------------------------|----------------------------------------|-------------------|-----|---|-----|---|-----|---|----|---------------------|
| ejtag_tms, ejtag_debugboot   | t <sub>5</sub>                         | jtag_tclk rising  | 4   | — | 4   | — | 4   | — | ns | See Figure 4 below. |
| ejtag_tms, ejtag_debugboot   | t <sub>6</sub>                         | jtag_clk rising   | 2   | — | 2   | — | 2   | — | ns |                     |
| jtag_tdo Output Delay Time   | t <sub>TDOD0</sub> , t <sub>4</sub>    | jtag_tck falling  | —   | 6 | —   | 6 | —   | 6 | ns |                     |
| jtag_tdi Input Setup Time    | t <sub>DIS</sub> , t <sub>5</sub>      | jtag_tck rising   | 4   | — | 4   | — | 4   | — | ns |                     |
| jtag_tdi Input Hold Time     | t <sub>DIH</sub> , t <sub>6</sub>      | jtag_tck rising   | 2   | — | 2   | — | 2   | — | ns |                     |
| jtag_trst_n Low Time         | t <sub>TRSTLow</sub> , t <sub>12</sub> | —                 | 100 | — | 100 | — | 100 | — | ns |                     |
| jtag_trst_n Removal Time     | t <sub>TRSTR</sub> , t <sub>13</sub>   | jtag_tck rising   | 3   | — | 3   | — | 3   | — | ns |                     |
| ejtag_tpc Output Delay Time  | t <sub>PCDO</sub> , t <sub>8</sub>     | ejtag_dclk rising | -1  | 3 | -1  | 3 | -1  | 3 | ns |                     |
| ejtag_pcst Output Delay Time | t <sub>PCSTDO</sub> , t <sub>7</sub>   | ejtag_dclk rising | -1  | 3 | -1  | 3 | -1  | 3 | ns |                     |

**Table 6 AC Timing Characteristics - RC32332 (Part 4 of 4)**<sup>1</sup>. At all pipeline frequencies.<sup>2</sup>. Guaranteed by design.<sup>3</sup>. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2 at 33MHz.<sup>4</sup>. pci\_rst\_n is tested per PCI 2.2 as an asynchronous signal.

## Output Loading for AC Testing



| Signal                 | C <sub>ld</sub> |
|------------------------|-----------------|
| All High Drive Signals | 50 pF           |
| All Low Drive Signals  | 25 pF           |

Figure 5 Output Loading for AC Testing

**Note:** PCI pins have been correlated to PCI 2.2.

## Recommended Operation Temperature and Supply Voltage

### 3.3V Device

| Grade      | Ambient Temperature    | Gnd | V <sub>ccIO</sub> | V <sub>ccCore</sub> | V <sub>ccP</sub> |
|------------|------------------------|-----|-------------------|---------------------|------------------|
| Commercial | 0°C to +70°C Ambient   | 0V  | 3.3V±5%           | 3.3V±5%             | 3.3V±5%          |
| Industrial | -40°C to +85°C Ambient | 0V  | 3.3V±5%           | 3.3V±5%             | 3.3V±5%          |

Table 7 Temperature and Voltage — 3.3V Device

### 2.5V Device

| Grade      | Ambient Temperature    | Gnd | V <sub>ccIO</sub> | V <sub>ccCore</sub> | V <sub>ccP</sub> |
|------------|------------------------|-----|-------------------|---------------------|------------------|
| Commercial | 0°C to +70°C Ambient   | 0V  | 3.3V±5%           | 2.5V±5%             | 2.5V±5%          |
| Industrial | -40°C to +85°C Ambient | 0V  | 3.3V±5%           | 2.5V±5%             | 2.5V±5%          |

Table 8 Temperature and Voltage — 2.5V Device

## DC Electrical Characteristics — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version:  $V_{CC}$  Core = +3.3V±5%;  $V_{CC}$  I/O = +3.3V±5%

2.5V version:  $V_{CC}$  Core = +2.5V±5%;  $V_{CC}$  I/O = +3.3V±5%

|                        | Parameter    | RC32332 <sup>1</sup> |         | Pin Numbers                                                                                                                                          | Conditions           |
|------------------------|--------------|----------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
|                        |              | Minimum              | Maximum |                                                                                                                                                      |                      |
| Input Pads             | $V_{IL}$     | —                    | 0.8V    | 52, 64, 95, 160, 161, 164, 166-169, 176, 191                                                                                                         | —                    |
|                        | $V_{IH}$     | 2.0V                 | —       |                                                                                                                                                      | —                    |
| LOW Drive Output Pads  | $V_{OL}$     | —                    | 0.4V    | 41-45, 48, 170, 171, 174, 175, 177-180, 185-190, 195-200, 207, 208                                                                                   | $ I_{OUT}  = 6mA$    |
|                        | $V_{OH}$     | $V_{CC} - 0.4V$      | —       |                                                                                                                                                      | $ I_{OUT}  = 8mA$    |
|                        | $V_{IL}$     | —                    | 0.8V    |                                                                                                                                                      | —                    |
|                        | $V_{IH}$     | 2.0V                 | —       |                                                                                                                                                      | —                    |
| HIGH Drive Output Pads | $V_{OL}$     | —                    | 0.4V    | 1- 5, 8, 13-15, 18-25, 28-35, 38-40, 49-51, 53- 57, 60, 61, 63, 65-67, 70-76, 79, 80, 83-87, 90-94, 153, 154, 156, 158, 165, 194, 201, 204, 205, 206 | $ I_{OUT}  = 7mA$    |
|                        | $V_{OH}$     | $V_{CC} - 0.4V$      | —       |                                                                                                                                                      | $ I_{OUT}  = 16mA$   |
|                        | $V_{IL}$     | —                    | 0.8V    |                                                                                                                                                      | —                    |
|                        | $V_{IH}$     | 2.0V                 | —       |                                                                                                                                                      | —                    |
| PCI Drive Input Pads   | $V_{IL}$     | —                    | —       | 123, 155, 157, 159                                                                                                                                   | Per PCI 2.2          |
|                        | $V_{IH}$     | —                    | —       |                                                                                                                                                      |                      |
| PCI Drive Output Pads  | $V_{OL}$     | —                    | —       | 96, 97, 100-109, 112-119, 122, 124-129, 132-139, 142-149, 152                                                                                        | Per PCI 2.2          |
|                        | $V_{OH}$     | —                    | —       |                                                                                                                                                      |                      |
|                        | $V_{IL}$     | —                    | —       |                                                                                                                                                      |                      |
|                        | $V_{IH}$     | —                    | —       |                                                                                                                                                      |                      |
| All Pads               | $C_{IN}$     | —                    | 10pF    | All input pads except 155 and 156                                                                                                                    | —                    |
|                        | $C_{IN}^2$   | 5pf                  | 12pF    | 155                                                                                                                                                  | Per PCI 2.2          |
|                        | $C_{IN}^3$   | —                    | 8pF     | 156                                                                                                                                                  | Per PCI 2.2          |
|                        | $C_{OUT}$    | —                    | 10pF    | All output pads                                                                                                                                      | —                    |
|                        | $I/O_{LEAK}$ | —                    | 10μA    | All non-internal pull-up pins                                                                                                                        | Input/Output Leakage |
|                        | $I/O_{LEAK}$ | —                    | 50μA    | All internal pull-up pins                                                                                                                            | Input/Output Leakage |

Table 9 DC Electrical Characteristics - RC32332

<sup>1</sup>. At all pipeline frequencies.

<sup>2</sup>. Applies only to pad 155.

<sup>3</sup>. Applies only to pad 156.

## Capacitive Load Deration — RC32332

Refer to the IDT document [79RC32332 IBIS Model](#) located on the company's web site.

## Power Consumption

### 3.3V Device

**Note:** This table is based on a 2:1 pipeline-to-bus clock ratio.

| Parameter         |                           | 100MHz  |      | 133MHz  |      | 150MHz  |      | Unit | Conditions                                                                                                                                                                                                                                                                                        |
|-------------------|---------------------------|---------|------|---------|------|---------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                   |                           | Typical | Max. | Typical | Max. | Typical | Max. |      |                                                                                                                                                                                                                                                                                                   |
| I <sub>CC</sub>   | Normal mode               | 360     | 480  | 480     | 630  | 550     | 700  | mA   | C <sub>L</sub> = (See Figure 5, Output Loading for AC Testing)<br>T <sub>a</sub> = 25°C<br>V <sub>CC</sub> Core = 3.46V (for max. values)<br>V <sub>CC</sub> I/O = 3.46V (for max. values)<br>V <sub>CC</sub> Core = 3.3V (for typical values)<br>V <sub>CC</sub> I/O = 3.3V (for typical values) |
|                   | Standby mode <sup>1</sup> | 250     | 370  | 330     | 480  | 390     | 540  | mA   |                                                                                                                                                                                                                                                                                                   |
| Power Dissipation | Normal mode               | 1.2     | 1.7  | 1.5     | 2.2  | 1.7     | 2.4  | W    |                                                                                                                                                                                                                                                                                                   |
|                   | Standby mode <sup>1</sup> | 0.83    | 1.3  | 1.1     | 1.7  | 1.3     | 1.9  | W    |                                                                                                                                                                                                                                                                                                   |

**Table 10 Power Consumption — 3.3V Device**

<sup>1</sup> RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

### 2.5V Device

**Note:** This table is based on a 2:1 pipeline-to-bus clock ratio.

| Parameter            |                           | 100MHz  |      | 133MHz  |      | 150MHz  |      | Unit | Conditions                                                                                                                                                                                                                                                                                         |
|----------------------|---------------------------|---------|------|---------|------|---------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                      |                           | Typical | Max. | Typical | Max. | Typical | Max. |      |                                                                                                                                                                                                                                                                                                    |
| I <sub>CC</sub> I/O  | Normal mode               | 24      | 81   | 32      | 93   | 35      | 104  | mA   | C <sub>L</sub> = (See Figure 5, Output Loading for AC Testing)<br>T <sub>a</sub> = 25°C<br>V <sub>CC</sub> Core = 2.625V (for max. values)<br>V <sub>CC</sub> I/O = 3.46V (for max. values)<br>V <sub>CC</sub> Core = 2.5V (for typical values)<br>V <sub>CC</sub> I/O = 3.3V (for typical values) |
|                      | Standby mode <sup>1</sup> | 2       | 81   | 2       | 93   | 2       | 104  | mA   |                                                                                                                                                                                                                                                                                                    |
| I <sub>CC</sub> core | Normal mode               | 232     | 301  | 298     | 392  | 333     | 438  | mA   |                                                                                                                                                                                                                                                                                                    |
|                      | Standby mode <sup>1</sup> | 120     | 269  | 151     | 319  | 168     | 345  | mA   |                                                                                                                                                                                                                                                                                                    |
| Power Dissipation    | Normal mode               | 0.66    | 1.07 | 0.85    | 1.35 | 0.95    | 1.51 | W    |                                                                                                                                                                                                                                                                                                    |
|                      | Standby mode <sup>1</sup> | 0.31    | 0.94 | 0.38    | 1.10 | 0.43    | 1.21 | W    |                                                                                                                                                                                                                                                                                                    |

**Table 11 Power Consumption — 2.5V Device**

<sup>1</sup> RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

## Power Ramp-up

### 3.3V Device

There is no special requirement for how fast V<sub>CC</sub> I/O ramps up to 3.3V. However, all timing references are based on a stable V<sub>CC</sub> I/O.

### 2.5V Device

The 2.5V core supply (and 2.5V V<sub>CC</sub>P supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast V<sub>CC</sub> I/O ramps up to 3.3V. However, all timing references are based on a stable V<sub>CC</sub> I/O.

## Power Curves

The following four graphs contain the simulated power curves that show power consumption at various bus frequencies. Figures 6 and 7 apply to the 3.3V device, while Figures 8 and 9 apply to the 2.5V device.

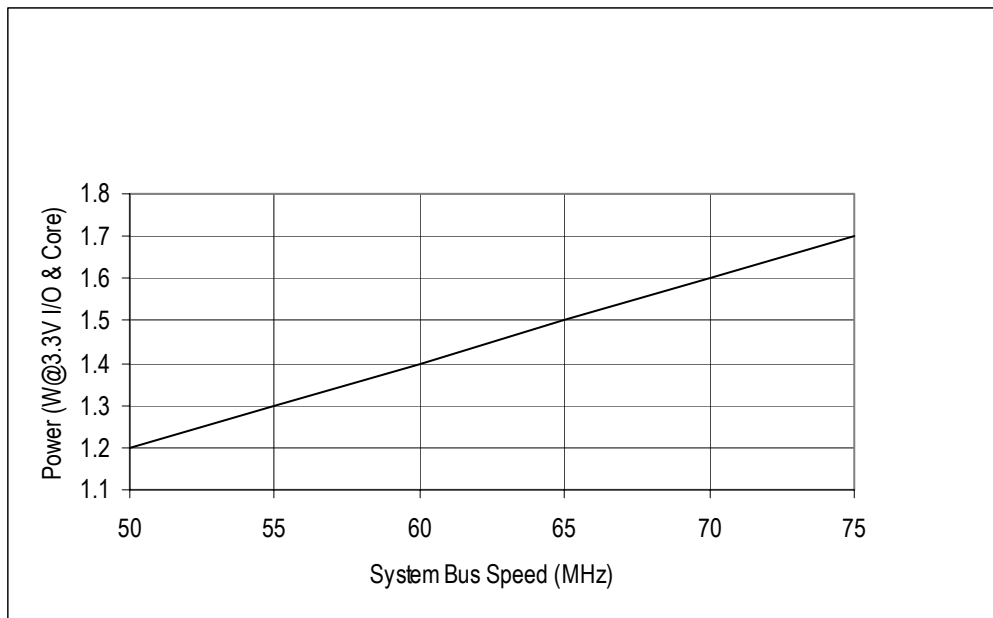


Figure 6 Typical Power Usage — RC32V332 Device

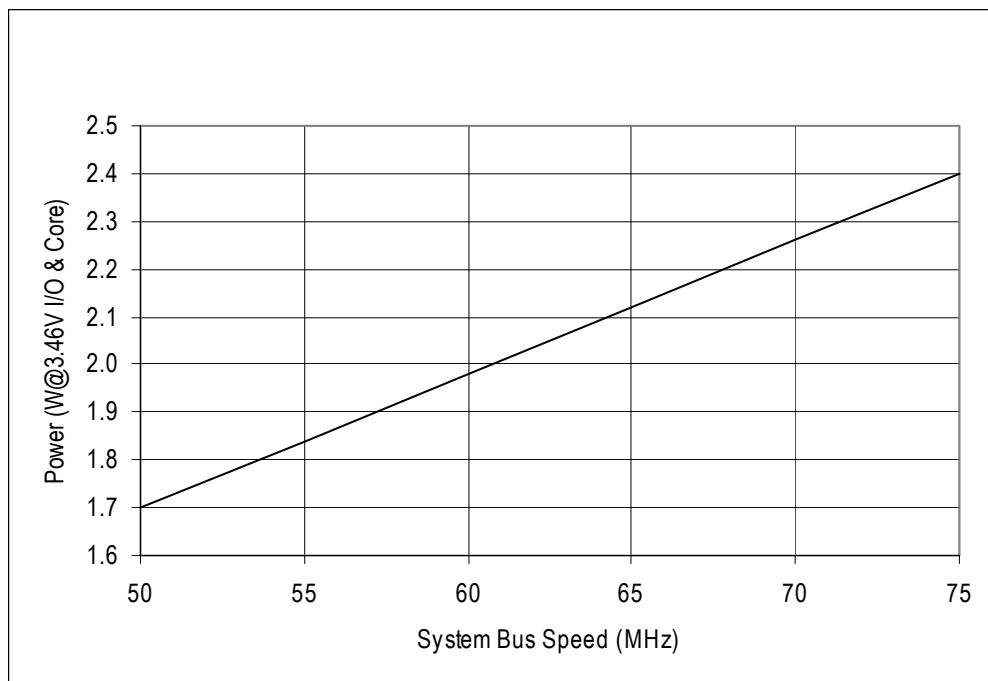


Figure 7 Maximum Power Usage — RC32V332 Device



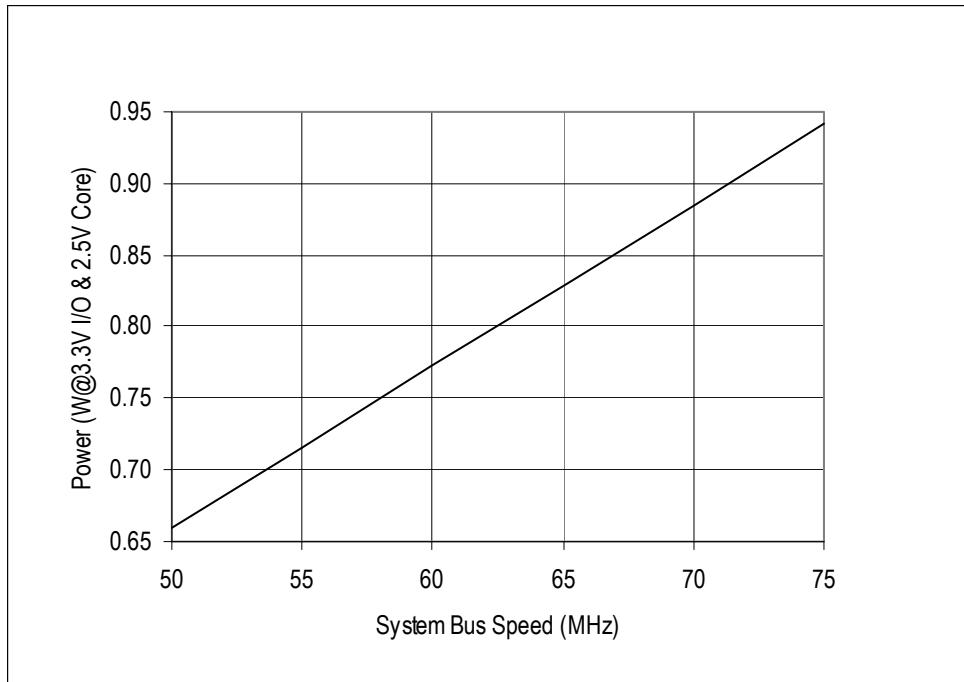


Figure 8 Typical Power Usage — RC32T332 Device

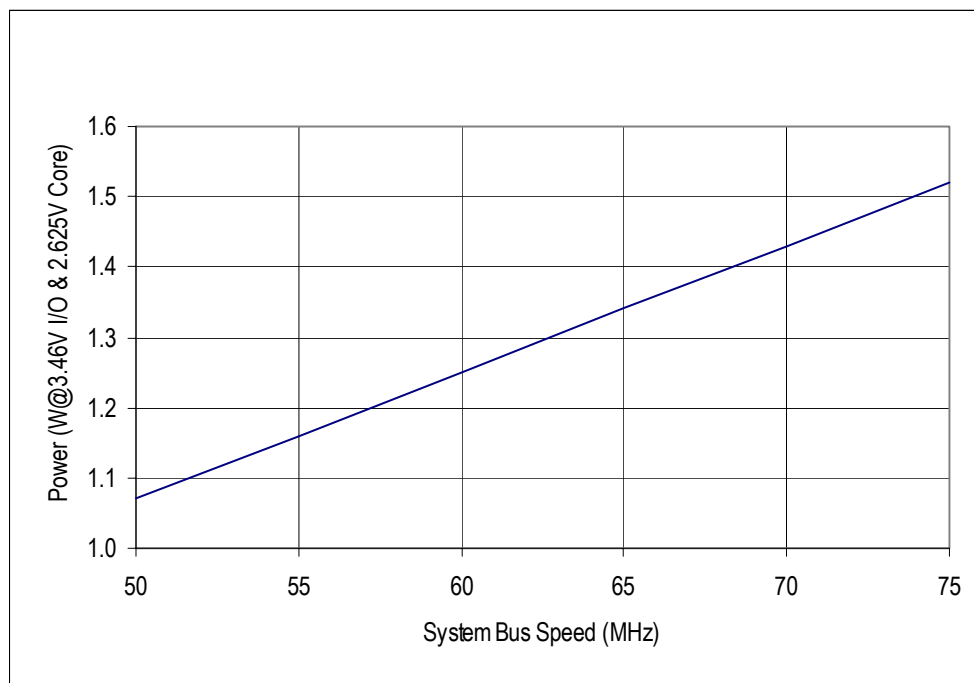


Figure 9 Maximum Power Usage — RC32T332 Device

## Absolute Maximum Ratings

| Symbol                              | Parameter                               | Min <sup>1</sup> | Max <sup>1</sup>       | Unit      |
|-------------------------------------|-----------------------------------------|------------------|------------------------|-----------|
| V <sub>cc</sub> Core<br>3.3V Device | Supply Voltage                          | -0.3             | 4.0                    | V         |
| V <sub>cc</sub> Core<br>2.5V Device | Supply Voltage                          | -0.3             | 3.0                    | V         |
| V <sub>cc</sub> I/O                 | I/O Supply Voltage                      | -0.3             | 4.0                    | V         |
| V <sub>i</sub> 3.3V Device          | Input Voltage                           | -0.3             | 5.5                    | V         |
| V <sub>i</sub> 2.5V Device          | Input Voltage                           | -0.3             | V <sub>cc</sub> /O+0.3 | V         |
| V <sub>imin</sub>                   | Input Voltage - undershoot <sup>2</sup> | -0.6             | —                      | V         |
| T <sub>stg</sub>                    | Storage Temperature                     | -40              | 125                    | degrees C |

**Table 12 Absolute Maximum Ratings**

<sup>1</sup> Functional and tested operating conditions are given in Table 7. Absolute maximum ratings are stress ratings only, and functional operation is not guaranteed beyond recommended operating voltages and temperatures. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

<sup>2</sup> All PCI pads are fully compatible with PCI Specification version 2.2.

## Package Pin-out — 208-PQFP for RC32332

The following table lists the pin numbers and signal names for the RC32332. Signal names ending with an \_n are active when low.

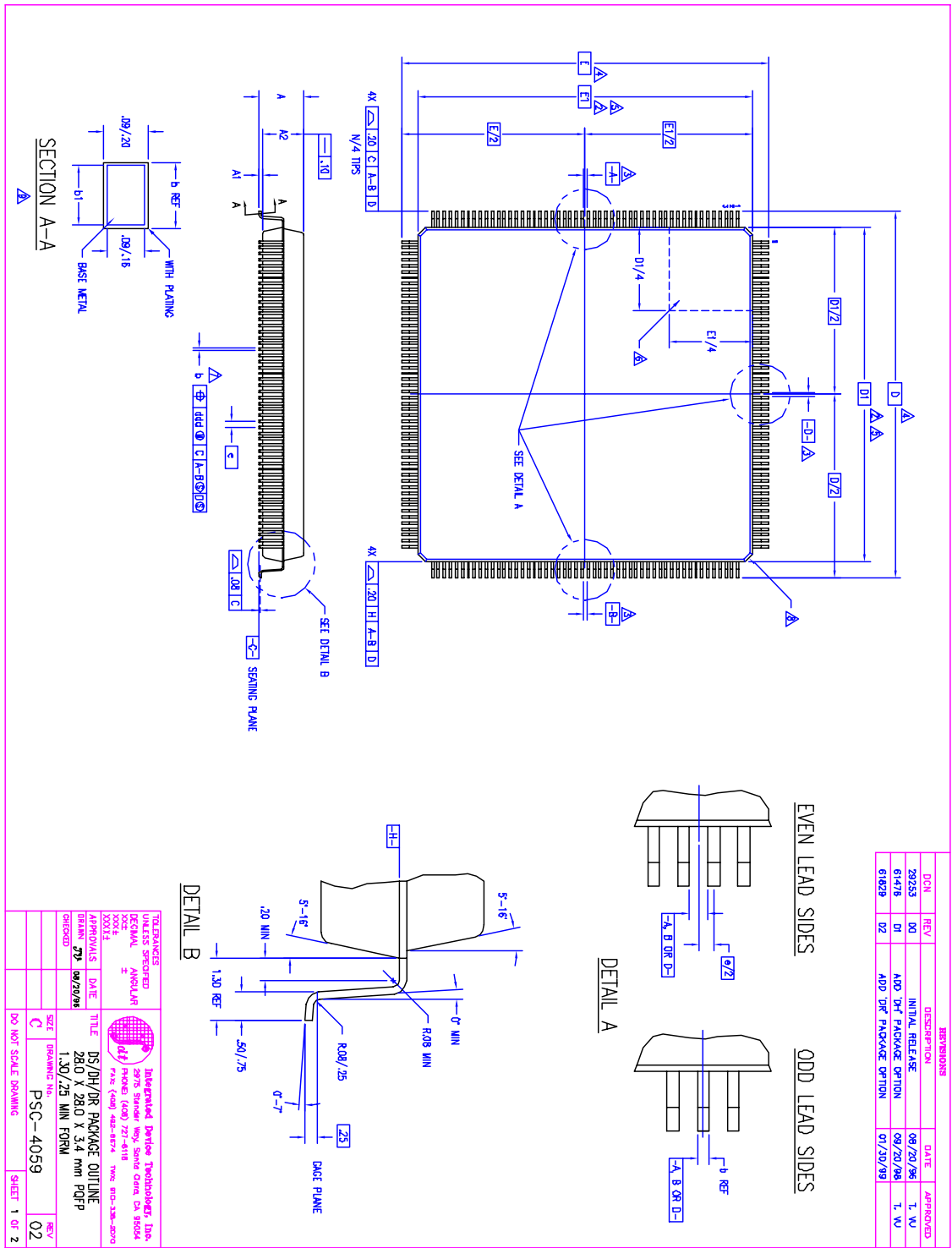
| Pin | Function            | Alt | Pin | Function             | Alt | Pin | Function            | Alt | Pin | Function            | Alt |
|-----|---------------------|-----|-----|----------------------|-----|-----|---------------------|-----|-----|---------------------|-----|
| 1   | sdram_245_oe_n      |     | 53  | mem_data[12]         |     | 105 | pci_ad[7]           |     | 157 | pci_req_n[2]        | 1   |
| 2   | sdram_we_n          |     | 54  | mem_data[19]         |     | 106 | pci_cbe_n[0]        |     | 158 | pci_gnt_n[2]        | 1   |
| 3   | sdram_cas_n         |     | 55  | mem_data[13]         |     | 107 | pci_ad[8]           |     | 159 | pci_rst_n           |     |
| 4   | sdram_bemask_n[0]   |     | 56  | mem_data[18]         |     | 108 | pci_ad[9]           |     | 160 | cpu_int_n[0]        |     |
| 5   | sdram_bemask_n[1]   |     | 57  | mem_data[14]         |     | 109 | pci_ad[10]          |     | 161 | cpu_int_n[1]        |     |
| 6   | V <sub>ss</sub>     |     | 58  | V <sub>ss</sub>      |     | 110 | V <sub>ss</sub>     |     | 162 | V <sub>ss</sub>     |     |
| 7   | V <sub>cc</sub> I/O |     | 59  | V <sub>cc</sub> I/O  |     | 111 | V <sub>cc</sub> I/O |     | 163 | V <sub>cc</sub> I/O |     |
| 8   | sdram_cs_n[0]       |     | 60  | mem_data[17]         |     | 112 | pci_ad[11]          |     | 164 | jtag_tdi            |     |
| 9   | sdram_cs_n[1]       |     | 61  | mem_data[16]         |     | 113 | pci_ad[12]          |     | 165 | jtag_tdo            |     |
| 10  | sdram_ras_n         |     | 62  | V <sub>cc</sub> core |     | 114 | pci_ad[13]          |     | 166 | jtag_tms            |     |
| 11  | sdram_s_n[0]        |     | 63  | mem_data[15]         |     | 115 | pci_ad[14]          |     | 167 | ejtag_tms           |     |
| 12  | sdram_s_n[1]        |     | 64  | cpu_masterclk        |     | 116 | pci_ad[15]          |     | 168 | jtag_tck            |     |
| 13  | mem_addr[2]         | 1   | 65  | mem_data[31]         |     | 117 | pci_cbe_n[1]        |     | 169 | jtag_trst_n         |     |
| 14  | mem_addr[3]         | 1   | 66  | mem_data[0]          |     | 118 | pci_par             |     | 170 | ejtag_pcst[0]       | 1   |
| 15  | mem_addr[4]         | 1   | 67  | mem_data[30]         |     | 119 | pci_serr_n          |     | 171 | ejtag_pcst[1]       | 1   |
| 16  | V <sub>ss</sub>     |     | 68  | V <sub>ss</sub>      |     | 120 | V <sub>ss</sub>     |     | 172 | V <sub>ss</sub>     |     |
| 17  | V <sub>cc</sub> I/O |     | 69  | V <sub>cc</sub> I/O  |     | 121 | V <sub>cc</sub> I/O |     | 173 | V <sub>cc</sub> I/O |     |
| 18  | mem_addr[5]         | 1   | 70  | mem_data[1]          |     | 122 | pci_perr_n          |     | 174 | ejtag_pcst[2]       | 1   |
| 19  | mem_addr[6]         | 1   | 71  | mem_data[29]         |     | 123 | pci_lock_n          |     | 175 | ejtag_dclk          |     |

**Table 13 RC32332 208-pin QFP Package Pin-Out (Part 1 of 2)**

| Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| 20  | mem_addr[7]          | 1   | 72  | mem_data[2]          |     | 124 | pci_stop_n           |     | 176 | ejtag_debugboot      |     |
| 21  | mem_addr[8]          | 1   | 73  | mem_data[28]         |     | 125 | pci_devsel_n         |     | 177 | debug_cpu_i_d_n      | 1   |
| 22  | mem_addr[9]          | 1   | 74  | mem_data[3]          |     | 126 | pci_trdy_n           |     | 178 | debug_cpu_ads_n      | 1   |
| 23  | mem_addr[10]         | 1   | 75  | mem_data[27]         |     | 127 | pci_irdy_n           |     | 179 | debug_cpu_ack_n      | 1   |
| 24  | mem_addr[11]         | 1   | 76  | mem_data[4]          |     | 128 | pci_frame_n          |     | 180 | debug_cpu_dma_n      | 1   |
| 25  | output_clk           |     | 77  | V <sub>cc</sub> P    |     | 129 | pci_cbe_n[2]         |     | 181 | V <sub>cc</sub> I/O  |     |
| 26  | V <sub>ss</sub>      |     | 78  | V <sub>ss</sub> P    |     | 130 | V <sub>ss</sub>      |     | 182 | V <sub>ss</sub>      |     |
| 27  | V <sub>cc</sub> core |     | 79  | mem_data[26]         |     | 131 | V <sub>cc</sub> core |     | 183 | V <sub>cc</sub> core |     |
| 28  | mem_addr_12          |     | 80  | mem_data[5]          |     | 132 | pci_ad[16]           |     | 184 | V <sub>cc</sub> I/O  |     |
| 29  | sdram_addr_12        |     | 81  | V <sub>ss</sub>      |     | 133 | pci_ad[17]           |     | 185 | spi_ss_n             | 1   |
| 30  | sdram_cke            |     | 82  | V <sub>cc</sub> core |     | 134 | pci_ad[18]           |     | 186 | spi_sck              | 2   |
| 31  | sdram_cs_n[2]        |     | 83  | cpu_dt_r_n           | 2   | 135 | pci_ad[19]           |     | 187 | spi_miso             | 2   |
| 32  | sdram_cs_n[3]        |     | 84  | mem_data[25]         |     | 136 | pci_ad[20]           |     | 188 | spi_mosi             | 2   |
| 33  | sdram_bemask_n[2]    |     | 85  | mem_data[6]          |     | 137 | pci_ad[21]           |     | 189 | dma_ready_n[0]       | 2   |
| 34  | sdram_bemask_n[3]    |     | 86  | mem_data[24]         |     | 138 | pci_ad[22]           |     | 190 | mem_245_oe_n         |     |
| 35  | mem_addr[13]         |     | 87  | mem_data[7]          |     | 139 | pci_ad[23]           |     | 191 | mem_wait_n           | 2   |
| 36  | V <sub>ss</sub>      |     | 88  | V <sub>ss</sub>      |     | 140 | V <sub>ss</sub>      |     | 192 | V <sub>ss</sub>      |     |
| 37  | V <sub>cc</sub> I/O  |     | 89  | V <sub>cc</sub> I/O  |     | 141 | V <sub>cc</sub> I/O  |     | 193 | V <sub>cc</sub> I/O  |     |
| 38  | mem_addr[14]         |     | 90  | mem_data[23]         |     | 142 | pci_cbe_n[3]         |     | 194 | mem_oe_n             |     |
| 39  | mem_addr[15]         | 1   | 91  | mem_data[8]          |     | 143 | pci_ad[24]           |     | 195 | mem_cs_n[0]          |     |
| 40  | mem_addr[16]         | 1   | 92  | mem_data[22]         |     | 144 | pci_ad[25]           |     | 196 | mem_cs_n[1]          |     |
| 41  | mem_addr[17]         | 1   | 93  | mem_data[9]          |     | 145 | pci_ad[26]           |     | 197 | mem_cs_n[2]          |     |
| 42  | mem_addr[18]         | 1   | 94  | mem_data[21]         |     | 146 | pci_ad[27]           |     | 198 | mem_cs_n[3]          |     |
| 43  | mem_addr[19]         | 1   | 95  | cpu_nmi_n            |     | 147 | pci_ad[28]           |     | 199 | mem_cs_n[4]          |     |
| 44  | mem_addr[20]         | 1   | 96  | pci_ad[0]            |     | 148 | pci_ad[29]           |     | 200 | mem_cs_n[5]          |     |
| 45  | mem_addr[21]         | 1   | 97  | pci_ad[1]            |     | 149 | pci_ad[30]           |     | 201 | mem_we_n[0]          |     |
| 46  | V <sub>ss</sub>      |     | 98  | V <sub>ss</sub>      |     | 150 | V <sub>ss</sub>      |     | 202 | V <sub>ss</sub>      |     |
| 47  | V <sub>cc</sub> I/O  |     | 99  | V <sub>cc</sub> I/O  |     | 151 | V <sub>cc</sub> I/O  |     | 203 | V <sub>cc</sub> I/O  |     |
| 48  | mem_addr[22]         | 1   | 100 | pci_ad[2]            |     | 152 | pci_ad[31]           |     | 204 | mem_we_n[1]          |     |
| 49  | mem_data[10]         |     | 101 | pci_ad[3]            |     | 153 | pci_req_n[0]         |     | 205 | mem_we_n[2]          |     |
| 50  | mem_data[11]         |     | 102 | pci_ad[4]            |     | 154 | pci_gnt_n[0]         |     | 206 | mem_we_n[3]          |     |
| 51  | mem_data[20]         |     | 103 | pci_ad[5]            |     | 155 | pci_clk              |     | 207 | uart_tx[0]           | 1   |
| 52  | cpu_coldreset_n      |     | 104 | pci_ad[6]            |     | 156 | pci_gnt_n[1]         | 2   | 208 | uart_rx[0]           | 1   |

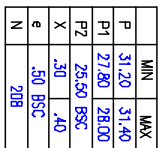
Table 13 RC32332 208-pin QFP Package Pin-Out (Part 2 of 2)

RC32332 Package Drawing — 208-pin PQFP



| REV. VERSIONS |     |                        |          |          |
|---------------|-----|------------------------|----------|----------|
| DCN           | REV | DESCRIPTION            | DATE     | APPROVED |
| 28253         | D0  | INITIAL RELEASE        | 08/20/96 | T. WU    |
| 61476         | D1  | ADD 'D' PACKAGE OPTION | 09/20/96 | T. WU    |
| 61829         | D2  | ADD 'D' PACKAGE OPTION | 01/30/99 |          |

## LAND PATTERN DIMENSIONS



## NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- ▲ TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- ▲ DATUMS [A-B] AND [D-D'] TO BE DETERMINED AT DATUM PLANE [H-H']
- ▲ DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [C-C']
- ▲ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- ▲ DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- ▲ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIIUS OR THE FOOT.
- ▲ EXACT SHAPE OF EACH CORNER IS OPTIONAL
- ▲ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1

[illegible]