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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32v332-133dhg

- ◆ 2KB of 2-way set associative data cache, capable of write-back and write-through operation.
- ◆ Cache locking per line to speed real-time systems and critical system functions
- ◆ On-chip TLB to enable multi-tasking in modern operating systems
- ◆ EJTAG interface to enable sophisticated low-cost in-circuit emulation.

Synchronous-DRAM Interface

The RC32332 integrates a SDRAM controller which provides direct control of system SyncDRAM running at speeds to 75MHz.

Key capabilities of the SDRAM controller include:

- ◆ Direct control of 4 banks of SDRAM (up to 2 64-bit wide DIMMs)
- ◆ On-chip page comparators optimize access latency.
- ◆ Speeds to 75MHz
- ◆ Programmable address map.
- ◆ Supports 16, 64, 128, 256, or 512Mb SDRAM devices
- ◆ Automatic refresh generation driven by on-chip timer
- ◆ Support for discrete devices, SODIMM, or DIMM modules.

Thus, systems can take advantage of the full range of commodity memory that is available, enabling system optimization for cost, real-estate, or other attributes.

Local Memory and I/O Controller

The local memory and I/O controller implements direct control of external memory devices, including the boot ROM as well as other memory areas, and also implements direct control of external peripherals.

The local memory controller is highly flexible, allowing a wide range of devices to be directly controlled by the RC32332 processor. For example, a system can be built using an 8-bit boot ROM, 16-bit FLASH cards (possibly on PCMCIA), a 32-bit SRAM or dual-port memory, and a variety of low-cost peripherals.

Key capabilities include:

- ◆ Direct control of EPROM, FLASH, RAM, and dual-port memories
- ◆ 6 chip-select outputs, supporting up to 8MB per memory space
- ◆ Supports mixture of 8-, 16-, and 32-bit wide memory regions
- ◆ Flexible timing protocols allow direct control of a wide variety of devices
- ◆ Programmable address map for 2 chip selects
- ◆ Automatic wait state generation.

PCI Bus Bridge

In order to leverage the wide availability of low-cost peripherals for the PC market as well as to simplify the design of add-in functions, the RC32332 integrates a full 32-bit PCI bus bridge. Key attributes of this bridge include:

- ◆ 50 MHz operation
- ◆ PCI revision 2.2 compliant
- ◆ Programmable address mappings between CPU/Local memory and PCI memory and I/O
- ◆ On-chip PCI arbiter
- ◆ Extensive buffering allows PCI to operate concurrently with local memory transfers
- ◆ Selectable byte-ordering swapper.

On-Chip DMA Controller

To minimize CPU exception handling and maximize the efficiency of system bandwidth, the RC32332 integrates a very sophisticated 4-channel DMA controller on chip.

The RC32332 DMA controller is capable of:

- ◆ Chaining and scatter/gather support through the use of a flexible, linked list of DMA transaction descriptors
- ◆ Capable of memory<->memory, memory<->I/O, and PCI<->memory DMA
- ◆ Unaligned transfer support
- ◆ Byte, halfword, word, quadword DMA support.

On-Chip Peripherals

The RC32332 also integrates peripherals that are common to a wide variety of embedded systems.

- ◆ Single 16550 compatible UART.
- ◆ SPI master mode interface for direct interface to EEPROM, A/D, etc.
- ◆ Interrupt Controller to speed interrupt decode and management
- ◆ Four 32-bit on-chip Timer/Counters
- ◆ Programmable I/O module

Debug Support

To facilitate rapid time to market, the RC32332 provides extensive support for system debug.

First and foremost, this product integrates an EJTAG in-circuit emulation module, allowing a low-cost emulator to interoperate with programs executing on the controller. By using an augmented JTAG interface, the RC32332 is able to reuse the same low-cost emulators developed around the RC32364 CPU.

Pin Description Table

The following table lists the pins provided on the RC32332. Note that those pin names followed by “_n” are active-low signals. All external pull-ups and pull-downs require 10 kΩ resistor.

Name	Type	Reset State Status	Drive Strength Capability	Description																														
Local System Interface																																		
mem_data[31:0]	I/O	Z	High	Local system data bus Primary data bus for memory. I/O and SDRAM.																														
mem_addr[22:2]	I/O	[22:10] Z [9:2] L	[22:17] Low [16:2] High	Memory Address Bus These signals provide the Memory or DRAM address, during a Memory or DRAM bus transaction. During each word data, the address increments either in linear or sub-block ordering, depending on the transaction type. The table below indicates how the memory write enable signals are used to address discreet memory port width types. <table border="1"> <thead> <tr> <th>Port Width</th><th colspan="4">Pin Signals</th></tr> <tr> <th></th><th>mem_we_n[3]</th><th>mem_we_n[2]</th><th>mem_we_n[1]</th><th>mem_we_n[0]</th></tr> </thead> <tbody> <tr> <td>DMA (32-bit)</td><td>mem_we_n[3]</td><td>mem_we_n[2]</td><td>mem_we_n[1]</td><td>mem_we_n[0]</td></tr> <tr> <td>32-bit</td><td>mem_we_n[3]</td><td>mem_we_n[2]</td><td>mem_we_n[1]</td><td>mem_we_n[0]</td></tr> <tr> <td>16-bit</td><td>Byte High Write Enable</td><td>mem_addr[1]</td><td>Not Used (Driven Low)</td><td>Byte Low Write Enable</td></tr> <tr> <td>8-bit</td><td>Not Used (Driven High)</td><td>mem_addr[1]</td><td>mem_addr[0]</td><td>Byte Write Enable</td></tr> </tbody> </table> mem_addr[22] Alternate function: reset_boot_mode[1]. mem_addr[21] Alternate function: reset_boot_mode[0]. mem_addr[20] Alternate function: reset_pci_host_mode. mem_addr[19] Alternate function: modebit [9]. mem_addr[18] Alternate function: modebit [8]. mem_addr[17] Alternate function: modebit [7]. mem_addr[16] Alternate function: sdram_addr[16]. mem_addr[15] Alternate function: sdram_addr[15]. mem_addr[14] Alternate function: sdram_addr[14]. mem_addr[13] Alternate function: sdram_addr[13]. mem_addr[11] Alternate function: sdram_addr[11]. mem_addr[10] Alternate function: sdram_addr[10]. mem_addr[9] Alternate function: sdram_addr[9]. mem_addr[8] Alternate function: sdram_addr[8]. mem_addr[7] Alternate function: sdram_addr[7]. mem_addr[6] Alternate function: sdram_addr[6]. mem_addr[5] Alternate function: sdram_addr[5]. mem_addr[4] Alternate function: sdram_addr[4]. mem_addr[3] Alternate function: sdram_addr[3]. mem_addr[2] Alternate function: sdram_addr[2].	Port Width	Pin Signals					mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]	DMA (32-bit)	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]	32-bit	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]	16-bit	Byte High Write Enable	mem_addr[1]	Not Used (Driven Low)	Byte Low Write Enable	8-bit	Not Used (Driven High)	mem_addr[1]	mem_addr[0]	Byte Write Enable
Port Width	Pin Signals																																	
	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]																														
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32-bit	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]																														
16-bit	Byte High Write Enable	mem_addr[1]	Not Used (Driven Low)	Byte Low Write Enable																														
8-bit	Not Used (Driven High)	mem_addr[1]	mem_addr[0]	Byte Write Enable																														
mem_cs_n[5:0]	Output	H	Low	Memory Chip Select Negated Recommend an external pull-up. Signals that a Memory Bank is actively selected.																														
mem_oe_n	Output	H	High	Memory Output Enable Negated Recommend an external pull-up. Signals that a Memory Bank can output its data lines onto the cpu_ad bus.																														
mem_we_n[3:0]	Output	H	High	Memory Write Enable Negated Bus Signals which bytes are to be written during a memory transaction. Bits act as Byte Enable and mem_addr[1:0] signals for 8-bit or 16-bit wide addressing.																														

Table 1 Pin Descriptions (Part 1 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
pci_req_n[2]	Input	Z	—	PCI Bus Request #2 Negated Requires an external pull-up. Host mode: pci_req_n[2] is an input indicating a request from an external device. Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write. Alternate function: pci_idsel (satellite).
pci_req_n[0]	I/O	Z	High	PCI Bus Request #0 Negated Requires an external pull-up for burst mode. Host mode: pci_req_n[0] is an input indicating a request from an external device. Satellite mode: pci_req_n[0] is an output indicating a request from this device.
pci_gnt_n[2]	Output	Z ¹	High	PCI Bus Grant #2 Negated Recommend an external pull-up. Host mode: pci_gnt_n[2] is an output indicating a grant to an external device. Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin. External pull-up is required. Alternate function: pci_inta_n (satellite).
pci_gnt_n[1] (can only be used as alternate function)	I/O	X for 1 pci clock then H ²	High	PCI Bus Grant #1 Negated Recommend external pull-up. Host mode: not used as pci_gnt_n[1]. Must be used as alternate function PIO[7]. Satellite mode: Not used as pci_gnt_n[1]. Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32332 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time. 1st Alternate function: pci_eeprom_cs (satellite). 2nd Alternate function: PIO[7].
pci_gnt_n[0]	I/O	Z	High	PCI Bus Grant #0 Negated Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up. Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Requires external pull-up.
pci_inta_n	Output Open-collector	Z	PCI	PCI Interrupt #A Negated Uses pci_gnt_n[2]. See the PCI subsection.
pci_lock_n	Input		—	PCI Lock Negated Driven by the Bus Master to indicate that an exclusive operation is occurring.

¹ Z in host mode; L in satellite non-boot mode; Z in satellite boot mode.
² H in host mode, L in satellite non-boot and boot modes. X = unknown.

SDRAM Control Interface

sdram_addr_12	Output	L	High	SDRAM Address Bit 12 and Precharge All SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command.
sdram_ras_n	Output	H	High	SDRAM RAS Negated SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks.
sdram_cas_n	Output	H	High	SDRAM CAS Negated SDRAM mode: Provides SDRAM CAS control signal to all SDRAM banks.
sdram_we_n	Output	H	High	SDRAM WE Negated SDRAM mode: Provides SDRAM WE control signal to all SDRAM banks.
sdram_cke	Output	H	High	SDRAM Clock Enable SDRAM mode: Provides clock enable to all SDRAM banks.
sdram_cs_n[3:0]	Output	H	High	SDRAM Chip Select Negated Bus Recommend an external pull-up. SDRAM mode: Provides chip select to each SDRAM bank. SODIMM mode: Provides upper select byte enables [7:4].
sdram_s_n[1:0]	Output	H	High	SDRAM SODIMM Select Negated Bus SDRAM mode: Not used. SDRAM SODIMM mode: Upper and lower chip selects.

Table 1 Pin Descriptions (Part 3 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
spi_ss_n	I/O	H	Low	SPI Chip Select Output pin selecting the serial protocol device as opposed to the PCI satellite mode EEPROM device. Alternate function: PIO[4]. Defaults to the output direction at reset time.

CPU Core Specific Signals

cpu_nmi_n	Input		—	CPU Non-Maskable Interrupt Requires an external pull-up. This interrupt input is active low to the CPU.
cpu_masterclk	Input		—	CPU Master System Clock Provides the basic system clock.
cpu_int_n[1:0]	Input		—	CPU Interrupt Requires an external pull-up. These interrupt inputs are active low to the CPU.
cpu_coldreset_n	Input	L	—	CPU Cold Reset This active-low signal is asserted to the RC32332 after V_{CC} becomes valid on the initial power-up. The Reset initialization vectors for the RC32332 are latched by cold reset.
cpu_dt_r_n	Output	Z	—	CPU Direction Transmit/Receive This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations. 1st Alternate function: mem_245_dt_r_n. 2nd Alternate function: sdram_245_dt_r_n.

JTAG Interface Signals

jtag_tck	Input		—	JTAG Test Clock Requires an external pull-down. An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle.
jtag_tdi, ejtag_dint_n	Input		—	JTAG Test Data In Requires an external pull-up. On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode.
jtag_tdo, ejtag_tpc	Output	Z	High	JTAG Test Data Out The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode.
jtag_tms	Input		—	JTAG Test Mode Select Requires an external pull-up. The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck.
jtag_trst_n	Input	L	—	JTAG Test Reset When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked.
ejtag_dclk	Output	Z	—	EJTAG Test Clock Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline.

Table 1 Pin Descriptions (Part 5 of 6)

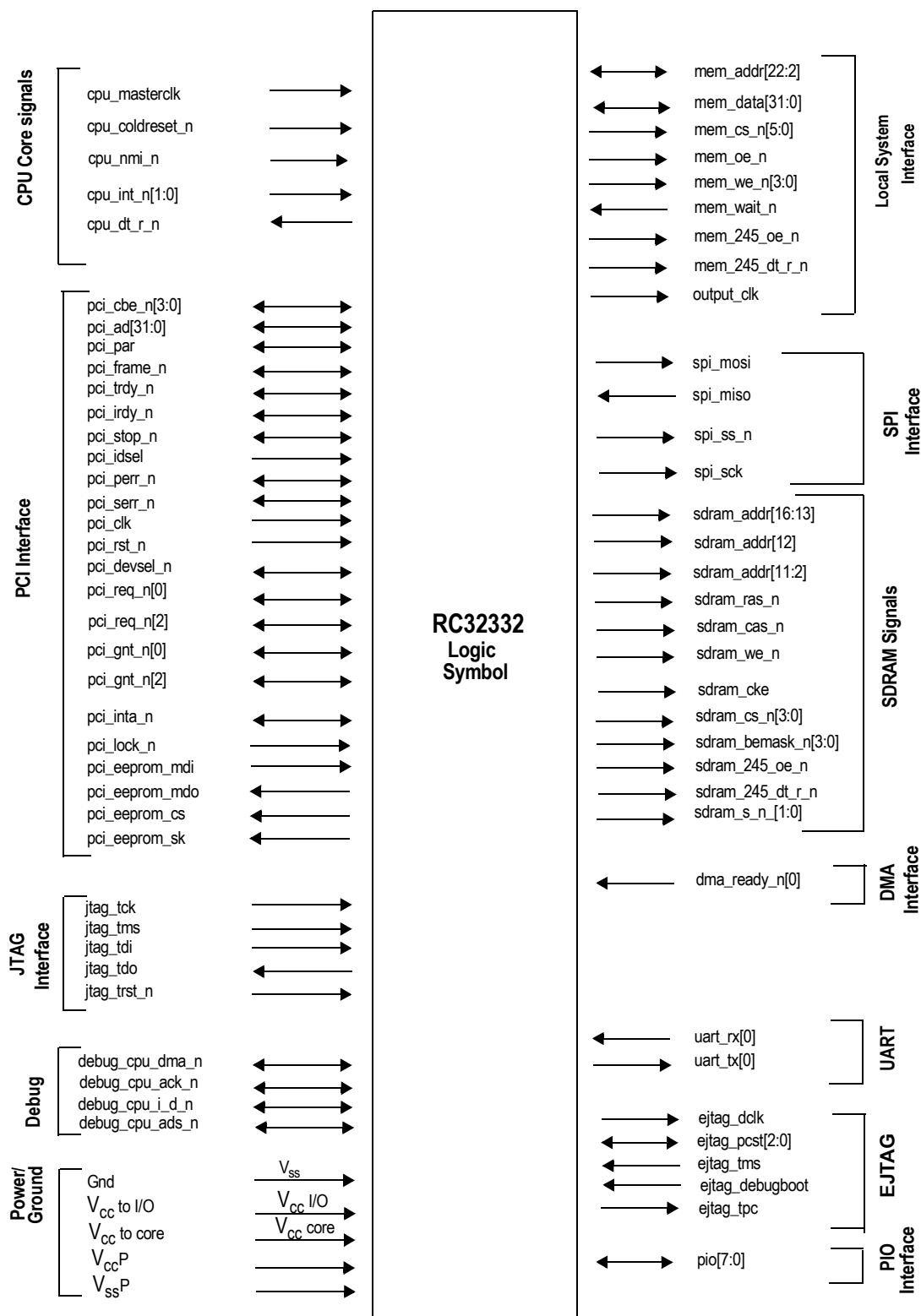
Name	Type	Reset State Status	Drive Strength Capability	Description
ejtag_pcst[2:0]	I/O	Z	Low	EJTAG PC Trace Status Information 111 (STL) Pipe line Stall 110 (JMP) Branch/Jump forms with PC output 101 (BRT) Branch/Jump forms with no PC output 100 (EXP) Exception generated with an exception vector code output 011 (SEQ) Sequential performance 010 (TST) Trace is outputted at pipeline stall time 001 (TSQ) Trace trigger output at performance time 000 (DBM) Run Debug Mode Alternate function: modebit[2:0].
ejtag_debugboot	Input		—	EJTAG DebugBoot Requires an external pull-down. The ejtag_debugboot input is used during reset and forces the CPU core to take a debug exception at the end of the reset sequence instead of a reset exception. This enables the CPU to boot from the ICE probe without having the external memory working. This input signal is level sensitive and is not latched internally. This signal will also set the JtagBrk bit in the JTAG_Control_Register[12].
ejtag_tms	Input		—	EJTAG Test Mode Select Requires an external pull-up. The ejtag_tms is sampled on the rising edge of jtag_tck.

Debug Signals

debug_cpu_dma_n	I/O	Z	Low	Debug CPU versus DMA Negated De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU. Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA. Alternate function: modebit[6].
debug_cpu_ack_n	I/O	Z	Low	Debug CPU Acknowledge Negated Indicates either a data acknowledge to the CPU or DMA. Alternate function: modebit[4].
debug_cpu_ads_n	I/O	Z	Low	Debug CPU Address/Data Strobe Negated Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address. Alternate function: modebit[5].
debug_cpu_i_d_n	I/O	Z	Low	Debug CPU Instruction versus Data Negated Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction. De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction. Alternate function: modebit[3].

Table 1 Pin Descriptions (Part 6 of 6)

Logic Diagram — RC32332



pci_host_mode Settings

During cold reset initialization, the RC32332's PCI interface can be set to the Satellite or Host mode settings. When set to the Host mode, the CPU must configure the RC32332's PCI configuration registers, including the read-only registers. If the RC32332's PCI is in the PCI-boot mode Satellite mode, read-only configuration registers are loaded by the serial EEPROM.

Pin	Reset Boot Mode	Description	Value	Mode Settings
mem_addr[20]	PCI host mode	PCI is in satellite mode	1	PCI_satellite
		PCI is in host mode (typical system)	0	PCI_host

Table 4 RC32332 pci_host_mode Initialization Settings

Clock Parameters — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V_{cc} Core = +3.3V±5%; V_{cc} I/O = +3.3V±5%

2.5V version: V_{cc} Core = +2.5V±5%; V_{cc} I/O = +3.3V±5%

Parameter	Symbol	Test Conditions	RC32332 100MHz		RC32332 133MHz		RC32332 150MHz		Units
			Min	Max	Min	Max	Min	Max	
cpu_masterclock HIGH	t _{MCHIGH}	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock LOW	t _{MCLOW}	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock period ¹ - 3.3V ver.	t _{MCP}	—	20	66.6	15	66.6	13.33	66.6	ns
cpu_masterclock period ¹ - 2.5V ver.	t _{MCP}	—	20	40.0	15	40.0	13.33	40.0	ns
cpu_masterclock Rise & Fall Time ²	t _{MCRise} , t _{MCFall}	—	—	3	—	3	—	3	ns
cpu_masterclock Jitter	t _{JITTER}	—	—	± 250	—	± 250	—	± 200	ps
pci_clk Rise & Fall Time	t _{PCRise} , t _{PCFall}	PCI 2.2	—	1.6	—	1.6	—	1.6	ns
pci_clk Period ¹	t _{PCP}	—	20	—	20	—	20	—	ns
jtag_tck Rise & Fall Time	t _{JCRise} , t _{JCFall}	—	—	5	—	5	—	5	ns
ejtag_dck period	t _{DCK} , t _{t1}	—	10	—	10	—	10	—	ns
jtag_tck clock period	t _{TCK} , t _{t3}	—	100	—	100	—	100	—	ns
ejtag_dclk High, Low Time	t _{DCK High} , t _{t9} t _{DCK Low} , t _{t10}	—	4	—	4	—	4	—	ns
ejtag_dclk Rise, Fall Time	t _{DCK Rise} , t _{t9} t _{DCK Fall} , t _{t10}	—	—	1	—	1	—	1	ns
output_clk ³	t _{DO21}	—	N/A	N/A	N/A	N/A	N/A	N/A	—
cpu_coldreset_n Asserted during power-up	—	power-on sequence	120	—	120	—	120	—	ms
cpu_coldreset_n Rise Time	t _{CRRise}	—	—	5	—	5	—	5	ns

Table 5 Clock Parameters - RC32332

¹ cpu_masterclock frequency should never be below pci_clk frequency if PCI interface is used.

² Rise and Fall times are measured between 10% and 90%.

³ Output_clk should not be used in a system. Only the cpu_masterclock or its derivative must be used to drive all the subsystems with designs based on the RC32334/RC32332. Refer to the RC32334/RC32332 Device Errata for more information.

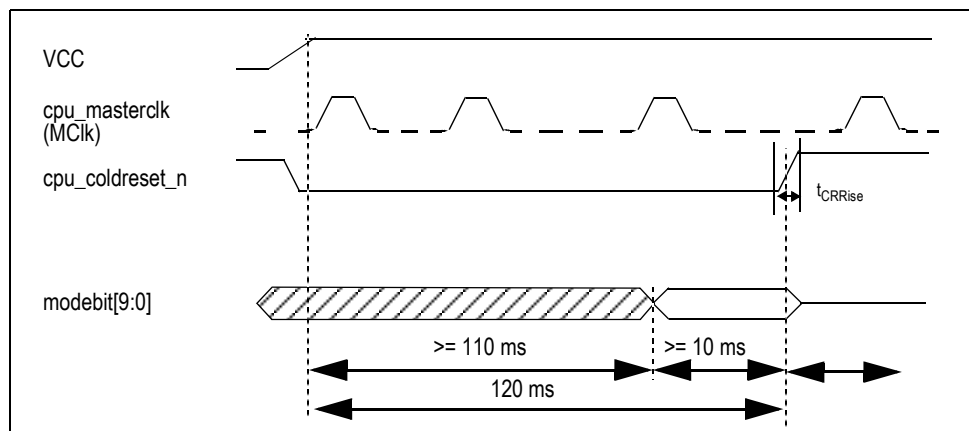
Reset Specification

Figure 3 Mode Configuration Interface Cold Reset Sequence

Signal	Symbol	Reference Edge	100MHz ¹		133MHz ¹		150MHz ¹		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdi	Thld	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdo, pci-eeprom_cs	Tdo	pci_clk rising, pci_eeprom_sk falling	—	15	—	12	—	10	ns	
pci_eeprom_sk	Tdo	pci_clk rising	—	15	—	12	—	10	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
pci_req_n[0], pci_gnt_n[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	

PCI for 2.5V Device³

pci_ad[31:0], pci_par, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n ⁴	Tsu	pci_clk rising	3	—	3	—	3	—	ns	
pci_cbe_n[3:0], pci_frame_n, pci_trdy_n, pci_irdy_n	Tsu	pci_clk rising	4	—	4	—	4	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_gnt_n[0]	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n ⁴	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdi	Thld	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdo, pci-eeprom_cs	Tdo	pci_clk rising, pci_eeprom_sk falling	—	15	—	12	—	10	ns	
pci_eeprom_sk	Tdo	pci_clk rising	—	15	—	12	—	10	ns	

Table 6 AC Timing Characteristics - RC32332 (Part 2 of 4)

Standard EJTAG Timing — RC32332

Figure 4 represents the timing diagram for the EJTAG interface signals.

The standard JTAG connector is a 10-pin connector providing 5 signals and 5 ground pins. For Standard EJTAG, a 24-pin connector has been chosen providing 12 signals and 12 ground pins. This guarantees elimination of noise problems by incorporating signal-ground type arrangement. Refer to the RC32334/RC32332 User Reference Manual for connector pinout and mechanical specifications.

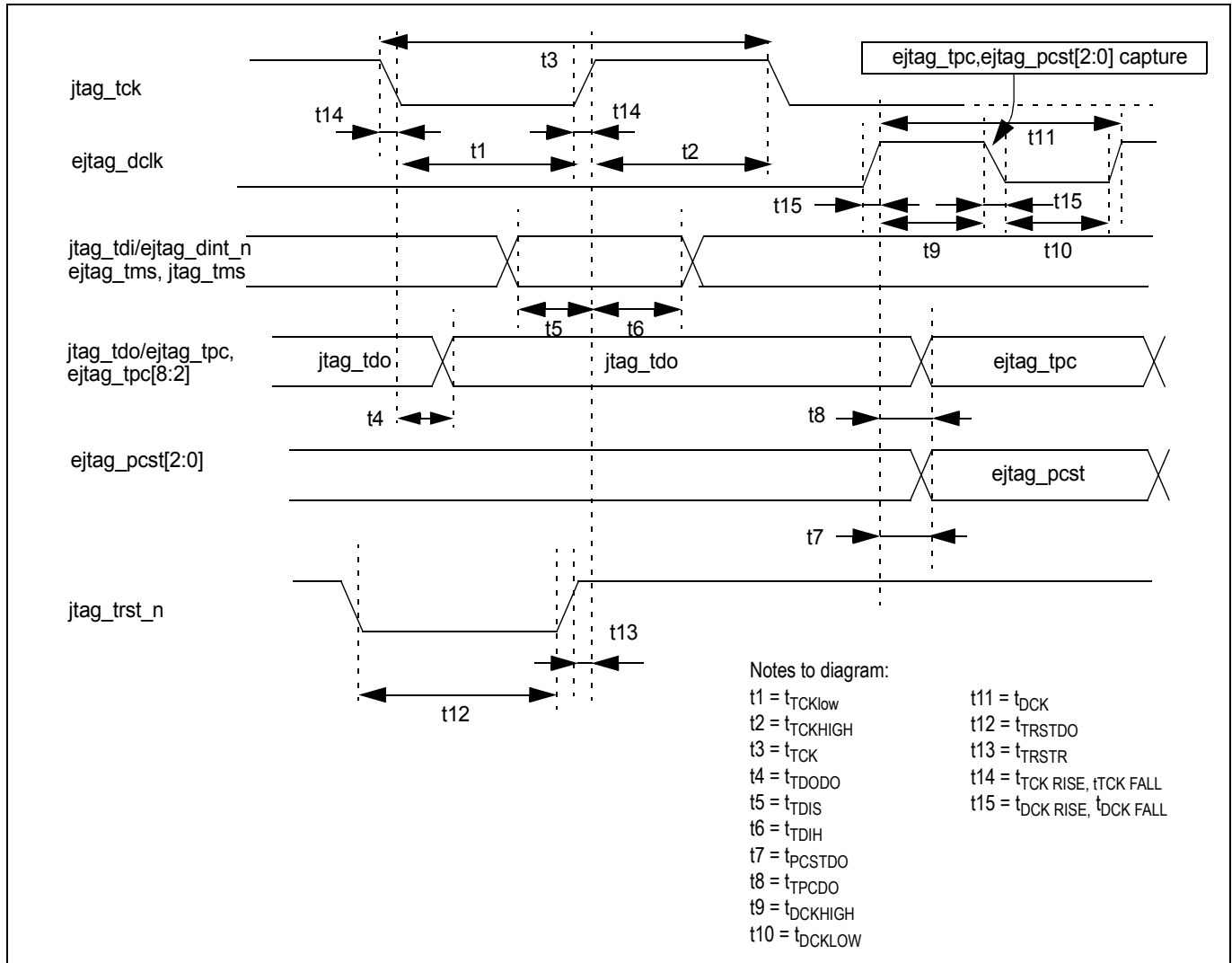
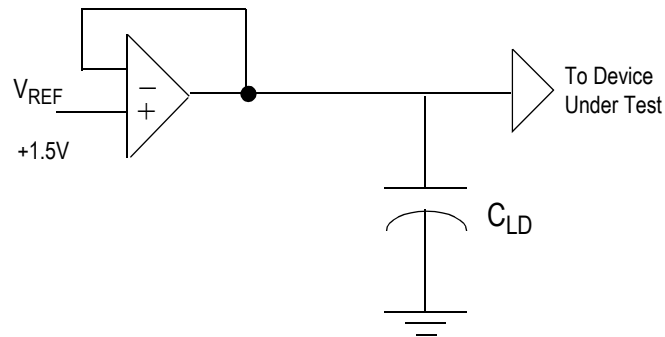


Figure 4 Standard EJTAG Timing

Output Loading for AC Testing



Signal	Cld
All High Drive Signals	50 pF
All Low Drive Signals	25 pF

Figure 5 Output Loading for AC Testing

Note: PCI pins have been correlated to PCI 2.2.

Recommended Operation Temperature and Supply Voltage

3.3V Device

Grade	Ambient Temperature	Gnd	V _{ccIO}	V _{ccCore}	V _{ccP}
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C Ambient	0V	3.3V±5%	3.3V±5%	3.3V±5%

Table 7 Temperature and Voltage — 3.3V Device

2.5V Device

Grade	Ambient Temperature	Gnd	V _{ccIO}	V _{ccCore}	V _{ccP}
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	2.5V±5%	2.5V±5%
Industrial	-40°C to +85°C Ambient	0V	3.3V±5%	2.5V±5%	2.5V±5%

Table 8 Temperature and Voltage — 2.5V Device

Power Consumption

3.3V Device

Note: This table is based on a 2:1 pipeline-to-bus clock ratio.

Parameter		100MHz		133MHz		150MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I _{CC}	Normal mode	360	480	480	630	550	700	mA	C _L = (See Figure 5, Output Loading for AC Testing) T _a = 25°C V _{CC} Core = 3.46V (for max. values) V _{CC} I/O = 3.46V (for max. values) V _{CC} Core = 3.3V (for typical values) V _{CC} I/O = 3.3V (for typical values)
	Standby mode ¹	250	370	330	480	390	540	mA	
Power Dissipation	Normal mode	1.2	1.7	1.5	2.2	1.7	2.4	W	
	Standby mode ¹	0.83	1.3	1.1	1.7	1.3	1.9	W	

Table 10 Power Consumption — 3.3V Device

¹ RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

2.5V Device

Note: This table is based on a 2:1 pipeline-to-bus clock ratio.

Parameter		100MHz		133MHz		150MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I _{CC} I/O	Normal mode	24	81	32	93	35	104	mA	C _L = (See Figure 5, Output Loading for AC Testing) T _a = 25°C V _{CC} Core = 2.625V (for max. values) V _{CC} I/O = 3.46V (for max. values) V _{CC} Core = 2.5V (for typical values) V _{CC} I/O = 3.3V (for typical values)
	Standby mode ¹	2	81	2	93	2	104	mA	
I _{CC} core	Normal mode	232	301	298	392	333	438	mA	
	Standby mode ¹	120	269	151	319	168	345	mA	
Power Dissipation	Normal mode	0.66	1.07	0.85	1.35	0.95	1.51	W	
	Standby mode ¹	0.31	0.94	0.38	1.10	0.43	1.21	W	

Table 11 Power Consumption — 2.5V Device

¹ RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

Power Ramp-up

3.3V Device

There is no special requirement for how fast V_{CC} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{CC} I/O.

2.5V Device

The 2.5V core supply (and 2.5V V_{CC}P supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast V_{CC} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{CC} I/O.

Power Curves

The following four graphs contain the simulated power curves that show power consumption at various bus frequencies. Figures 6 and 7 apply to the 3.3V device, while Figures 8 and 9 apply to the 2.5V device.

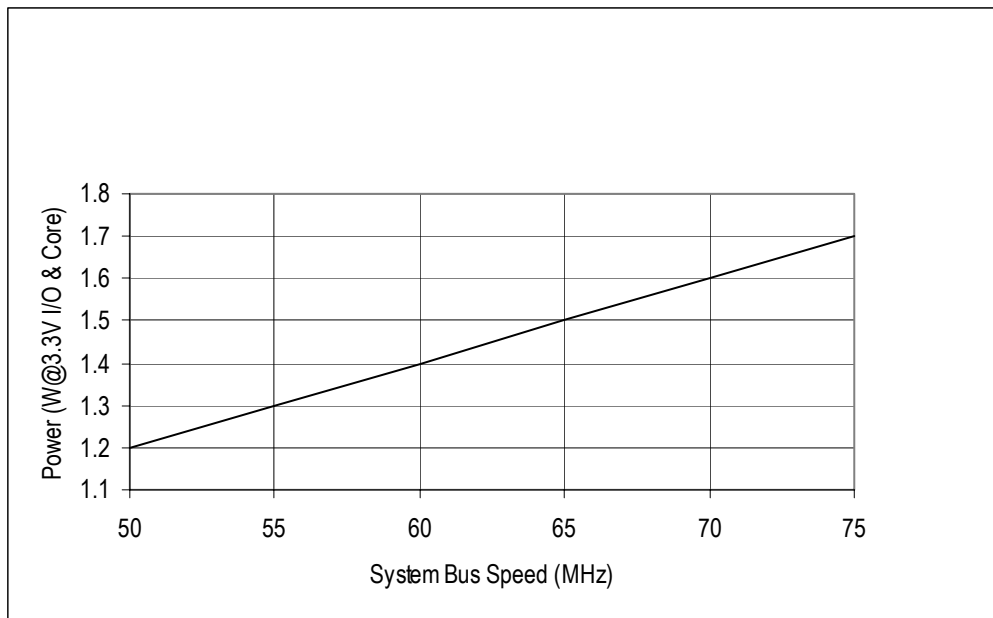


Figure 6 Typical Power Usage — RC32V332 Device

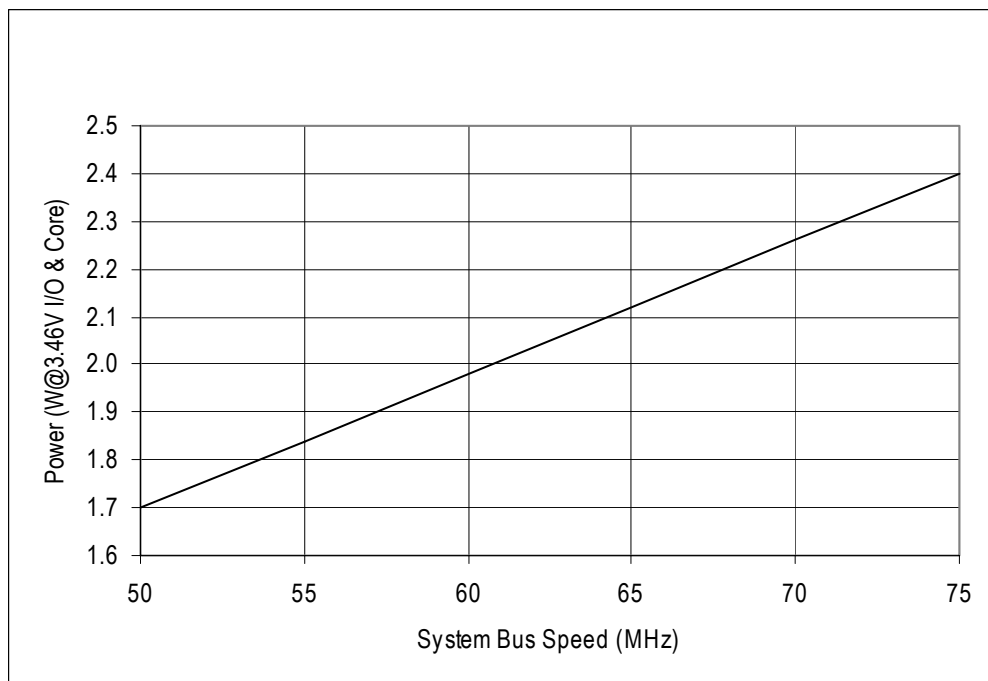


Figure 7 Maximum Power Usage — RC32V332 Device

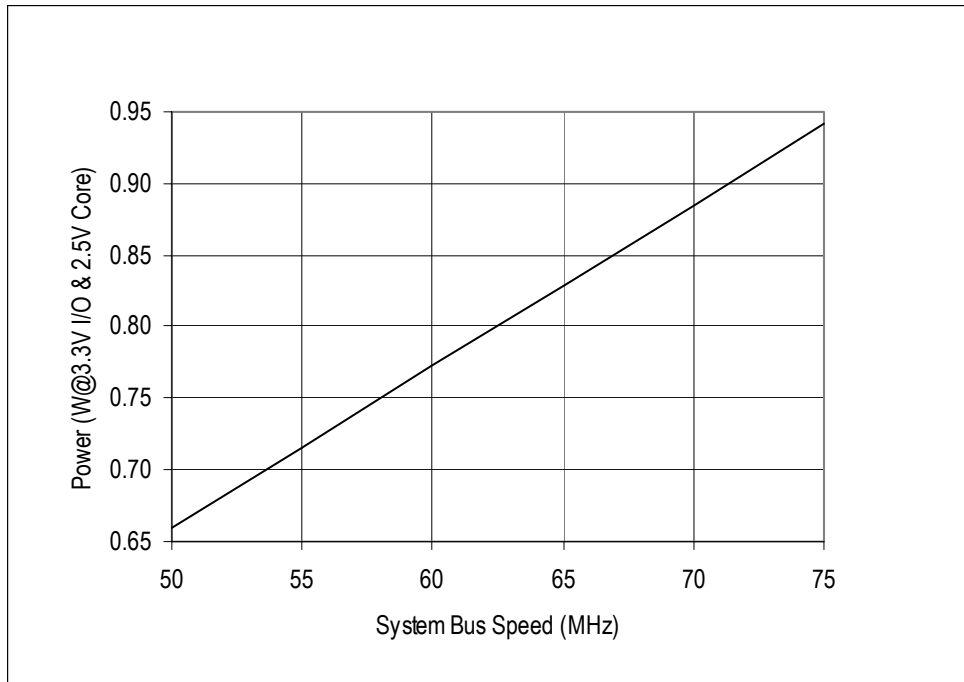


Figure 8 Typical Power Usage — RC32T332 Device

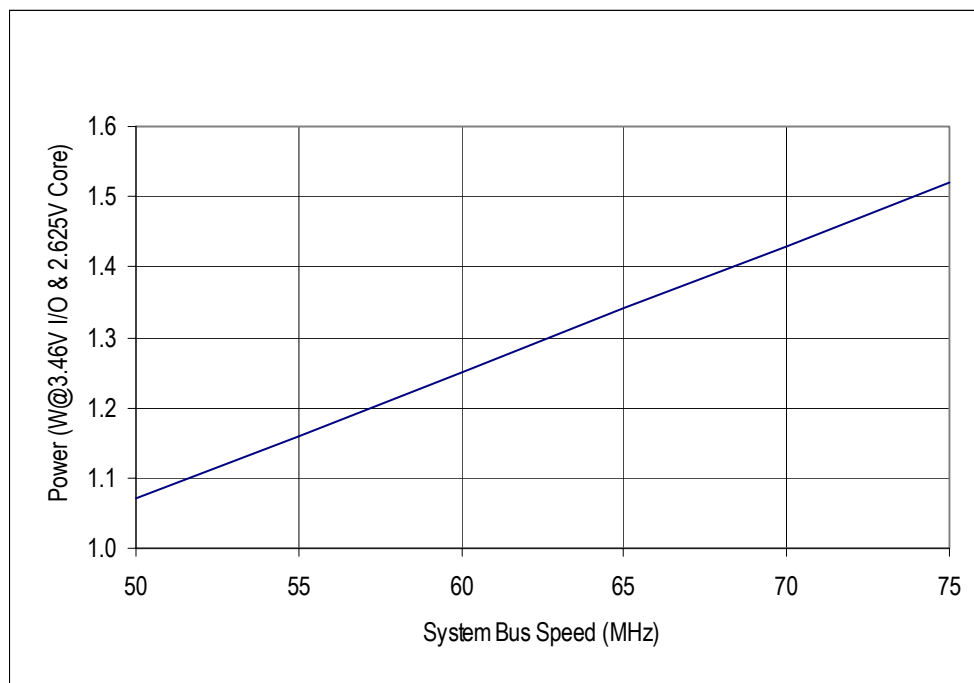


Figure 9 Maximum Power Usage — RC32T332 Device

Absolute Maximum Ratings

Symbol	Parameter	Min ¹	Max ¹	Unit
V _{cc} Core 3.3V Device	Supply Voltage	-0.3	4.0	V
V _{cc} Core 2.5V Device	Supply Voltage	-0.3	3.0	V
V _{cc} I/O	I/O Supply Voltage	-0.3	4.0	V
V _i 3.3V Device	Input Voltage	-0.3	5.5	V
V _i 2.5V Device	Input Voltage	-0.3	V _{cc} /O+0.3	V
V _{imin}	Input Voltage - undershoot ²	-0.6	—	V
T _{stg}	Storage Temperature	-40	125	degrees C

Table 12 Absolute Maximum Ratings

¹ Functional and tested operating conditions are given in Table 7. Absolute maximum ratings are stress ratings only, and functional operation is not guaranteed beyond recommended operating voltages and temperatures. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

² All PCI pads are fully compatible with PCI Specification version 2.2.

Package Pin-out — 208-PQFP for RC32332

The following table lists the pin numbers and signal names for the RC32332. Signal names ending with an _n are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	sdram_245_oe_n		53	mem_data[12]		105	pci_ad[7]		157	pci_req_n[2]	1
2	sdram_we_n		54	mem_data[19]		106	pci_cbe_n[0]		158	pci_gnt_n[2]	1
3	sdram_cas_n		55	mem_data[13]		107	pci_ad[8]		159	pci_rst_n	
4	sdram_bemask_n[0]		56	mem_data[18]		108	pci_ad[9]		160	cpu_int_n[0]	
5	sdram_bemask_n[1]		57	mem_data[14]		109	pci_ad[10]		161	cpu_int_n[1]	
6	V _{ss}		58	V _{ss}		110	V _{ss}		162	V _{ss}	
7	V _{cc} I/O		59	V _{cc} I/O		111	V _{cc} I/O		163	V _{cc} I/O	
8	sdram_cs_n[0]		60	mem_data[17]		112	pci_ad[11]		164	jtag_tdi	
9	sdram_cs_n[1]		61	mem_data[16]		113	pci_ad[12]		165	jtag_tdo	
10	sdram_ras_n		62	V _{cc} core		114	pci_ad[13]		166	jtag_tms	
11	sdram_s_n[0]		63	mem_data[15]		115	pci_ad[14]		167	ejtag_tms	
12	sdram_s_n[1]		64	cpu_masterclk		116	pci_ad[15]		168	jtag_tck	
13	mem_addr[2]	1	65	mem_data[31]		117	pci_cbe_n[1]		169	jtag_trst_n	
14	mem_addr[3]	1	66	mem_data[0]		118	pci_par		170	ejtag_pcst[0]	1
15	mem_addr[4]	1	67	mem_data[30]		119	pci_serr_n		171	ejtag_pcst[1]	1
16	V _{ss}		68	V _{ss}		120	V _{ss}		172	V _{ss}	
17	V _{cc} I/O		69	V _{cc} I/O		121	V _{cc} I/O		173	V _{cc} I/O	
18	mem_addr[5]	1	70	mem_data[1]		122	pci_perr_n		174	ejtag_pcst[2]	1
19	mem_addr[6]	1	71	mem_data[29]		123	pci_lock_n		175	ejtag_dclk	

Table 13 RC32332 208-pin QFP Package Pin-Out (Part 1 of 2)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
20	mem_addr[7]	1	72	mem_data[2]		124	pci_stop_n		176	ejtag_debugboot	
21	mem_addr[8]	1	73	mem_data[28]		125	pci_devsel_n		177	debug_cpu_i_d_n	1
22	mem_addr[9]	1	74	mem_data[3]		126	pci_trdy_n		178	debug_cpu_ads_n	1
23	mem_addr[10]	1	75	mem_data[27]		127	pci_irdy_n		179	debug_cpu_ack_n	1
24	mem_addr[11]	1	76	mem_data[4]		128	pci_frame_n		180	debug_cpu_dma_n	1
25	output_clk		77	V _{cc} P		129	pci_cbe_n[2]		181	V _{cc} I/O	
26	V _{ss}		78	V _{ss} P		130	V _{ss}		182	V _{ss}	
27	V _{cc} core		79	mem_data[26]		131	V _{cc} core		183	V _{cc} core	
28	mem_addr_12		80	mem_data[5]		132	pci_ad[16]		184	V _{cc} I/O	
29	sdram_addr_12		81	V _{ss}		133	pci_ad[17]		185	spi_ss_n	1
30	sdram_cke		82	V _{cc} core		134	pci_ad[18]		186	spi_sck	2
31	sdram_cs_n[2]		83	cpu_dt_r_n	2	135	pci_ad[19]		187	spi_miso	2
32	sdram_cs_n[3]		84	mem_data[25]		136	pci_ad[20]		188	spi_mosi	2
33	sdram_bemask_n[2]		85	mem_data[6]		137	pci_ad[21]		189	dma_ready_n[0]	2
34	sdram_bemask_n[3]		86	mem_data[24]		138	pci_ad[22]		190	mem_245_oe_n	
35	mem_addr[13]		87	mem_data[7]		139	pci_ad[23]		191	mem_wait_n	2
36	V _{ss}		88	V _{ss}		140	V _{ss}		192	V _{ss}	
37	V _{cc} I/O		89	V _{cc} I/O		141	V _{cc} I/O		193	V _{cc} I/O	
38	mem_addr[14]		90	mem_data[23]		142	pci_cbe_n[3]		194	mem_oe_n	
39	mem_addr[15]	1	91	mem_data[8]		143	pci_ad[24]		195	mem_cs_n[0]	
40	mem_addr[16]	1	92	mem_data[22]		144	pci_ad[25]		196	mem_cs_n[1]	
41	mem_addr[17]	1	93	mem_data[9]		145	pci_ad[26]		197	mem_cs_n[2]	
42	mem_addr[18]	1	94	mem_data[21]		146	pci_ad[27]		198	mem_cs_n[3]	
43	mem_addr[19]	1	95	cpu_nmi_n		147	pci_ad[28]		199	mem_cs_n[4]	
44	mem_addr[20]	1	96	pci_ad[0]		148	pci_ad[29]		200	mem_cs_n[5]	
45	mem_addr[21]	1	97	pci_ad[1]		149	pci_ad[30]		201	mem_we_n[0]	
46	V _{ss}		98	V _{ss}		150	V _{ss}		202	V _{ss}	
47	V _{cc} I/O		99	V _{cc} I/O		151	V _{cc} I/O		203	V _{cc} I/O	
48	mem_addr[22]	1	100	pci_ad[2]		152	pci_ad[31]		204	mem_we_n[1]	
49	mem_data[10]		101	pci_ad[3]		153	pci_req_n[0]		205	mem_we_n[2]	
50	mem_data[11]		102	pci_ad[4]		154	pci_gnt_n[0]		206	mem_we_n[3]	
51	mem_data[20]		103	pci_ad[5]		155	pci_clk		207	uart_tx[0]	1
52	cpu_coldreset_n		104	pci_ad[6]		156	pci_gnt_n[1]	2	208	uart_rx[0]	1

Table 13 RC32332 208-pin QFP Package Pin-Out (Part 2 of 2)

RC32332 Alternate Signal Functions

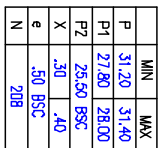
Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2
13	sdram_addr[2]		40	sdram_addr[16]		174	modebit[2]	
14	sdram_addr[3]		41	modebit[7]		177	modebit[3]	
15	sdram_addr[4]		42	modebit[8]		178	modebit[5]	
18	sdram_addr[5]		43	modebit[9]		179	modebit[4]	
19	sdram_addr[6]		44	reset_pci_host_mode		180	modebit[6]	
20	sdram_addr[7]		45	reset_boot_mode[0]		185	PIO[4]	
21	sdram_addr[8]		48	reset_boot_mode[1]		186	PIO[5]	pci_eeeprom_sk
22	sdram_addr[9]		83	mem_245_dt_r_n	sdram_245_dt_r_n	187	PIO[3]	pci_eeeprom_mdi
23	sdram_addr[10]		156	pci_eeeprom_cs (satellite)	PIO[7]	188	PIO[6]	pci_eeeprom_mdo
24	sdram_addr[11]		157	pci_idsel (satellite)		189	PIO[0]	dma_done_n[0]
35	sdram_addr[13]		158	pci_inta_n (satellite)		191	sdram_wait_n	mem_wait_n
38	sdram_addr[14]		170	modebit[0]		207	PIO[1]	
39	sdram_addr[15]		171	modebit[1]		208	PIO[2]	

Table 14 RC32332 Alternate Signal Functions






REV. VERSIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
28253	D0	INITIAL RELEASE	08/20/96	T. WU
61478	D1	ADD 1 st PACKAGE OPTION	09/20/98	T. WU
61829	D2	ADD 2 nd PACKAGE OPTION	01/30/99	

LAND PATTERN DIMENSIONS



NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- 2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- 3 DATUMS   TO BE DETERMINED AT DATUM PLANE
- 4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE  TO BE DETERMINED AT SEATING PLANE
- 5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION, ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- 6 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- 7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION, DAMBAR CANNOT BE LOCATED ON THE LOWER RADIIUS OR THE FOOT.
- 8 EXACT SHAPE OF EACH CORNER IS OPTIONAL
- 9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1

TOLANSING		DATE	
DRUM	APPROVALS	TITLE	
2	2	05/04/DR PACKAGE OUTLINE	
2	2	26.0 X 26.0 X 3.4 mm PQRP	
2	2	1.30, 25 MIN FORM	
2	2	PSC-4059	
2	2	REV	
2	2	SHEET 2 OF 2	

Valid Combinations

79RC32T332 - 100DH, 133DH, 150DH	Commercial
79RC32T332 - 100DHI, 133DHI, 150DHI	Industrial

