Renesas Electronics America Inc - IDT79RC32V332-150DH Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32v332-150dh

- **Serial Peripheral Interface (SPI) master mode interface**
- **UART Interface**
  - *16550 compatible UART*
  - *Baud rate support up to 1.5 Mb/s*
- **Memory & Peripheral Controller**
  - *6 banks, up to 8MB per bank*
  - *Supports 8-,16-, and 32-bit interfaces*
  - *Supports Flash ROM, SRAM, dual-port memory, and peripheral devices*
  - *Supports external wait-state generation*
  - *8-bit boot PROM support*
  - *Flexible I/O timing protocols*
- **4 DMA Channels**
  - *4 general purpose DMA, each with endianess swappers and byte lane data alignment*
  - *Supports scatter/gather, chaining via linked lists of records*
  - *Supports memory-to-memory, memory-to-I/O, memory-to-PCI, PCI-to-PCI, and I/O-to-I/O transfers*
  - *Supports unaligned transfers*
  - *Supports burst transfers*
  - *Programmable DMA bus transactions burst size (up to 16 bytes)*
- **PCI Bus Interface**
  - *32-bit PCI, up to 50 MHz*
  - *Revision 2.2 compatible*
  - *Target or master*
  - *Host or satellite*
  - *Two slot PCI arbiter*
  - *Serial EEPROM support, for loading configuration registers*
- **Off-the-shelf development tools**
- **JTAG Interface (IEEE Std. 1149.1 compatible)**
- **208 QFP Package**
- **3.3V or 2.5V core supply with 3.3V I/O supply**
  - *3.3V core supply is 5V I/O tolerant*
- **EJTAG in-circuit emulator interface**

CPU Execution Core

The RC32332 integrates the RISCore 32300, the same CPU core found in the award-winning RC32364 microprocessor. The RISCore 32300 implements the Enhanced MIPS-II ISA. Thus, it is upwardly compatible with applications written for a wide variety of MIPS architecture processors, and it is kernel compatible with the modern operating systems that support IDT's 64-bit RISController product family. The RISCore 32300 was explicitly defined and designed for integrated processor products such as the RC32332. Key attributes of the execution core found within this product include:

- High-speed, 5-stage scalar pipeline executes to 150MHz. This high performance enables the RC32332 to perform a variety of performance intensive tasks, such as routing, DSP algorithms, etc.
- 32-bit architecture with enhancements of key capabilities. Thus, the RC32332 can execute existing 32-bit programs, while enabling designers to take advantage of recent advances in CPU architecture.
- Count leading-zeroes/ones. These instructions are common to a wide variety of tasks, including modem emulation, voice over IP compression and decompression, etc.
- Cache PREFetch instruction support, including a specialized form intended to help memory coherency. System programmers can allocate and stage the use of memory bandwidth to achieve maximum performance.
- 8KB of 2-way set associative instruction cache

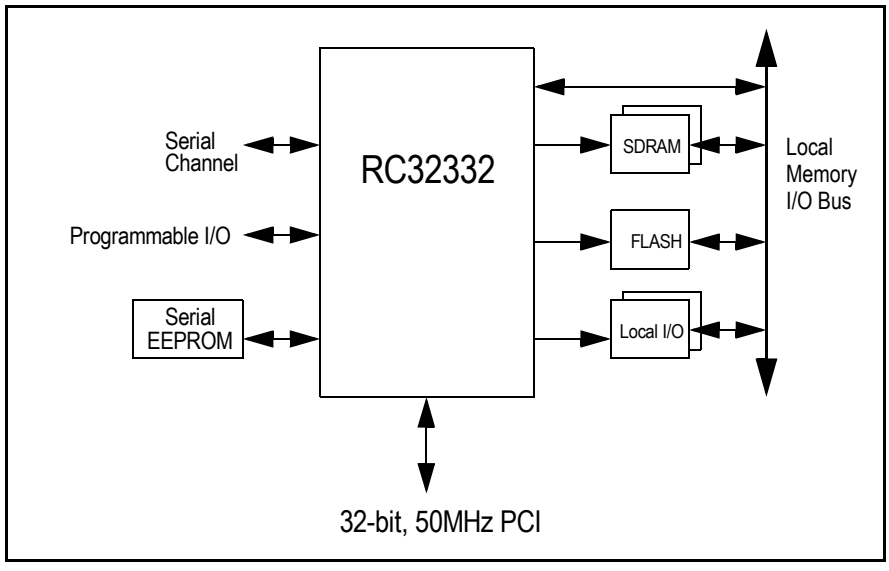


Figure 2 RC32332 Based System Diagram

Secondly, the RC32332 implements additional reporting signals intended to simplify the task of system debugging when using a logic analyzer. This product allows the logic analyzer to differentiate transactions initiated by DMA from those initiated by the CPU and further allows CPU transactions to be sorted into instruction fetches vs. data fetches.

Finally, the RC32332 implements a full boundary scan capability, allowing board manufacturing diagnostics and debug.

Packaging

The RC32332 is packaged using a 208 Quad Flat Pack (QFP) package.

Thermal Considerations

The RC32332 consumes less than 2.0 W peak power. The device is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices; -40° to +85° C for industrial temperature devices.

Revision History

November 15, 2000: Initial publication.

December 12, 2000: Changed Max values for cpu_masterclock period in Table 5 and added footnote. In Table 1, added 2nd alternate function for spi_mosi, spi_miso, spi_sck. In Table 11, added "2" in Alt column for pins 186, 187, 188. In RC32332 Alternate Signal Functions table, added pin names in Alt #2 column for pins 186, 187, 188.

January 4, 2001: In Table 6 under Interrupt Handling, changed Tdoh9 to Thld13 and moved the values for Tsu9 from the Max to the Min column.

February 23, 2001: In Table 1, changed alternate function for uart_tx[0] from PIO[3] to PIO[1]. In Table 11, changed the number of alternate pins for Pin 156 from 1 to 2. In Table 12, added PIO[7] to Alt #2 column for Pin 156 and changed PIO[3] to PIO[1] for Pin 207.

March 13, 2001: Changed upper ambient temperature for industrial and commercial uses from +70° C to +85° C.

June 7, 2001: In the Clock Parameters table, added footnote 3 to output_clk category and added NA to Min and Max columns. In Figure 3 (Reset Specification), enhanced signal line for cpu_masterclk. In Local System Interface section of AC Timing Characteristics table, changed values in Min column for last category of signals (Tdoh3) from 1.5 to 2.5 for both speeds. In SDRAM Controller section of same table, changed values in Min column for last category of signals (9 signals) from 1 to 2.5 for both speeds.

September 14, 2001: In the Reset category of Table 6: switched mem_addr[19:17] from Tsu22 and Thld22 to Tsu10 and Thld10; switched mem_addr[22:20] from Tsu10 and Thld10 to Tsu22 and Thld22; moved ejtag_pcst[2:0] from Reset to Debug Interface category under Tsu20 and Thld20.

November 1, 2001: Added Input Voltage Undershoot parameter and 2 footnotes to Table 10. Changed to DH package.

May 2, 2002: Changed from PCI 2.1 to 2.2 compliant. Added 512 MB SDRAM support. Changed upper ambient temperature for commercial uses back from +85° C to +70° C (changed erroneously from 70 to 85 on March 13, 2001). Added Reset State Status column to Table 1. Revised description of jtag_trst_n in Table 1 and changed this pin to a pull-down instead of a pull-up.

July 3, 2002: This data sheet now describes revision Y silicon and is no longer applicable to revision Z.

July 12, 2002: Added 150MHz speed grade. In Table 6: DMA section, changed Thld9 Min values from 2 to 1; in PIO section, changed Thld9 Min values from 2 to 1. Changed revision Y data sheet from Preliminary to Final.

September 18, 2002: Added cpu_coldreset_n rise time to Table 5, Clock Parameters. Added mem_addr[16] and sdram_addr[16] to Tables 1 and 12. Changed Logic Diagram to include sdram_addr[16].

December 18, 2002: In the Reset section of Table 6, AC Timing Characteristics, setup and hold time categories for cpu_coldreset_n have been deleted.

September 2, 2003: Added 2.5V version of device. Changed tables to include 2.5V values where appropriate. Added a Power Consumption table, Temperature and Voltage table, and Power Curves for the 2.5V device. In the PCI category of Table 6, created separate sections for 3.3V and 2.5V devices and in 2.5V section changed time to 4 ns for pci_cbe_n[3:0], pci_frame_n, pci_trdy_n, and pci_irdy_n. In Table 8, added 3 new categories (Input Pads, PCI Input Pads, and All Pads) and added footnotes 2 and 3. In Table 13, pins 181 and 184 were changed from Vcc Core to Vcc I/O.

March 24, 2004: In Table 1, changed description in Satellite Mode for pci_rst_n. Specified "cold" reset on pages 12 and 13. Changed several values in Table 12, Absolute Maximum Ratings, and changed footnote 1 to that table.

May 4, 2004: Revised values in Table 9, Power Consumption.

Name	Type	Reset State Status	Drive Strength Capability	Description
pci_req_n[2]	Input	Z	—	**PCI Bus Request #2 Negated** Requires an external pull-up. Host mode: pci_req_n[2] is an input indicating a request from an external device. Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write. Alternate function: pci_idsel (satellite).
pci_req_n[0]	I/O	Z	High	**PCI Bus Request #0 Negated** Requires an external pull-up for burst mode. Host mode: pci_req_n[0] is an input indicating a request from an external device. Satellite mode: pci_req_n[0] is an output indicating a request from this device.
pci_gnt_n[2]	Output	Z[1]	High	**PCI Bus Grant #2 Negated** Recommend an external pull-up. Host mode: pci_gnt_n[2] is an output indicating a grant to an external device. Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin. External pull-up is required. Alternate function: pci_inta_n (satellite).
pci_gnt_n[1] (can only be used as alternate function)	I/O	X for 1 pci clock then H[2]	High	**PCI Bus Grant #1 Negated** Recommend external pull-up. Host mode: not used as pci_gnt_n[1]. Must be used as alternate function PIO[7]. Satellite mode: Not used as pci_gnt_n[1]. Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32332 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time. 1st Alternate function: pci_eeprom_cs (satellite). 2nd Alternate function: PIO[7].
pci_gnt_n[0]	I/O	Z	High	**PCI Bus Grant #0 Negated** Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up. Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Requires external pull-up.
pci_inta_n	Output Open-collector	Z	PCI	**PCI Interrupt #A Negated** Uses pci_gnt_n[2]. See the PCI subsection.
pci_lock_n	Input		—	**PCI Lock Negated** Driven by the Bus Master to indicate that an exclusive operation is occurring.

[1] Z in host mode; L in satellite non-boot mode; Z in satellite boot mode.
[2] H in host mode, L in satellite non-boot and boot modes. X = unknown.

SDRAM Control Interface

sdram_addr_12	Output	L	High	**SDRAM Address Bit 12 and Precharge All** SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command.
sdram_ras_n	Output	H	High	**SDRAM RAS Negated** SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks.
sdram_cas_n	Output	H	High	**SDRAM CAS Negated** SDRAM mode: Provides SDRAM CAS control signal to all SDRAM banks.
sdram_we_n	Output	H	High	**SDRAM WE Negated** SDRAM mode: Provides SDRAM WE control signal to all SDRAM banks.
sdram_cke	Output	H	High	**SDRAM Clock Enable** SDRAM mode: Provides clock enable to all SDRAM banks.
sdram_cs_n[3:0]	Output	H	High	**SDRAM Chip Select Negated Bus** Recommend an external pull-up. SDRAM mode: Provides chip select to each SDRAM bank. SODIMM mode: Provides upper select byte enables [7:4].
sdram_s_n[1:0]	Output	H	High	**SDRAM SODIMM Select Negated Bus** SDRAM mode: Not used. SDRAM SODIMM mode: Upper and lower chip selects.

Table 1 Pin Descriptions (Part 3 of 6)

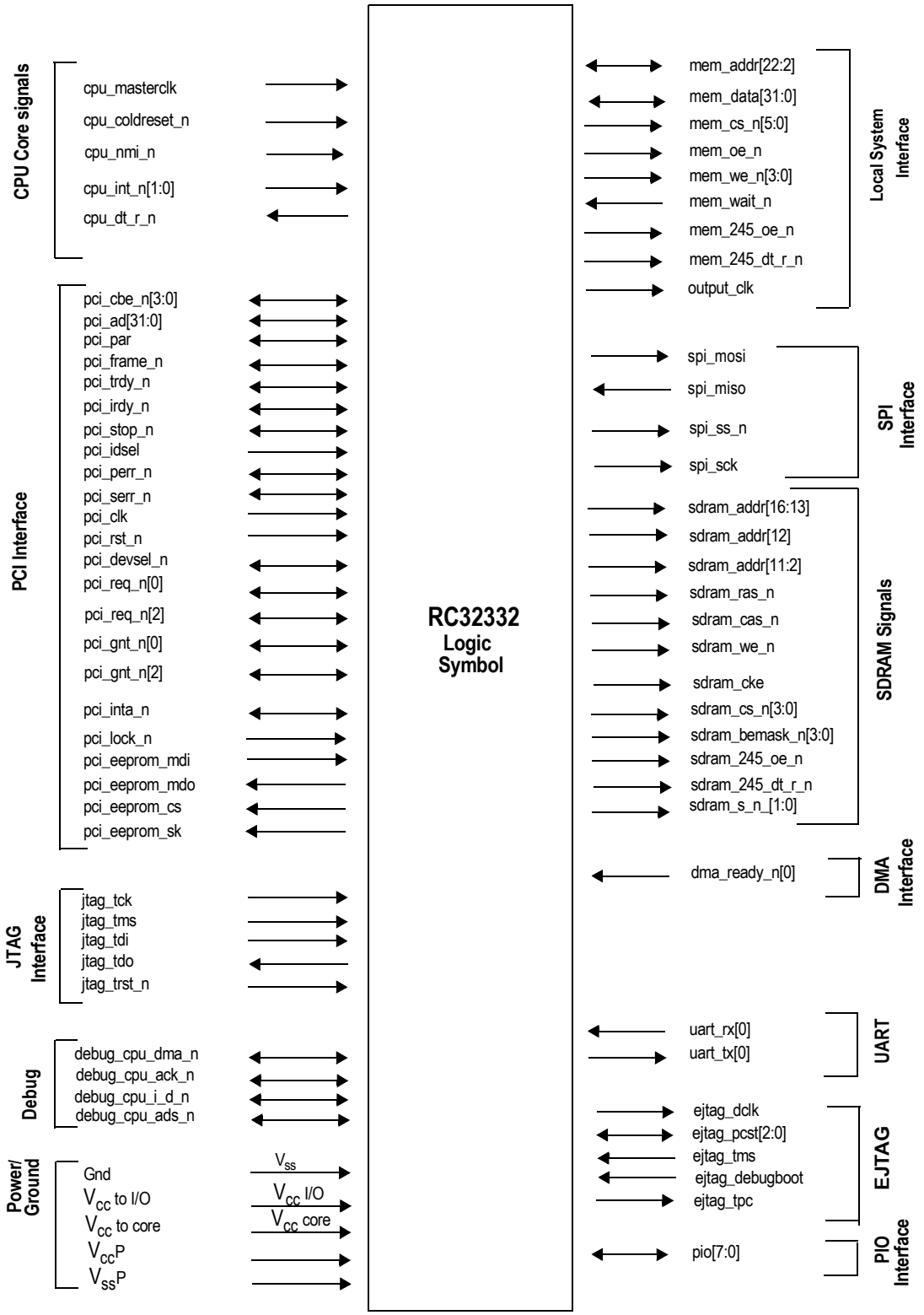
Name	Type	Reset State Status	Drive Strength Capability	Description
spi_ss_n	I/O	H	Low	**SPI Chip Select** Output pin selecting the serial protocol device as opposed to the PCI satellite mode EEPROM device. Alternate function: PIO[4]. Defaults to the output direction at reset time.
CPU Core Specific Signals				
cpu_nmi_n	Input		—	**CPU Non-Maskable Interrupt** Requires an external pull-up. This interrupt input is active low to the CPU.
cpu_masterclk	Input		—	**CPU Master System Clock** Provides the basic system clock.
cpu_int_n[1:0]	Input		—	**CPU Interrupt** Requires an external pull-up. These interrupt inputs are active low to the CPU.
cpu_coldreset_n	Input	L	—	**CPU Cold Reset** This active-low signal is asserted to the RC32332 after V_{cc} becomes valid on the initial power-up. The Reset initialization vectors for the RC32332 are latched by cold reset.
cpu_dt_r_n	Output	Z	—	**CPU Direction Transmit/Receive** This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations. 1st Alternate function: mem_245_dt_r_n. 2nd Alternate function: sdram_245_dt_r_n.
JTAG Interface Signals				
jtag_tck	Input		—	**JTAG Test Clock** Requires an external pull-down. An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle.
jtag_tdi, ejtag_dint_n	Input		—	**JTAG Test Data In** Requires an external pull-up. On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode.
jtag_tdo, ejtag_tpc	Output	Z	High	**JTAG Test Data Out** The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode.
jtag_tms	Input		—	**JTAG Test Mode Select** Requires an external pull-up. The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck.
jtag_trst_n	Input	L	—	**JTAG Test Reset** When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked.
ejtag_dclk	Output	Z	—	**EJTAG Test Clock** Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline.

Table 1 Pin Descriptions (Part 5 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
ejtag_pcst[2:0]	I/O	Z	Low	**EJTAG PC Trace Status Information** 111 (STL) Pipe line Stall 110 (JMP) Branch/Jump forms with PC output 101 (BRT) Branch/Jump forms with no PC output 100 (EXP) Exception generated with an exception vector code output 011 (SEQ) Sequential performance 010 (TST) Trace is outputted at pipeline stall time 001 (TSQ) Trace trigger output at performance time 000 (DBM) Run Debug Mode Alternate function: modebit[2:0].
ejtag_debugboot	Input		—	**EJTAG DebugBoot** Requires an external pull-down. The ejtag_debugboot input is used during reset and forces the CPU core to take a debug exception at the end of the reset sequence instead of a reset exception. This enables the CPU to boot from the ICE probe without having the external memory working. This input signal is level sensitive and is not latched internally. This signal will also set the JtagBrk bit in the JTAG_Control_Register[12].
ejtag_tms	Input		—	**EJTAG Test Mode Select** Requires an external pull-up. The ejtag_tms is sampled on the rising edge of jtag_tck.
Debug Signals				
debug_cpu_dma_n	I/O	Z	Low	**Debug CPU versus DMA Negated** De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU. Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA. Alternate function: modebit[6].
debug_cpu_ack_n	I/O	Z	Low	**Debug CPU Acknowledge Negated** Indicates either a data acknowledge to the CPU or DMA. Alternate function: modebit[4].
debug_cpu_ads_n	I/O	Z	Low	**Debug CPU Address/Data Strobe Negated** Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address. Alternate function: modebit[5].
debug_cpu_i_d_n	I/O	Z	Low	**Debug CPU Instruction versus Data Negated** Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction. De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction. Alternate function: modebit[3].

Table 1 Pin Descriptions (Part 6 of 6)

Logic Diagram — RC32332



pci_host_mode Settings

During cold reset initialization, the RC32332's PCI interface can be set to the Satellite or Host mode settings. When set to the Host mode, the CPU must configure the RC32332's PCI configuration registers, including the read-only registers. If the RC32332's PCI is in the PCI-boot mode Satellite mode, read-only configuration registers are loaded by the serial EEPROM.

Pin	Reset Boot Mode	Description	Value	Mode Settings
mem_addr[20]	PCI host mode	PCI is in satellite mode	1	PCI_satellite
		PCI is in host mode (typical system)	0	PCI_host

Table 4 RC32332 pci_host_mode Initialization Settings

Clock Parameters — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V_{cc} Core = +3.3V±5%; V_{cc} I/O = +3.3V±5%

2.5V version: V_{cc} Core = +2.5V±5%; V_{cc} I/O = +3.3V±5%

Parameter	Symbol	Test Conditions	RC32332 100MHz		RC32332 133MHz		RC32332 150MHz		Units
			Min	Max	Min	Max	Min	Max	
cpu_masterclock HIGH	t_{MCHIGH}	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock LOW	t_{MCLOW}	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock period[1] - 3.3V ver.	t_{MCP}	—	20	66.6	15	66.6	13.33	66.6	ns
cpu_masterclock period[1] - 2.5V ver.	t_{MCP}	—	20	40.0	15	40.0	13.33	40.0	ns
cpu_masterclock Rise & Fall Time[2]	t_{MCRise}, t_{MCFall}	—	—	3	—	3	—	3	ns
cpu_masterclock Jitter	t_{JITTER}	—	—	± 250	—	± 250	—	± 200	ps
pci_clk Rise & Fall Time	t_{PCRise}, t_{PCFall}	PCI 2.2	—	1.6	—	1.6	—	1.6	ns
pci_clk Period[1]	t_{PCP}		20	—	20	—	20	—	ns
jtag_tck Rise & Fall Time	t_{JCRise}, t_{JCFall}	—	—	5	—	5	—	5	ns
ejtag_dck period	t_{DCK}, t_{11}		10	—	10	—	10	—	ns
jtag_tck clock period	t_{TCK}, t_3		100	—	100	—	100	—	ns
ejtag_dclk High, Low Time	$t_{DCK\ High}$, t_9 $t_{DCK\ Low}$, t_{10}		4	—	4	—	4	—	ns
ejtag_dclk Rise, Fall Time	$t_{DCK\ Rise}$, t_9 $t_{DCK\ Fall}$, t_{10}		—	1	—	1	—	1	ns
output_clk[3]	t_{DO}21		N/A	N/A	N/A	N/A	N/A	N/A	—
cpu_coldreset_n Asserted during power-up		power-on sequence	120	—	120	—	120	—	ms
cpu_coldreset_n Rise Time	t_{CRRise}		—	5	—	5	—	5	ns

Table 5 Clock Parameters - RC32332

1. cpu_masterclock frequency should never be below pci_clk frequency if PCI interface is used.

2. Rise and Fall times are measured between 10% and 90%.

3. Output_clk should not be used in a system. Only the cpu_masterclock or its derivative must be used to drive all the subsystems with designs based on the RC32334/RC32332. Refer to the RC32334/RC32332 Device Errata for more information.

AC Timing Characteristics — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V_{cc} Core = +3.3V±5%; V_{cc} I/O = +3.3V±5%

2.5V version: V_{cc} Core = +2.5V±5%; V_{cc} I/O = +3.3V±5%

Signal	Symbol	Reference Edge	100MHz[1]		133MHz[1]		150MHz[1]		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
Local System Interface										
mem_data[31:0] (data phase)	Tsu2	cpu_masterclk rising	6	—	5	—	4.8	—	ns	Chapter 9, Figures 9.2 and 9.3
mem_data[31:0] (data phase)	Thld2	cpu_masterclk rising	1.5	—	1.5	—	1.5	—	ns	
cpu_dt_r_n	Tdo3	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_data[31:0]	Tdo4	cpu_masterclk rising	—	12	—	10	—	9.3	ns	
mem_data[31:0] output hold time	Tdoh1	cpu_masterclk rising	1	—	1	—	1	—	ns	
mem_data[31:0] (tristate disable time)	Tdz	cpu_masterclk rising	—	12[2]	—	10[2]	—	9.3[2]	ns	Chapter 10, Figures 10.6 through 10.8
mem_data[31:0] (tristate to data time)	Tzd	cpu_masterclk rising	—	12[2]	—	10[2]	—	9.3[2]	ns	
mem_wait_n	Tsu6	cpu_masterclk rising	9	—	7	—	6	—	ns	
mem_wait_n	Thld8	cpu_masterclk rising	1	—	1	—	1	—	ns	
mem_addr[22:2]	Tdo5	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_cs_n[5:0]	Tdo6	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_oe_n, mem_245_oe_n	Tdo7	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_we_n[3:0]	Tdo7a	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_245_dt_r_n	Tdo8	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_addr[25:2] mem_cs_n[5:0] mem_oe_n, mem_we_n[3:0], mem_245_dt_r_n, mem_245_oe_n	Tdoh3	cpu_masterclk rising	1.5	—	1.5	—	1.5	—	ns	
PCI for 3.3V Device[3]										
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n	Tsu	pci_clk rising	3	—	3	—	3	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_gnt_n[0]	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n[4]	Thld	pci_clk rising	0	—	0	—	0	—	ns	

Table 6 AC Timing Characteristics - RC32332 (Part 1 of 4)

Signal	Symbol	Reference Edge	100MHz[1]		133MHz[1]		150MHz[1]		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
pci_req_n[0], pci_gnt_[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
SDRAM Controller										
sdram_245_dt_r_n	Tdo8	cpu_masterclk rising	—	15	—	12	—	10	ns	Chapter 11, Figures 11.4 and 11.5
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0], sdram_cke	Tdo9	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_addr_12	Tdo10	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_245_oe_n	Tdo11	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_245_dt_r_n	Tdoh4	cpu_masterclk rising	1	—	1	—	1	—	ns	
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0] sdram_cke, sdram_addr_12, sdram_245_oe_n	Tdoh4	cpu_masterclk rising	2.5	—	2.5	—	2.5	—	ns	
DMA										
dma_ready_n[0], dma_done_n[0]	Tsu7	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 13, Figure 13.4
dma_ready_n[0], dma_done_n[0]	Thld9	cpu_masterclk rising	1	—	1	—	1	—	ns	
Interrupt Handling										
cpu_int_n[1:0], cpu_nmi_n	Tsu9	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 14, Figure 14.12
cpu_int_n[1:0], cpu_nmi_n	Thld13	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO										
PIO[7:0]	Tsu7	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 15, Figures 15.9 and 15.10
PIO[7:0]	Thld9	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO[7:6], PIO[4:0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
PIO[5]	Tdo19	cpu_masterclk rising	—	15	—	12	—	10	ns	
PIO[7:6], PIO[4:0]	Tdoh7	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO[5]	Tdoh7	cpu_masterclk rising	1	—	1	—	1	—	ns	
UARTs										
uart_rx[0], uart_tx[0]	Tsu7	cpu_masterclk rising	15	—	12	—	10	—	ns	Chapter 17, Figure 17.16
uart_rx[0], uart_tx[0]	Thld9	cpu_masterclk rising	15	—	12	—	10	—	ns	
uart_rx[0], uart_tx[0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
uart_rx[0], uart_tx[0]	Tdoh8	cpu_masterclk rising	1	—	1	—	1	—	ns	

Table 6 AC Timing Characteristics - RC32332 (Part 3 of 4)

Signal	Symbol	Reference Edge	100MHz[1]		133MHz[1]		150MHz[1]		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
Reset										
mem_addr[19:17]	Tsu10	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19, Figures 19.8 and 19.9
mem_addr[19:17]	Thld10	cpu_coldreset_n rising	1	—	1	—	1	—	ns	
mem_addr[22:20]	Tsu22	cpu_masterclk rising	9	—	7	—	6	—	ns	
mem_addr[22:20]	Thld22	cpu_masterclk rising	1	—	1	—	1	—	ns	
Debug Interface										
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Tsu20	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19, Figure 19.9 and Chapter 9, Figure 9.2
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Thld20	cpu_coldreset_n rising	1	—	1	—	1	—	ns	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdo20	cpu_masterclk rising	—	15	—	12	—	10	ns	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdoh20	cpu_masterclk rising	1	—	1	—	1	—	ns	
JTAG Interface										
jtag_tms, jtag_tdi, jtag_trst_n	t_5	jtag_tck rising	10	—	10	—	10	—	ns	See Figure 4 below.
jtag_tms, jtag_tdi, jtag_trst_n	t_6	jtag_tck rising	10	—	10	—	10	—	ns	
jtag_tdo	t_4	jtag_tck falling	—	10	—	10	—	10	ns	
EJTAG Interface										
ejtag_tms, ejtag_debugboot	t_5	jtag_tclk rising	4	—	4	—	4	—	ns	See Figure 4 below.
ejtag_tms, ejtag_debugboot	t_6	jtag_clk rising	2	—	2	—	2	—	ns	
jtag_tdo Output Delay Time	t_{TDODO}, t_4	jtag_tck falling	—	6	—	6	—	6	ns	
jtag_tdi Input Setup Time	t_{TDIS}, t_5	jtag_tck rising	4	—	4	—	4	—	ns	
jtag_tdi Input Hold Time	t_{TDIH}, t_6	jtag_tck rising	2	—	2	—	2	—	ns	
jtag_trst_n Low Time	$t_{TRSTLow}$, t_{12}	—	100	—	100	—	100	—	ns	
jtag_trst_n Removal Time	t_{TRSTR}, t_{13}	jtag_tck rising	3	—	3	—	3	—	ns	
ejtag_tpc Output Delay Time	t_{TPCDO}, t_8	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	
ejtag_pcst Output Delay Time	t_{PCSTDO}, t_7	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	

Table 6 AC Timing Characteristics - RC32332 (Part 4 of 4)

1. At all pipeline frequencies.

2. Guaranteed by design.

3. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2 at 33MHz.

4. pci_rst_n is tested per PCI 2.2 as an asynchronous signal.

Standard EJTAG Timing — RC32332

Figure 4 represents the timing diagram for the EJTAG interface signals.

The standard JTAG connector is a 10-pin connector providing 5 signals and 5 ground pins. For Standard EJTAG, a 24-pin connector has been chosen providing 12 signals and 12 ground pins. This guarantees elimination of noise problems by incorporating signal-ground type arrangement. Refer to the RC32334/RC32332 User Reference Manual for connector pinout and mechanical specifications.

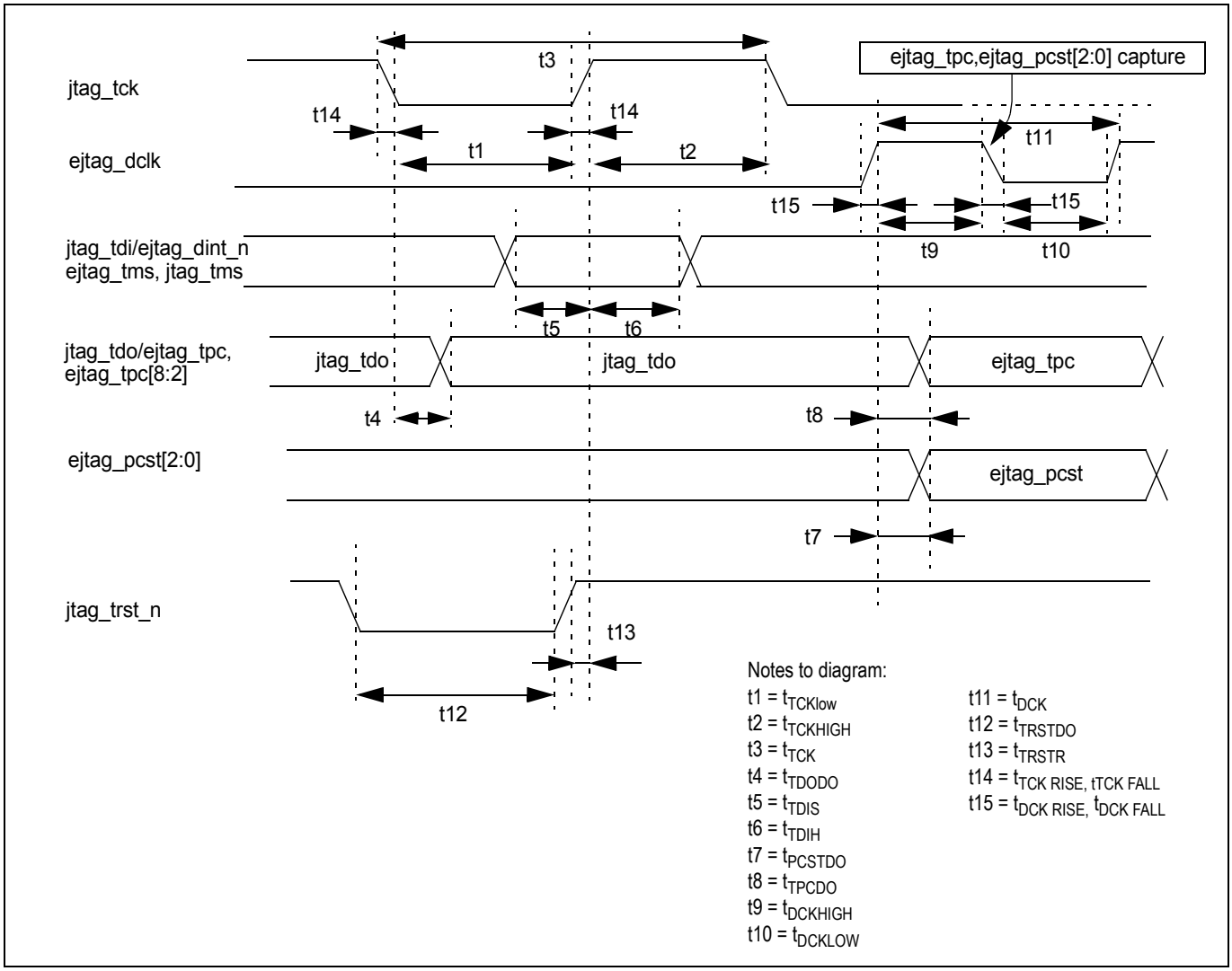
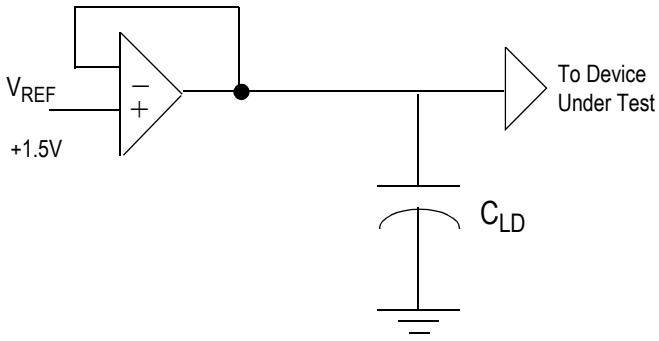


Figure 4 Standard EJTAG Timing

Output Loading for AC Testing



Signal	CId
All High Drive Signals	50 pF
All Low Drive Signals	25 pF

Figure 5 Output Loading for AC Testing

Note: PCI pins have been correlated to PCI 2.2.

Recommended Operation Temperature and Supply Voltage

3.3V Device

Grade	Ambient Temperature	Gnd	$V_{cc}IO$	$V_{cc}Core$	$V_{cc}P$
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C Ambient	0V	3.3V±5%	3.3V±5%	3.3V±5%

Table 7 Temperature and Voltage — 3.3V Device

2.5V Device

Grade	Ambient Temperature	Gnd	$V_{cc}IO$	$V_{cc}Core$	$V_{cc}P$
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	2.5V±5%	2.5V±5%
Industrial	-40°C to +85°C Ambient	0V	3.3V±5%	2.5V±5%	2.5V±5%

Table 8 Temperature and Voltage — 2.5V Device

DC Electrical Characteristics — RC32332

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V_{cc} Core = +3.3V±5%; V_{cc} I/O = +3.3V±5%

2.5V version: V_{cc} Core = +2.5V±5%; V_{cc} I/O = +3.3V±5%

	Parameter	RC32332[1]		Pin Numbers	Conditions
		Minimum	Maximum		
Input Pads	V_{IL}	—	0.8V	52, 64, 95, 160, 161, 164, 166-169, 176, 191	—
	V_{IH}	2.0V	—		—
LOW Drive Output Pads	V_{OL}	—	0.4V	41-45, 48, 170, 171, 174, 175, 177-180, 185-190, 195-200, 207, 208	$\|I_{OUT}\|$ = 6mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 8mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
HIGH Drive Output Pads	V_{OL}	—	0.4V	1- 5, 8, 13-15, 18-25, 28-35, 38-40, 49-51, 53- 57, 60, 61, 63, 65-67,70-76, 79, 80, 83-87, 90-94, 153, 154, 156, 158, 165, 194, 201, 204, 205, 206	$\|I_{OUT}\|$ = 7mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 16mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
PCI Drive Input Pads	V_{IL}	—	—	123, 155, 157, 159	Per PCI 2.2
	V_{IH}	—	—		
PCI Drive Output Pads	V_{OL}	—	—	96, 97, 100-109, 112-119, 122, 124-129, 132-139, 142-149, 152	Per PCI 2.2
	V_{OH}	—	—		
	V_{IL}	—	—		
	V_{IH}	—	—		
All Pads	C_{IN}	—	10pF	All input pads except 155 and 156	—
	C_{IN}[2]	5pf	12pF	155	Per PCI 2.2
	C_{IN}[3]		8pF	156	Per PCI 2.2
	C_{OUT}	—	10pF	All output pads	—
	I/O_{LEAK}	—	10µA	All non-internal pull-up pins	Input/Output Leakage
	I/O_{LEAK}	—	50µA	All internal pull-up pins	Input/Output Leakage

Table 9 DC Electrical Characteristics - RC32332

1. At all pipeline frequencies.
2. Applies only to pad 155.
3. Applies only to pad 156.

Capacitive Load Deration — RC32332

Refer to the IDT document 79RC32332 IBIS Model located on the company's web site.

Power Consumption

3.3V Device

Note: This table is based on a 2:1 pipeline-to-bus clock ratio.

Parameter		100MHz		133MHz		150MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I_{CC}	Normal mode	360	480	480	630	550	700	mA	C_L = (See Figure 5, Output Loading for AC Testing) T_a = 25°C V_{cc} Core = 3.46V (for max. values) V_{cc} I/O = 3.46V (for max. values) V_{cc} Core = 3.3V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	250	370	330	480	390	540	mA	
Power Dissipation	Normal mode	1.2	1.7	1.5	2.2	1.7	2.4	W	
	Standby mode[1]	0.83	1.3	1.1	1.7	1.3	1.9	W	

Table 10 Power Consumption — 3.3V Device

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

2.5V Device

Note: This table is based on a 2:1 pipeline-to-bus clock ratio.

Parameter		100MHz		133MHz		150MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I_{CC} I/O	Normal mode	24	81	32	93	35	104	mA	C_L = (See Figure 5, Output Loading for AC Testing) T_a = 25°C V_{cc} Core = 2.625V (for max. values) V_{cc} I/O = 3.46V (for max. values) V_{cc} Core = 2.5V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	2	81	2	93	2	104	mA	
I_{CC} core	Normal mode	232	301	298	392	333	438	mA	
	Standby mode[1]	120	269	151	319	168	345	mA	
Power Dissipation	Normal mode	0.66	1.07	0.85	1.35	0.95	1.51	W	
	Standby mode[1]	0.31	0.94	0.38	1.10	0.43	1.21	W	

Table 11 Power Consumption — 2.5V Device

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

Power Ramp-up

3.3V Device

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

2.5V Device

The 2.5V core supply (and 2.5V V_{cc}P supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

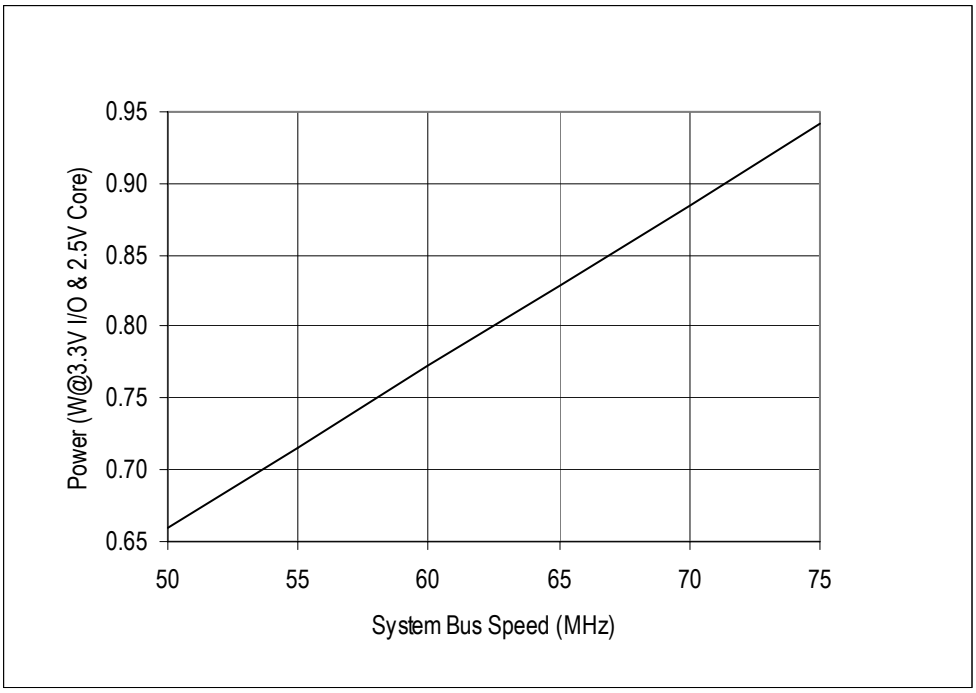


Figure 8 Typical Power Usage — RC32T332 Device

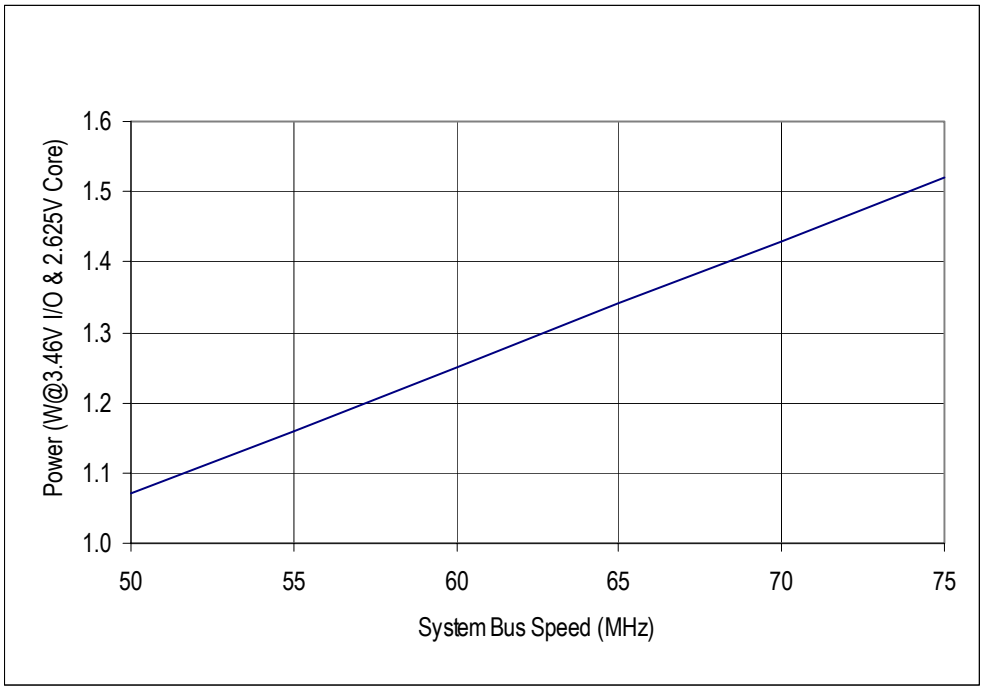


Figure 9 Maximum Power Usage — RC32T332 Device

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{cc} Core 3.3V Device	Supply Voltage	-0.3	4.0	V
V_{cc} Core 2.5V Device	Supply Voltage	-0.3	3.0	V
V_{CC} I/O	I/O Supply Voltage	-0.3	4.0	V
Vi 3.3V Device	Input Voltage	-0.3	5.5	V
Vi 2.5V Device	Input Voltage	-0.3	V_{CC}I/O+0.3	V
Vimin	Input Voltage - undershoot[2]	-0.6	—	V
Tstg	Storage Temperature	-40	125	degrees C

Table 12 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 7. Absolute maximum ratings are stress ratings only, and functional operation is not guaranteed beyond recommended operating voltages and temperatures. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. All PCI pads are fully compatible with PCI Specification version 2.2.

Package Pin-out — 208-PQFP for RC32332

The following table lists the pin numbers and signal names for the RC32332. Signal names ending with an _n are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	sdram_245_oe_n		53	mem_data[12]		105	pci_ad[7]		157	pci_req_n[2]	1
2	sdram_we_n		54	mem_data[19]		106	pci_cbe_n[0]		158	pci_gnt_n[2]	1
3	sdram_cas_n		55	mem_data[13]		107	pci_ad[8]		159	pci_rst_n	
4	sdram_bemask_n[0]		56	mem_data[18]		108	pci_ad[9]		160	cpu_int_n[0]	
5	sdram_bemask_n[1]		57	mem_data[14]		109	pci_ad[10]		161	cpu_int_n[1]	
6	V_{ss}		58	V_{ss}		110	V_{ss}		162	V_{ss}	
7	V_{cc} I/O		59	V_{cc} I/O		111	V_{cc} I/O		163	V_{cc} I/O	
8	sdram_cs_n[0]		60	mem_data[17]		112	pci_ad[11]		164	jtag_tdi	
9	sdram_cs_n[1]		61	mem_data[16]		113	pci_ad[12]		165	jtag_tdo	
10	sdram_ras_n		62	V_{cc} core		114	pci_ad[13]		166	jtag_tms	
11	sdram_s_n[0]		63	mem_data[15]		115	pci_ad[14]		167	ejtag_tms	
12	sdram_s_n[1]		64	cpu_masterclk		116	pci_ad[15]		168	jtag_tck	
13	mem_addr[2]	1	65	mem_data[31]		117	pci_cbe_n[1]		169	jtag_trst_n	
14	mem_addr[3]	1	66	mem_data[0]		118	pci_par		170	ejtag_pcst[0]	1
15	mem_addr[4]	1	67	mem_data[30]		119	pci_serr_n		171	ejtag_pcst[1]	1
16	V_{ss}		68	V_{ss}		120	V_{ss}		172	V_{ss}	
17	V_{cc} I/O		69	V_{cc} I/O		121	V_{cc} I/O		173	V_{cc} I/O	
18	mem_addr[5]	1	70	mem_data[1]		122	pci_perr_n		174	ejtag_pcst[2]	1
19	mem_addr[6]	1	71	mem_data[29]		123	pci_lock_n		175	ejtag_dclk	

Table 13 RC32332 208-pin QFP Package Pin-Out (Part 1 of 2)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
20	mem_addr[7]	1	72	mem_data[2]		124	pci_stop_n		176	ejtag_debugboot	
21	mem_addr[8]	1	73	mem_data[28]		125	pci_devsel_n		177	debug_cpu_i_d_n	1
22	mem_addr[9]	1	74	mem_data[3]		126	pci_trdy_n		178	debug_cpu_ads_n	1
23	mem_addr[10]	1	75	mem_data[27]		127	pci_irdy_n		179	debug_cpu_ack_n	1
24	mem_addr[11]	1	76	mem_data[4]		128	pci_frame_n		180	debug_cpu_dma_n	1
25	output_clk		77	V_{cc}p		129	pci_cbe_n[2]		181	V_{cc} I/O	
26	V_{ss}		78	V_{ss}p		130	V_{ss}		182	V_{ss}	
27	V_{cc} core		79	mem_data[26]		131	V_{cc} core		183	V_{cc} core	
28	mem_addr_12		80	mem_data[5]		132	pci_ad[16]		184	V_{cc} I/O	
29	sdram_addr_12		81	V_{ss}		133	pci_ad[17]		185	spi_ss_n	1
30	sdram_cke		82	V_{cc} core		134	pci_ad[18]		186	spi_sck	2
31	sdram_cs_n[2]		83	cpu_dt_r_n	2	135	pci_ad[19]		187	spi_miso	2
32	sdram_cs_n[3]		84	mem_data[25]		136	pci_ad[20]		188	spi_mosi	2
33	sdram_bemask_n[2]		85	mem_data[6]		137	pci_ad[21]		189	dma_ready_n[0]	2
34	sdram_bemask_n[3]		86	mem_data[24]		138	pci_ad[22]		190	mem_245_oe_n	
35	mem_addr[13]		87	mem_data[7]		139	pci_ad[23]		191	mem_wait_n	2
36	V_{ss}		88	V_{ss}		140	V_{ss}		192	V_{ss}	
37	V_{cc} I/O		89	V_{cc} I/O		141	V_{cc} I/O		193	V_{cc} I/O	
38	mem_addr[14]		90	mem_data[23]		142	pci_cbe_n[3]		194	mem_oe_n	
39	mem_addr[15]	1	91	mem_data[8]		143	pci_ad[24]		195	mem_cs_n[0]	
40	mem_addr[16]	1	92	mem_data[22]		144	pci_ad[25]		196	mem_cs_n[1]	
41	mem_addr[17]	1	93	mem_data[9]		145	pci_ad[26]		197	mem_cs_n[2]	
42	mem_addr[18]	1	94	mem_data[21]		146	pci_ad[27]		198	mem_cs_n[3]	
43	mem_addr[19]	1	95	cpu_nmi_n		147	pci_ad[28]		199	mem_cs_n[4]	
44	mem_addr[20]	1	96	pci_ad[0]		148	pci_ad[29]		200	mem_cs_n[5]	
45	mem_addr[21]	1	97	pci_ad[1]		149	pci_ad[30]		201	mem_we_n[0]	
46	V_{ss}		98	V_{ss}		150	V_{ss}		202	V_{ss}	
47	V_{cc} I/O		99	V_{cc} I/O		151	V_{cc} I/O		203	V_{cc} I/O	
48	mem_addr[22]	1	100	pci_ad[2]		152	pci_ad[31]		204	mem_we_n[1]	
49	mem_data[10]		101	pci_ad[3]		153	pci_req_n[0]		205	mem_we_n[2]	
50	mem_data[11]		102	pci_ad[4]		154	pci_gnt_n[0]		206	mem_we_n[3]	
51	mem_data[20]		103	pci_ad[5]		155	pci_clk		207	uart_tx[0]	1
52	cpu_coldreset_n		104	pci_ad[6]		156	pci_gnt_n[1]	2	208	uart_rx[0]	1

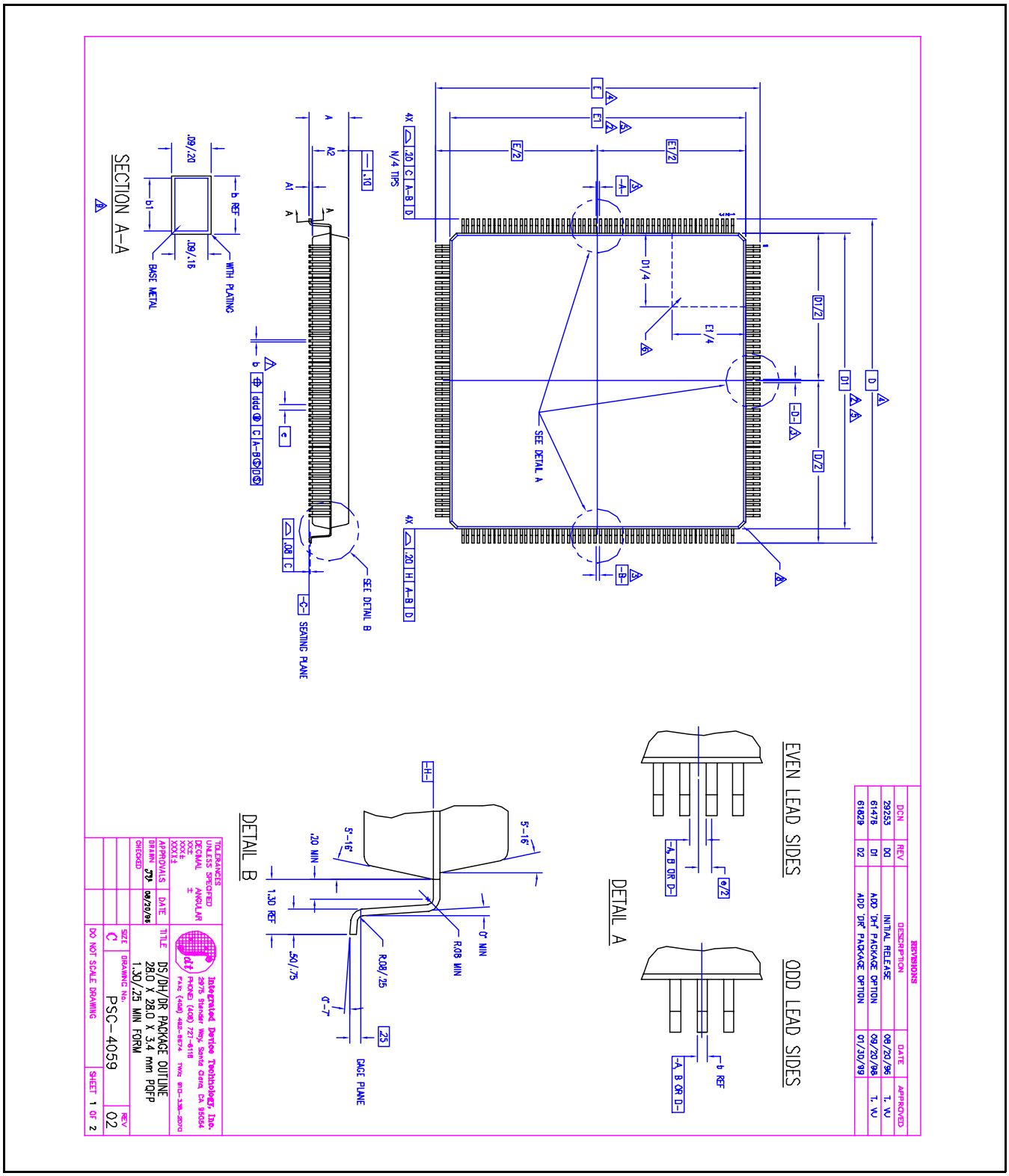
Table 13 RC32332 208-pin QFP Package Pin-Out (Part 2 of 2)

RC32332 Alternate Signal Functions

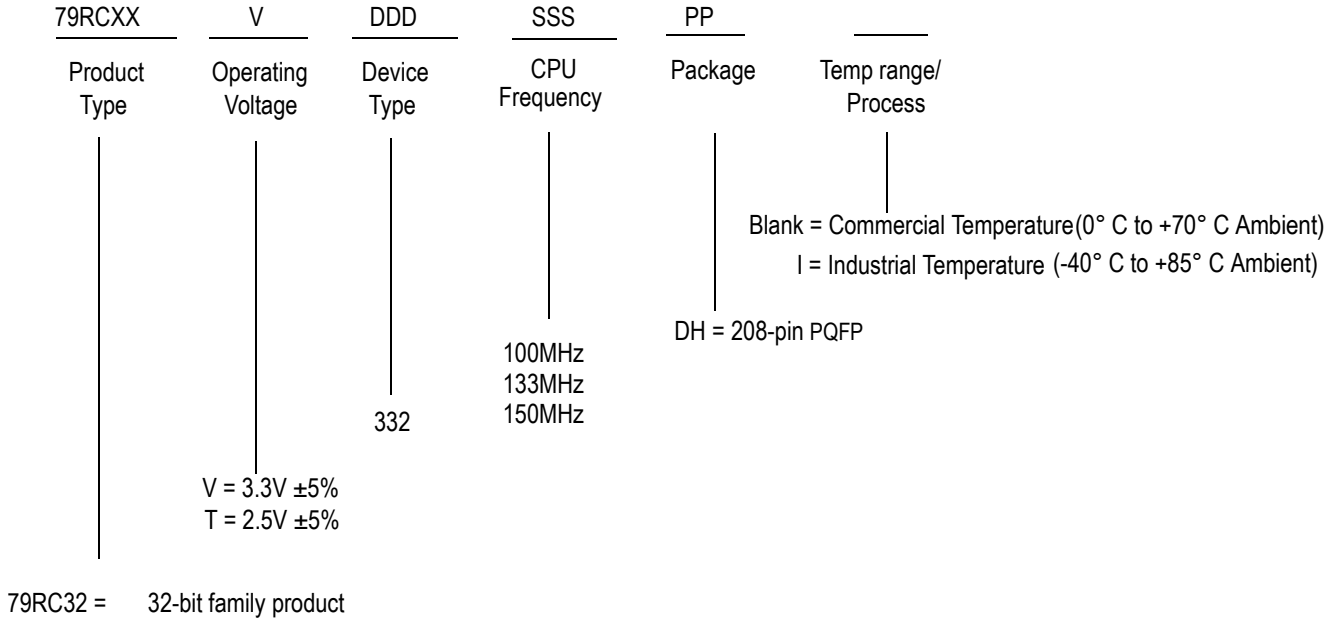
Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2
13	sdram_addr[2]		40	sdram_addr[16]		174	modebit[2]	
14	sdram_addr[3]		41	modebit[7]		177	modebit[3]	
15	sdram_addr[4]		42	modebit[8]		178	modebit[5]	
18	sdram_addr[5]		43	modebit[9]		179	modebit[4]	
19	sdram_addr[6]		44	reset_pci_host_mode		180	modebit[6]	
20	sdram_addr[7]		45	reset_boot_mode[0]		185	PIO[4]	
21	sdram_addr[8]		48	reset_boot_mode[1]		186	PIO[5]	pci_eeprom_sk
22	sdram_addr[9]		83	mem_245_dt_r_n	sdram_245_dt_r_n	187	PIO[3]	pci_eeprom_mdi
23	sdram_addr[10]		156	pci_eeprom_cs (satellite)	PIO[7]	188	PIO[6]	pci_eeprom_mdo
24	sdram_addr[11]		157	pci_idsel (satellite)		189	PIO[0]	dma_done_n[0]
35	sdram_addr[13]		158	pci_inta_n (satellite)		191	sdram_wait_n	mem_wait_n
38	sdram_addr[14]		170	modebit[0]		207	PIO[1]	
39	sdram_addr[15]		171	modebit[1]		208	PIO[2]	

Table 14 RC32332 Alternate Signal Functions

RC32332 Package Drawing — 208-pin PQFP



Ordering Information



Valid Combinations

3.3V Device

79RC32V332 - 100DH, 133DH, 150DH	Commercial
79RC32V332 - 100DHI, 133DHI, 150DHI	Industrial

2.5V Device

79RC32T332 - 100DH, 133DH, 150DH	Commercial
79RC32T332 - 100DHI, 133DHI, 150DHI	Industrial

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