Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, SPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-LQFP-EP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21362bswz-1aa

TABLE OF CONTENTS

REVISION HISTORY

7/13—Revision I to Revision J

Updated Development Tools 9

Added Nominal Value column in Operating Conditions .. 14

Changed Max values in Table 30 in Pulse-Width Modulation Generators 35

Updated Ordering Guide 56

generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

Digital Audio Interface (DAI)

The digital audio interface (DAI) provides the ability to connect various peripherals to any of the DSP's DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU, shown in Figure 1).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI-associated peripherals for a wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes six serial ports, an S/PDIF receiver/transmitter, a DTCP cipher, a precision clock generator (PCG), eight channels of asynchronous sample rate converters, an input data port (IDP), an SPI port, six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2136x core, configurable as either eight channels of I^2S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports

The processor features six synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and a frame sync and they can operate at maximum $f_{PCLK}/4$. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Left-justified sample pair mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the transmitter can be formatted as left-justified, I^2S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

Digital Transmission Content Protection (DTCP)

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) is protected by this copy protection system. This feature is available on the ADSP-21362 and ADSP-21365 processors only. Licensing through DTLA is required for these products. Visit www.dtcp.com for more information.

Memory-to-Memory (MTM)

If the DTCP module is not used, the memory-to-memory DMA module allows internal memory copies for a standard DMA.

Synchronous/Asynchronous Sample Rate Converter (SRC)

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 140 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC is used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

The S/PDIF and SRC are not available on the ADSP-21363 models.

Input Data Port (IDP)

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive

VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the processor's architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference* and the *ADSP-2136x SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

The processor's pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS and TDI).

Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

DAI_Px, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS, $\overline{\text{TRST}}$, TDI, and AD15–0. **Note**: These pins have pull-up resistors.

Table 6. Pin Descriptions

Pin	Type	State During and After Reset	Function
AD15–0	I/O/T (pu)	Three-state with pull-up enabled	**Parallel Port Address/Data.** The ADSP-2136x parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 kΩ internal pull-up resistor. For details about the AD pin operation, refer to the *ADSP-2136x SHARC Processor Hardware Reference*. For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, ADDR23–8; ALE is used in conjunction with an external latch to retain the values of the ADDR23–8. For detailed information on I/O operations and pin multiplexing, refer to the *ADSP-2136x SHARC Processor Hardware Reference*.
$\overline{\text{RD}}$	O (pu)	Three-state, driven high[1]	**Parallel Port Read Enable.** $\overline{\text{RD}}$ is asserted low whenever the processor reads 8-bit or 16-bit data from an external memory device. When AD15–0 are flags, this pin remains deasserted. $\overline{\text{RD}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{WR}}$	O (pu)	Three-state, driven high[1]	**Parallel Port Write Enable.** $\overline{\text{WR}}$ is asserted low whenever the processor writes 8-bit or 16-bit data to an external memory device. When AD15–0 are flags, this pin remains deasserted. $\overline{\text{WR}}$ has a 22.5 kΩ internal pull-up resistor.
ALE	O (pd)	Three-state, driven low[1]	**Parallel Port Address Latch Enable.** ALE is asserted whenever the processor drives a new address on the parallel port address pins. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15–0 are flags, this pin remains deasserted. ALE has a 20 kΩ internal pull-down resistor.
FLAG[0]/$\overline{\text{IRQ0}}$/SPIFLG[0]	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request0/SPI0 Slave Select.**
FLAG[1]/$\overline{\text{IRQ1}}$/SPIFLG[1]	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request1/SPI1 Slave Select.**
FLAG[2]/$\overline{\text{IRQ2}}$/$\overline{\text{SPI}}$ $\overline{\text{FLG[2]}}$	I/O	FLAG[2] INPUT	**FLAG2/Interrupt Request 2/SPI2 Slave Select**.
FLAG[3]/TMREXP/SPIFLG[3]	I/O	FLAG[3] INPUT	**FLAG3/Timer Expired/SPI3 Slave Select.**
DAI_P20–1	I/O/T (pu)	Three-state with programmable pull-up	**Digital Audio Interface Pins**. These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the SRU can be routed to any of these pins. The SRU provides the connection from the serial ports, input data port, precision clock generators and timers, sample rate converters and SPI to the DAI_P20–1 pins. These pins have internal 22.5 kΩ pull-up resistors that are enabled on reset. These pull-ups can be disabled using the DAI_PIN_PULLUP register.

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
BOOT_CFG1–0	I	Input only	**Boot Configuration Select.** This pin is used to select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. For a description of the boot mode, refer to Table 5, Boot Mode Selection.
$\overline{\text{RESETOUT}}$	O	Output only	**Reset Out.** Drives out the core reset signal to an external device.
$\overline{\text{RESET}}$	I/A	Input only	**Processor Reset.** Resets the ADSP-2136x to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Input only[3]	**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the processors.
TMS	I/S (pu)	Three-state with pull-up enabled	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TDI	I/S (pu)	Three-state with pull-up enabled	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 k internal pull-up resistor.
TDO	O	Three-state[4]	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A (pu)	Three-state with pull-up enabled	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2136x. $\overline{\text{TRST}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D) (pu)	Three-state with pull-up enabled	**Emulation Status.** Must be connected to the processor's JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 kΩ internal pull-up resistor.
V_{DDINT}	P		**Core Power Supply.** Supplies the processor's core.
V_{DDEXT}	P		**I/O Power Supply.**
A_{VDD}	P		**Analog Power Supply.** Supplies the processor's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 8.
A_{VSS}	G		**Analog Power Supply Return.**
GND	G		**Power Supply Return.**

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

[1] $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE are three-stated (and not driven) only when $\overline{\text{RESET}}$ is active.
[2] Output only is a three-state driver with its output path always enabled.
[3] Input only is a three-state driver with both output path and pull-up disabled.
[4] Three-state is a three-state driver with pull-up disabled.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[2]	2.4		V
V_{OL}[1]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[2]		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU}[4]	Low Level Input Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
I_{OZH}[5, 6]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU}[6]	Three-State Leakage Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$[7, 8]	Supply Current (Internal)	t_{CCLK} = Min, V_{DDINT} = Nom		800	mA
I_{AVDD}[9]	Supply Current (Analog)	A_{VDD} = Max		10	mA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.2 V		4.7	pF

[1] Applies to output and bidirectional pins: AD15–0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{EMU}$, TDO, and XTAL.
[2] See Output Drive Currents on Page 46 for typical drive current capabilities.
[3] Applies to input pins: $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, and CLKIN.
[4] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[5] Applies to three-stateable pins: FLAG3–0.
[6] Applies to three-stateable pins with 22.5 kΩ pull-ups: AD15–0, DAI_Px, SPICLK, $\overline{EMU}$, $\overline{MISO}$, and $\overline{MOSI}$.
[7] Typical internal current data reflects nominal operating conditions.
[8] See the Engineer-to-Engineer Note *"Estimating Power for the ADSP-21362 SHARC Processors"* (EE-277) for further information.
[9] Characterized, but not tested.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 4 provides details about the package branding for the ADSP-2136x processor. For a complete listing of product availability, see Ordering Guide on Page 56.

Figure 4. Typical Package Brand

Table 7. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See the Engineer-to-Engineer Note *"Estimating Power for the ADSP-21362 SHARC Processors"* (EE-277) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 47.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 8 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. For voltage reference levels, see Figure 39 on Page 46 under Test Conditions.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 5). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 11.

- The product of CLKIN and PLLM must never exceed 1/2 f_{VCO} (max) in Table 11 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 11 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLN)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLN = 1, 2, 4, 8 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

f_{INPUT} = Input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 9. All of the timing specifications for the ADSP-2136x peripherals are defined in relation to t_{PCLK}. Refer to the peripheral specific section for each peripheral's timing information.

Table 9. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, refer to the *ADSP-2136x SHARC Processor Hardware Reference*.

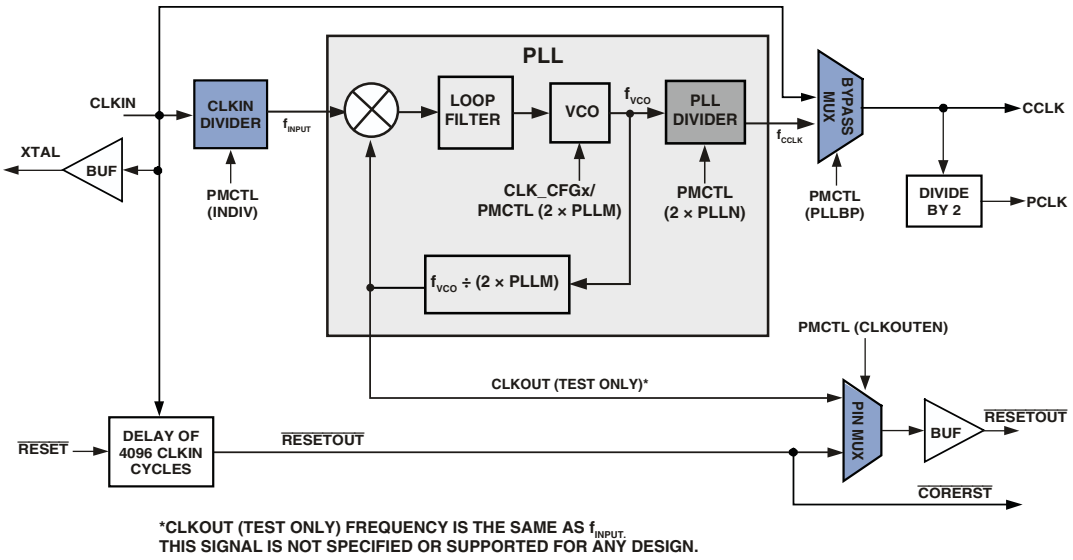


Figure 5. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for processor startup are given in Table 10. Note that during power-up, when the V_{DDINT} power supply comes up after V_{DDEXT}, a leakage current of the order of three-state leakage current pull-up, pull-down, may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the V_{DDINT} rail has powered up.

Table 10. Power-Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds, depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{\text{RESET}}$ to be held low to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{SRST} specification in Table 12. If setup time is not met, 1 additional CLKIN cycle can be added to the core reset time, resulting in 4097 cycles maximum.

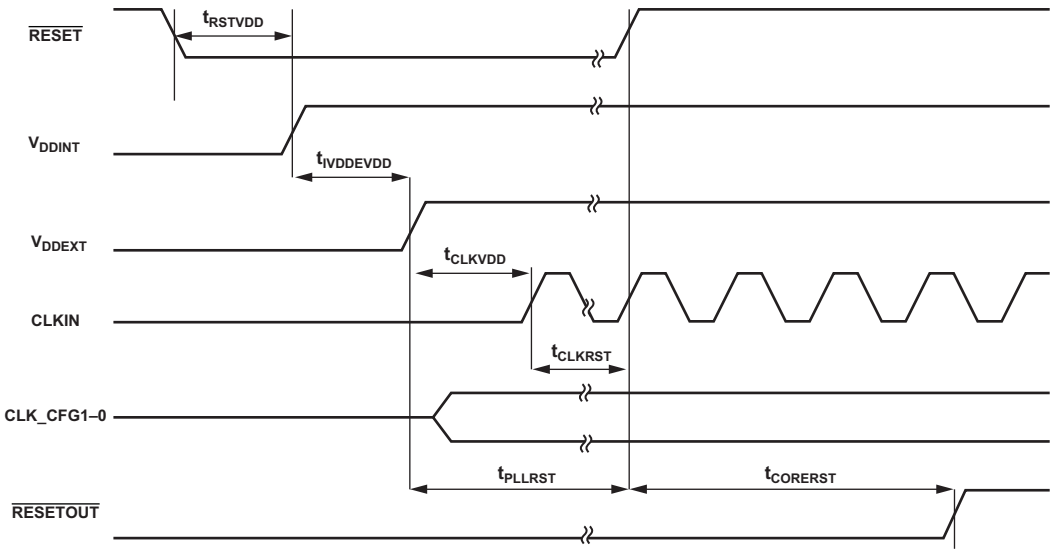


Figure 6. Power-Up Sequencing

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP pin).

Table 14. Core Timer

Parameter		Min	Unit
Switching Characteristic			
t_{WCTIM}	TMREXP Pulse Width	$2 \times t_{PCLK} - 1$	ns

Figure 11. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 15. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

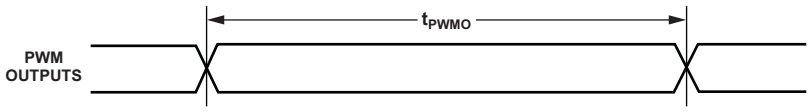


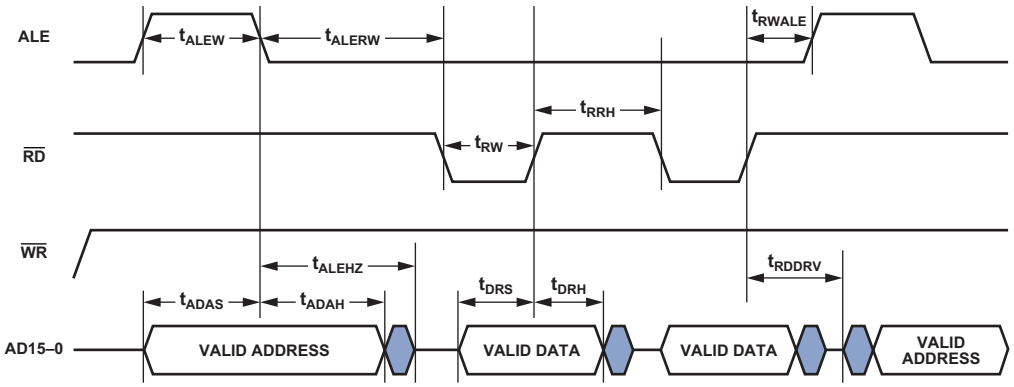
Figure 12. Timer PWM_OUT Timing

Table 21. 16-Bit Memory Read Cycle

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{DRS}	AD15–0 Data Setup Before $\overline{RD}$ High	3.3		4.5		ns
t_{DRH}	AD15–0 Data Hold After $\overline{RD}$ High	0		0		ns
Switching Characteristics						
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$		$2 \times t_{PCLK} - 2.0$		ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$		$t_{PCLK} - 2.5$		ns
t_{ALERW}	ALE Deasserted to Read Asserted	$2 \times t_{PCLK} - 3.8$		$2 \times t_{PCLK} - 3.8$		ns
t_{RRH}[2]	Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge	$H + t_{PCLK} - 1.4$		$H + t_{PCLK} - 1.4$		ns
t_{RWALE}	Read Deasserted to ALE Asserted	$F + H + 0.5$		$F + H + 0.5$		ns
t_{RDDRV}	ALE Address Drive After Read High	$F + H + t_{PCLK} - 2.3$		$F + H + t_{PCLK} - 2.3$		ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$		$t_{PCLK} - 2.3$		ns
t_{ALEHZ1}	ALE Deasserted to Address/Data15–0 in High-Z	t_{PCLK}	$t_{PCLK} + 3.0$	t_{PCLK}	$t_{PCLK} + 3.8$	ns
t_{RW}	$\overline{RD}$ Pulse Width	$D - 2.0$		$D - 2.0$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) $\times t_{PCLK}$
$H = t_{PCLK}$ (if a hold cycle is specified, else $H = 0$)
$F = 7 \times t_{PCLK}$ (if FLASH_MODE is set, else $F = 0$)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY READS, WHEN EMPP ≠ 0, ONLY ONE $\overline{RD}$ PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE $\overline{RD}$ PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 18. Read Cycle for 16-Bit Memory Timing

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync (FS) delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 24. Serial Ports—External Clock

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	2.5			ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5			ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 2$			ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$			ns
Switching Characteristics					
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)		9.5	11	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)	2			ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		9.5	11	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2			ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 25. Serial Ports—Internal Clock

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	7			ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7			ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5			ns
Switching Characteristics					
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		3	3.5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0			ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		8	9.5	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0			ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3	4.0	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0			ns
t_{SCLKIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 2$	$2 \times t_{PCLK} + 2$	$2 \times t_{PCLK} + 2$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

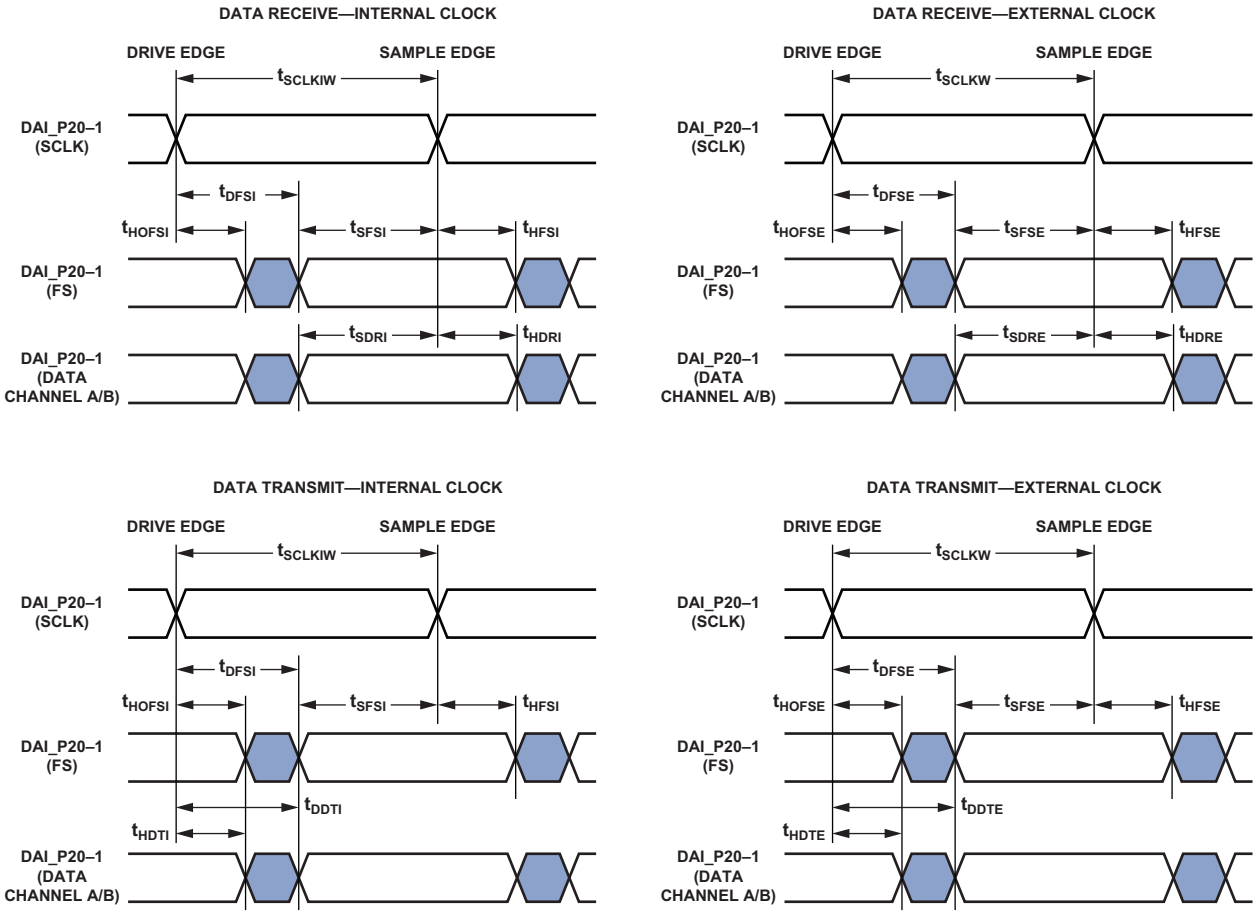


Figure 21. Serial Ports

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I^{2}S, or right justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 29 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

Table 33. S/PDIF Transmitter Right-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{RJD}	FS to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

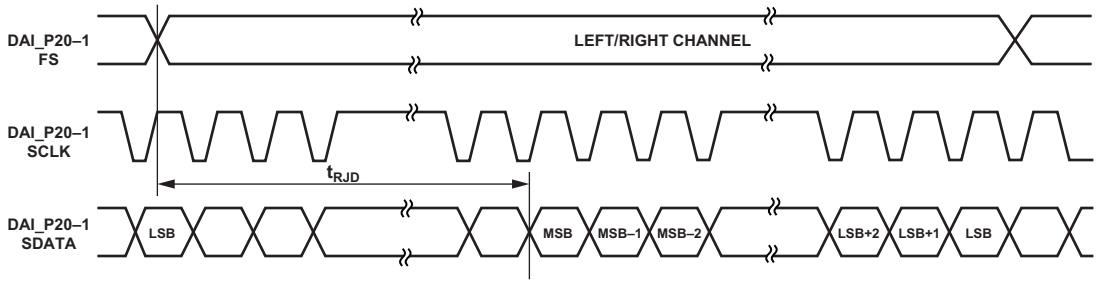


Figure 29. Right-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 36. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 36. S/PDIF Transmitter Input Data Timing

Parameter		K Grade Min	K Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		9.5		ns
$t_{SITXCLK}$	Transmit Clock Period	20		20		ns
$t_{SISCLKW}$	Clock Width	36		36		ns
t_{SISCLK}	Clock Period	80		80		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins.The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

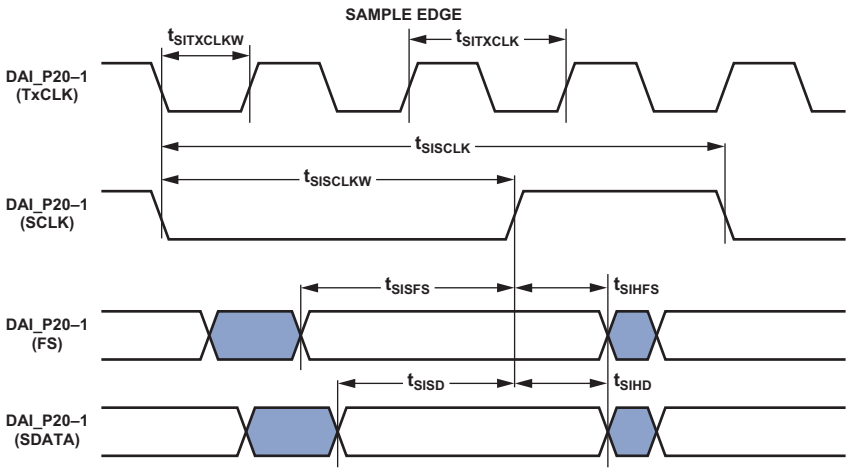


Figure 32. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 37. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Max	Unit
Frequency for TxCLK = 384 × Frame Sync	Oversampling Ratio × Frame Sync <= $1/t_{SITXCLK}$	MHz
Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

SPI Interface—Slave

Table 40. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$			ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$			ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$			ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge				
	CPHASE = 0	$2 \times t_{PCLK}$			ns
	CPHASE = 1	$2 \times t_{PCLK}$			ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$			ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2			ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2			ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$			ns
Switching Characteristics					
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	5	5	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	8	9	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	5	5.5	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	8.6	10	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	11.0	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$			ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, "Serial Peripheral Interface Port" chapter.

JTAG Test Access Port and Emulation

Table 41. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = ADDR15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, MISO, MOSI, SPICLK, DAI_Px, and FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, ADDR15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$, and ALE.

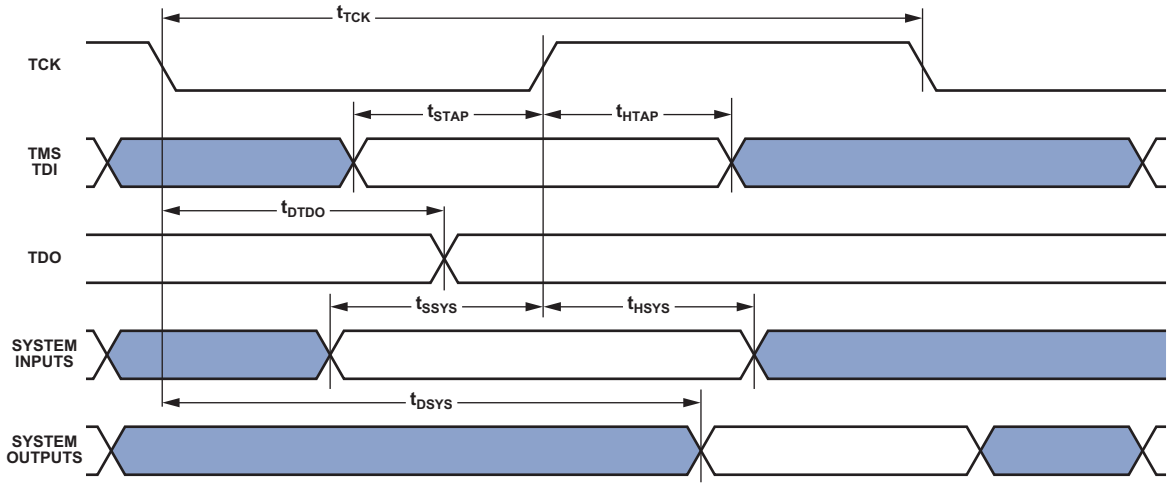


Figure 36. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 37 shows typical I-V characteristics for the output drivers of the processor. The curves represent the current drive capability of the output drivers as a function of output voltage.

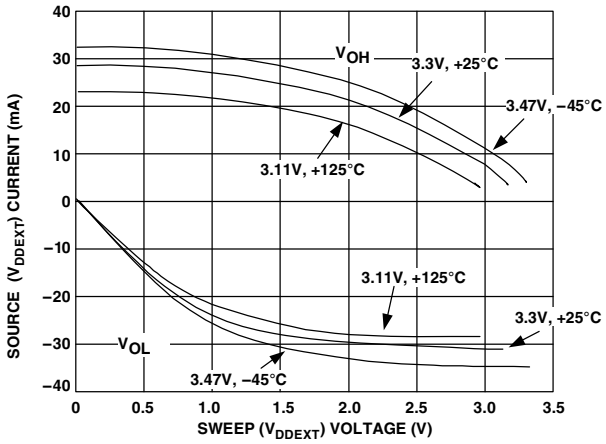


Figure 37. ADSP-2136x Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 12 on Page 20 through Table 41 on Page 45. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 38.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 39. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

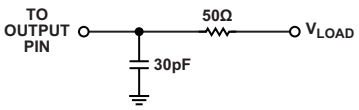


Figure 38. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

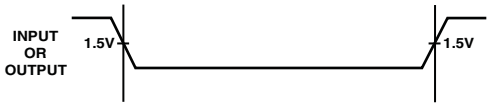


Figure 39. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 38). Figure 42 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 40, Figure 41, and Figure 42 may not be linear outside the ranges shown for Typical Output Delay versus Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) versus Load Capacitance.

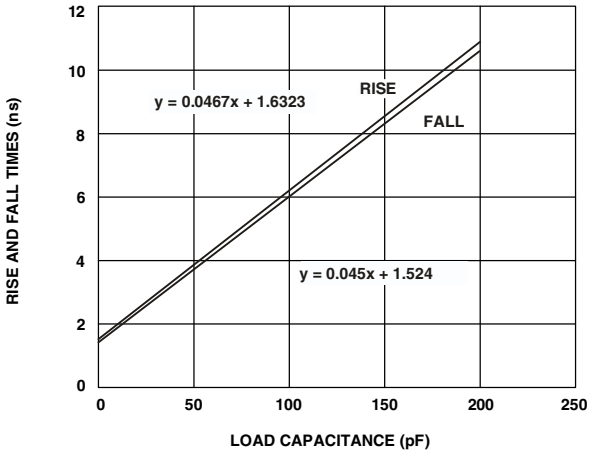


Figure 40. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

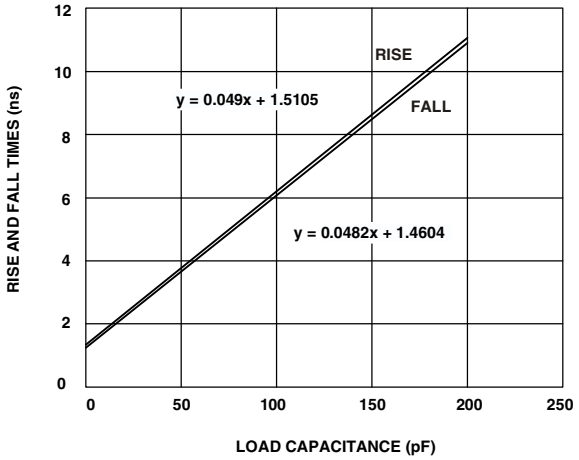


Figure 41. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

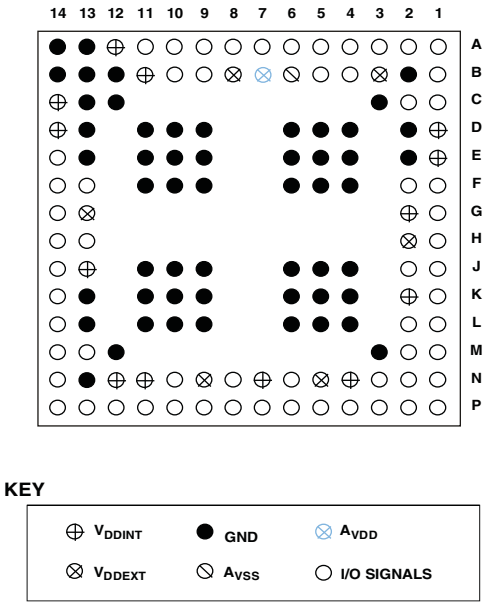


Figure 45. BGA Pin Assignments (Bottom View, Summary)

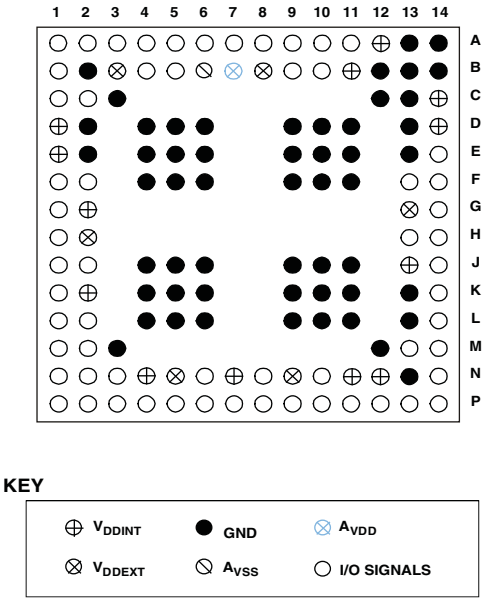


Figure 46. BGA Pin Assignments (Top View, Summary)

AUTOMOTIVE PRODUCTS

Some ADSP-2136x models are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 48. Automotive Products

Model	Notes	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
AD21362WBBCZ1xx	2	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21362WBSWZ1xx	2	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21362WYSWZ2xx	2	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WBBCZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21363WBSWZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WYSWZ2xx		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WBBCZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21364WBSWZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WYSWZ2xx		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ1xxA	2, 3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ1xxF	2, 3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WYSWZ2xxA	2, 3, 4	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WBBCZ1xxA	3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21366WBSWZ1xxA	3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WYSWZ2xxA	3, 4	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 14 for junction temperature (T_J) specification which is the only temperature specification.

[2] License from DTLA required for these products.

[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/sharc.

[4] License from Dolby Laboratories, Inc., and Digital Theater Systems (DTS) required for these products.