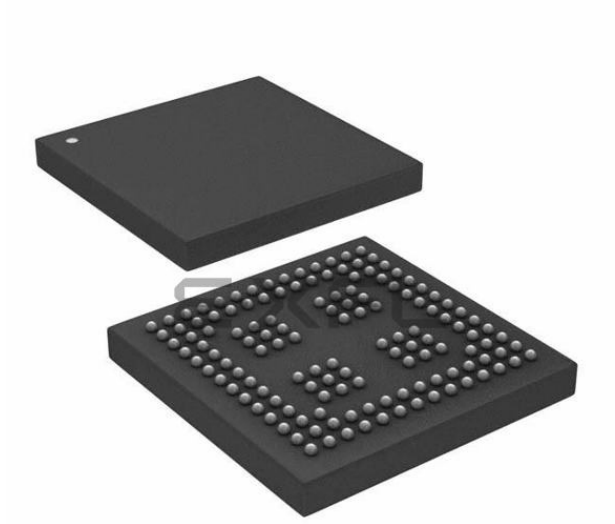

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, SPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	136-LFBGA, CSPBGA
Supplier Device Package	136-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21363bbc-1aa

audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of two units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A and B, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Peripheral Timers

The following three general-purpose timers can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

Each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

I/O PROCESSOR FEATURES

The processor's I/O provides many channels of DMA and controls the extensive set of peripherals described in the previous sections.

DMA Controller

The processor's on-chip DMA controllers allow data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the parallel port (PP). See Table 4.

Table 4. DMA Channels

Peripheral	ADSP-2136x
SPORTs	12
IDP/PDAP	8
SPI	2
MTM/DTCP	2
Parallel Port	1
Total DMA Channels	25

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the processor boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins in Table 5. Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Table 5. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port Boot via EPROM
11	No booting occurs. Processor executes from internal ROM after reset.

Phase-Locked Loop

The processors use an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK_CFG1–0 pins are used to select ratios of 32:1, 16:1, and 6:1. After booting, numerous other ratios can be selected via software control.

The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 1, 2, 4, and 8.

Power Supplies

The processor has a separate power supply connection for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2 V requirement for K, B, and Y grade models, and the 1.0 V requirement for Y models. (For information on the temperature ranges offered for this product, see Operating Conditions on Page 14, Package Information on Page 16, and Ordering Guide on Page 56.) The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 3. (A recommended ferrite chip is the muRata BLM18AG102SN1D.) To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 3 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the processor's architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference* and the *ADSP-2136x SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

The processor's pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS and TDI).

Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

DAI_Px, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS, $\overline{\text{TRST}}$, TDI, and AD15–0. **Note**: These pins have pull-up resistors.

Table 6. Pin Descriptions

Pin	Type	State During and After Reset	Function
AD15–0	I/O/T (pu)	Three-state with pull-up enabled	**Parallel Port Address/Data.** The ADSP-2136x parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 kΩ internal pull-up resistor. For details about the AD pin operation, refer to the *ADSP-2136x SHARC Processor Hardware Reference*. For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, ADDR23–8; ALE is used in conjunction with an external latch to retain the values of the ADDR23–8. For detailed information on I/O operations and pin multiplexing, refer to the *ADSP-2136x SHARC Processor Hardware Reference*.
$\overline{\text{RD}}$	O (pu)	Three-state, driven high[1]	**Parallel Port Read Enable.** $\overline{\text{RD}}$ is asserted low whenever the processor reads 8-bit or 16-bit data from an external memory device. When AD15–0 are flags, this pin remains deasserted. $\overline{\text{RD}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{WR}}$	O (pu)	Three-state, driven high[1]	**Parallel Port Write Enable.** $\overline{\text{WR}}$ is asserted low whenever the processor writes 8-bit or 16-bit data to an external memory device. When AD15–0 are flags, this pin remains deasserted. $\overline{\text{WR}}$ has a 22.5 kΩ internal pull-up resistor.
ALE	O (pd)	Three-state, driven low[1]	**Parallel Port Address Latch Enable.** ALE is asserted whenever the processor drives a new address on the parallel port address pins. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15–0 are flags, this pin remains deasserted. ALE has a 20 kΩ internal pull-down resistor.
FLAG[0]/$\overline{\text{IRQ0}}$/SPIFLG[0]	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request0/SPI0 Slave Select.**
FLAG[1]/$\overline{\text{IRQ1}}$/SPIFLG[1]	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request1/SPI1 Slave Select.**
FLAG[2]/$\overline{\text{IRQ2}}$/$\overline{\text{SPI}}$ $\overline{\text{FLG[2]}}$	I/O	FLAG[2] INPUT	**FLAG2/Interrupt Request 2/SPI2 Slave Select**.
FLAG[3]/TMREXP/SPIFLG[3]	I/O	FLAG[3] INPUT	**FLAG3/Timer Expired/SPI3 Slave Select.**
DAI_P20–1	I/O/T (pu)	Three-state with programmable pull-up	**Digital Audio Interface Pins**. These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the SRU can be routed to any of these pins. The SRU provides the connection from the serial ports, input data port, precision clock generators and timers, sample rate converters and SPI to the DAI_P20–1 pins. These pins have internal 22.5 kΩ pull-up resistors that are enabled on reset. These pull-ups can be disabled using the DAI_PIN_PULLUP register.

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
SPICLK	I/O (pu)	Three-state with pull-up enabled, driven high in SPI-master boot mode	**Serial Peripheral Interface Clock Signal.** Driven by the master, this signal controls the rate at which data is transferred. The master can transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (high). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{SPIDS}}$	I	Input only	**Serial Peripheral Interface Slave Device Select.** An active low signal used to select the processor as an SPI slave device. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode the processor's $\overline{\text{SPIDS}}$ signal can be driven by a slave device to signal to the processor (as SPI master) that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where flag pins are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For processor to processor SPI interaction, any of the master processor's flag pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the SPI slave device.
MOSI	I/O (O/D) (pu)	Three-state with pull-up enabled, driven low in SPI-master boot mode	**SPI Master Out Slave In.** If the ADSP-2136x is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the processor is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has a 22.5 kΩ internal pull-up resistor.
MISO	I/O (O/D) (pu)	Three-state with pull-up enabled	**SPI Master In Slave Out.** If the ADSP-2136x is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the processor is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has a 22.5 kΩ internal pull-up resistor. MISO can be configured as O/D by setting the OPD bit in the SPICTL register. **Note:** *Only one slave is allowed to transmit data at any given time.* To enable broadcast transmission to multiple SPI slaves, the processor's MISO pin can be disabled by setting Bit 5 (DMISO) of the SPICTL register equal to 1.
CLKIN	I	Input only	**Local Clock In.** Used in conjunction with XTAL. CLKIN is the ADSP-2136x clock input. It configures the ADSP-2136x to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. The core is clocked either by the PLL output or this clock input depending on the CLK_CFG1–0 pin settings. CLKIN should not be halted, changed, or operated below the specified frequency.
XTAL	O	Output only[2]	**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
CLK_CFG1–0	I	Input only	**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are: 00 = 6:1 01 = 32:1 10 = 16:1 11 = reserved.

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

SPECIFICATIONS

Specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter	Description	K Grade			B Grade			Y Grade			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{DDINT}	Internal (Core) Supply Voltage	1.14	1.2	1.26	1.14	1.2	1.26	0.95	1.0	1.05	V
A_{VDD}	Analog (PLL) Supply Voltage	1.14	1.2	1.26	1.14	1.2	1.26	0.95	1.0	1.05	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{IH}[1]	High Level Input Voltage @ V_{DDEXT} = Max	2.0		V_{DDEXT} + 0.5	2.0		V_{DDEXT} + 0.5	2.0		V_{DDEXT} + 0.5	V
V_{IL}[1]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5		+0.8	–0.5		+0.8	–0.5		+0.8	V
V_{IH_CLKIN}[2]	High Level Input Voltage @ V_{DDEXT} = Max	1.74		V_{DDEXT} + 0.5	1.74		V_{DDEXT} + 0.5	1.74		V_{DDEXT} + 0.5	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5		+1.19	–0.5		+1.19	–0.5		+1.19	V
T_J[3, 4]	Junction Temperature 136-Ball CSP_BGA	0		+110	–40		+125	–40		+125	°C
T_J[3, 4]	Junction Temperature 144-Lead LQFP_EP	0		+110	–40		+125	–40		+125	°C

[1] Applies to input and bidirectional pins: AD15–0, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, and $\overline{TRST}$.
[2] Applies to input pin CLKIN.
[3] See Thermal Characteristics on Page 47 for information on thermal specifications.
[4] See the Engineer-to-Engineer Note *"Estimating Power for the ADSP-21362 SHARC Processors"* (EE-277) for further information.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[2]	2.4		V
V_{OL}[1]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[2]		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU}[4]	Low Level Input Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
I_{OZH}[5, 6]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU}[6]	Three-State Leakage Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$[7, 8]	Supply Current (Internal)	t_{CCLK} = Min, V_{DDINT} = Nom		800	mA
I_{AVDD}[9]	Supply Current (Analog)	A_{VDD} = Max		10	mA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.2 V		4.7	pF

[1] Applies to output and bidirectional pins: AD15–0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{EMU}$, TDO, and XTAL.
[2] See Output Drive Currents on Page 46 for typical drive current capabilities.
[3] Applies to input pins: $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, and CLKIN.
[4] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[5] Applies to three-stateable pins: FLAG3–0.
[6] Applies to three-stateable pins with 22.5 kΩ pull-ups: AD15–0, DAI_Px, SPICLK, $\overline{EMU}$, $\overline{MISO}$, and $\overline{MOSI}$.
[7] Typical internal current data reflects nominal operating conditions.
[8] See the Engineer-to-Engineer Note *"Estimating Power for the ADSP-21362 SHARC Processors"* (EE-277) for further information.
[9] Characterized, but not tested.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

Clock Input

Table 11. Clock Input

Parameter		200 MHz[1]		333 MHz[2]		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{CK}	CLKIN Period	30[3]	100	18	100	ns
t_{CKL}	CLKIN Width Low	12.5		7.5		ns
t_{CKH}	CLKIN Width High	12.5		7.5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3	ns
t_{CCLK}[4]	CCLK Period	5.0	10	3.0	10	ns
t_{VCO}[5]	VCO Frequency	200	600	200	800	MHz
t_{CKJ}[6, 7]	CLKIN Jitter Tolerance	–250	+250	–250	+250	ps

[1] Applies to all 200 MHz models. See Ordering Guide on Page 56.
[2] Applies to all 333 MHz models. See Ordering Guide on Page 56.
[3] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in the PMCTL register.
[4] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[5] See Figure 5 on Page 17 for VCO diagram.
[6] Actual input jitter should be combined with AC specifications for accurate timing analysis.
[7] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

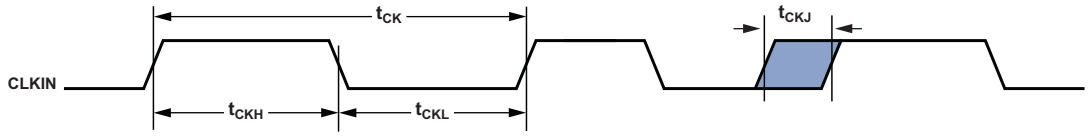


Figure 7. Clock Input

Clock Signals

The processor can use an external clock or a crystal. Refer to the CLKIN pin description in Table 6 on Page 11. The user application program can configure the processor to use its internal clock generator by connecting the necessary components to the CLKIN and XTAL pins. Figure 8 shows the component connections used for a fundamental frequency crystal operating in parallel mode.

Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1. (CCLK:CLKIN achieves a clock speed of 266.72 MHz.) To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

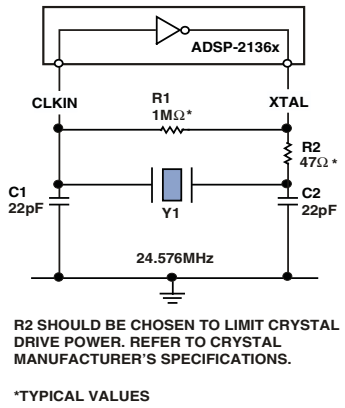


Figure 8. Recommended Circuit for Fundamental Mode Crystal Operation

Timer WDTH_CAP Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specification provided below are valid at the DAI_P20–1 pins.

Table 16. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

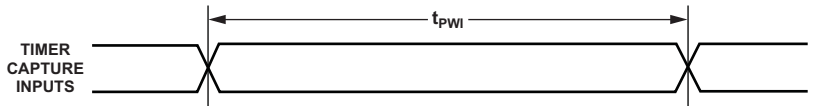


Figure 13. Timer Width Capture Timing

DAI Pin to Pin Direct Routing

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 17. DAI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	10	ns

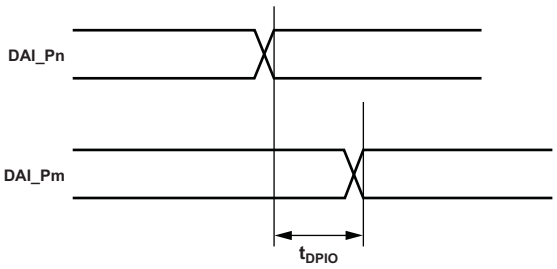


Figure 14. DAI Pin to Pin Direct Routing

Memory Read—Parallel Port

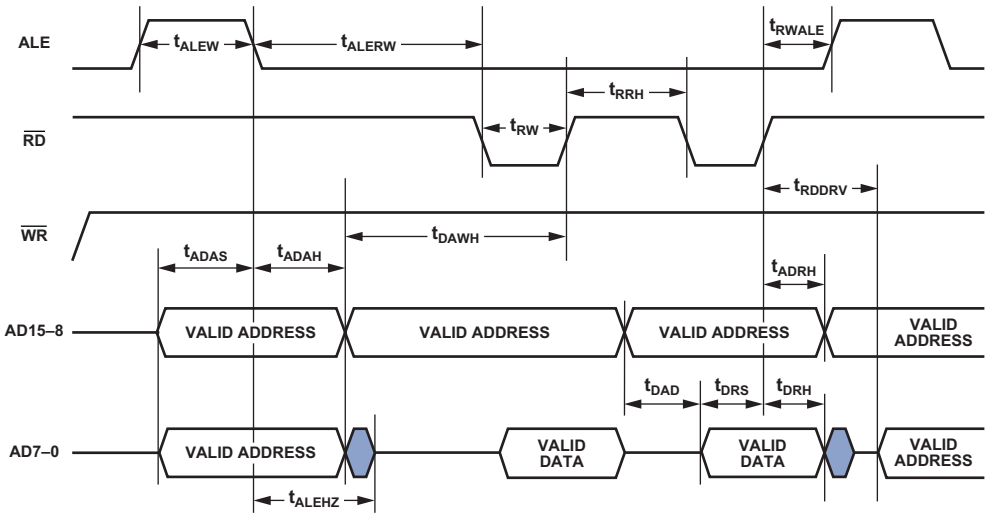
Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the processor is accessing external memory space.

Table 20. 8-Bit Memory Read Cycle

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{DRS}	AD7–0 Data Setup Before $\overline{RD}$ High	3.3		4.5		ns
t_{DRH}	AD7–0 Data Hold After $\overline{RD}$ High	0		0		ns
t_{DAD}	AD15–8 Address to AD7–0 Data Valid		D + t_{PCLK} – 5.0		D + t_{PCLK} – 5.0	ns
Switching Characteristics						
t_{ALEW}	ALE Pulse Width	2 × t_{PCLK} – 2.0		2 × t_{PCLK} – 2.0		ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	t_{PCLK} – 2.5		t_{PCLK} – 2.5		ns
t_{RRH}	Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge	H + t_{PCLK} – 1.4		H + t_{PCLK} – 1.4		ns
t_{ALERW}	ALE Deasserted to Read Asserted	2 × t_{PCLK} – 3.8		2 × t_{PCLK} – 3.8		ns
t_{RWALE}	Read Deasserted to ALE Asserted	F + H + 0.5		F + H + 0.5		ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	t_{PCLK} – 2.3		t_{PCLK} – 2.3		ns
t_{ALEHZ}[1]	ALE Deasserted to AD7–0 Address in High-Z	t_{PCLK}	t_{PCLK} + 3.0	t_{PCLK}	t_{PCLK} + 3.8	ns
t_{RW}	$\overline{RD}$ Pulse Width	D – 2.0		D – 2.0		ns
t_{RDDRV}	AD7–0 ALE Address Drive After Read High	F + H + t_{PCLK} – 2.3		F + H + t_{PCLK} – 2.3		ns
t_{ADRH}	AD15–8 Address Hold After $\overline{RD}$ High	H		H		ns
t_{DAWH}	AD15–8 Address to $\overline{RD}$ High	D + t_{PCLK} – 4.0		D + t_{PCLK} – 4.0		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}
H = t_{PCLK} (if a hold cycle is specified, else H = 0)
F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.



NOTE: MEMORY READS ALWAYS OCCUR IN GROUPS OF FOUR BETWEEN ALE CYCLES. THIS FIGURE SHOWS ONLY TWO MEMORY READS TO PROVIDE THE NECESSARY TIMING INFORMATION.

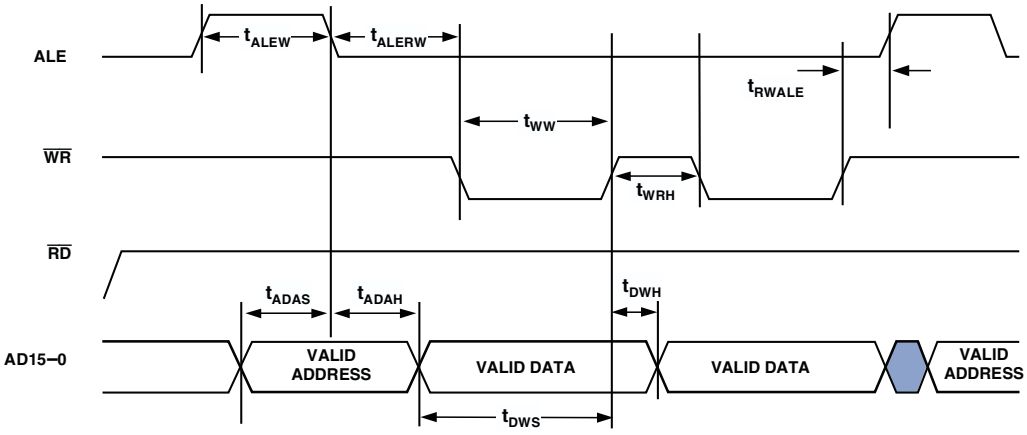
Figure 17. Read Cycle for 8-Bit Memory Timing

Table 23. 16-Bit Memory Write Cycle

Parameter		K and B Grade Min	Y Grade Min	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$	$2 \times t_{PCLK} - 2.0$	ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$	$t_{PCLK} - 2.5$	ns
t_{ALERW}	ALE Deasserted to Write Asserted	$2 \times t_{PCLK} - 3.8$	$2 \times t_{PCLK} - 3.8$	ns
t_{RWALE}	Write Deasserted to ALE Asserted	H + 0.5	H + 0.5	ns
t_{WRH}[2]	Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge	$F + H + t_{PCLK} - 2.3$	$F + H + t_{PCLK} - 2.3$	ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$	$t_{PCLK} - 2.3$	ns
t_{WW}	$\overline{WR}$ Pulse Width	D – F – 2.0	D – F – 2.0	ns
t_{DWS}	AD15–0 Data Setup Before $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns
t_{DWH}	AD15–0 Data Hold After $\overline{WR}$ High	H	H	ns

D = (the value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}.
H = t_{PCLK} (if a hold cycle is specified, else H = 0)
F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0). If FLASH_MODE is set, D must be ≥ 9 × t_{PCLK}.
t_{PCLK} = (peripheral) clock period = 2 × t_{CCLK}

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY WRITES, WHEN EMPP ≠ 0, ONLY ONE $\overline{WR}$ PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE $\overline{WR}$ PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 20. Write Cycle for 16-Bit Memory Timing

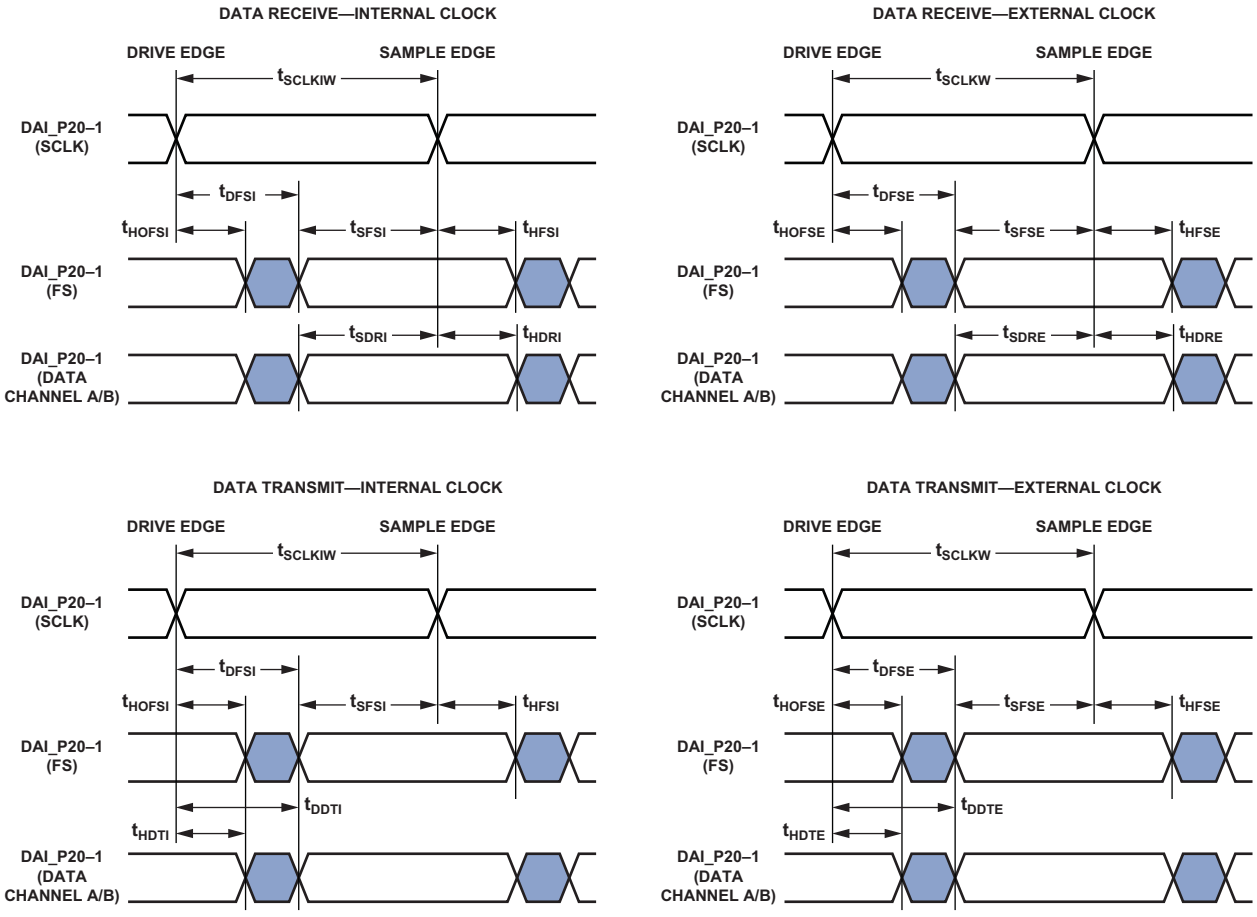


Figure 21. Serial Ports

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 28. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 28. IDP

Parameter		Min	Unit
Timing Requirements			
t_{SISFS}[1]	Frame Sync Setup Before Clock Rising Edge	3	ns
t_{SIHFS}[1]	Frame Sync Hold After Clock Rising Edge	3	ns
t_{SISD}[1]	Data Setup Before Clock Rising Edge	3	ns
t_{SIHD}[1]	Data Hold After Clock Rising Edge	3	ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$	ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$	ns

[1] The data, clock, and frame sync signals can come from any of the DAI pins. Clock and frame sync can also come via the PCGs or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

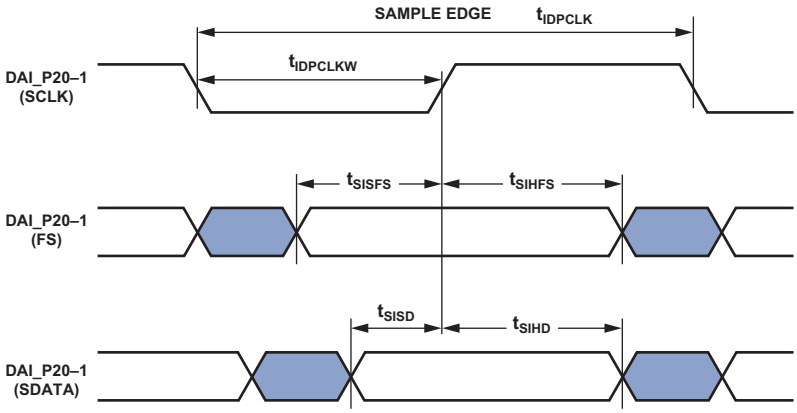


Figure 24. IDP Master Timing

Figure 30 shows the default I²S-justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

Table 34. S/PDIF Transmitter I²S Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{I2SD}	FS to MSB Delay in I²S Mode	1	SCLK

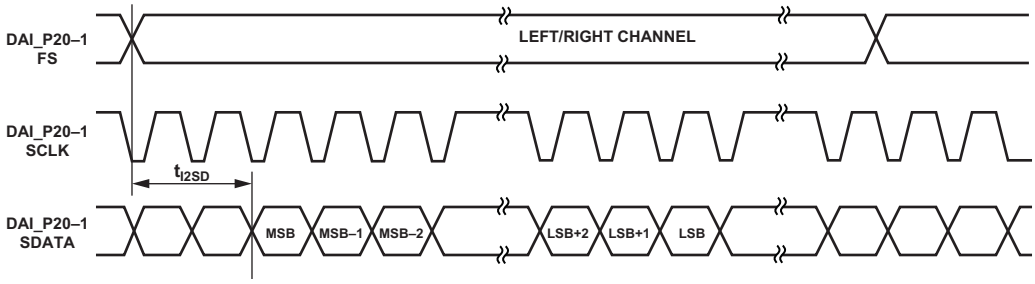


Figure 30. I²S-Justified Mode

Figure 31 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

Table 35. S/PDIF Transmitter Left-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{LJD}	FS to MSB Delay in Left-Justified Mode	0	SCLK

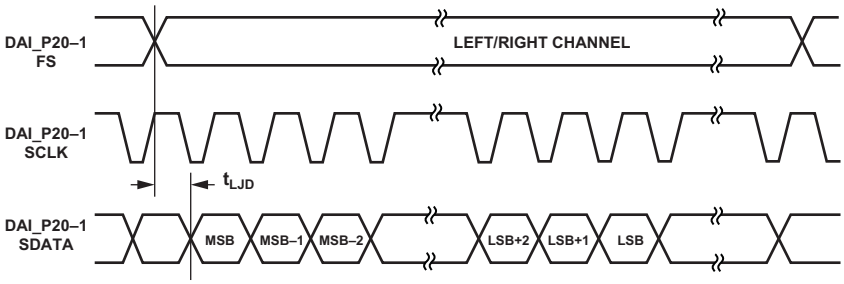


Figure 31. Left-Justified Mode

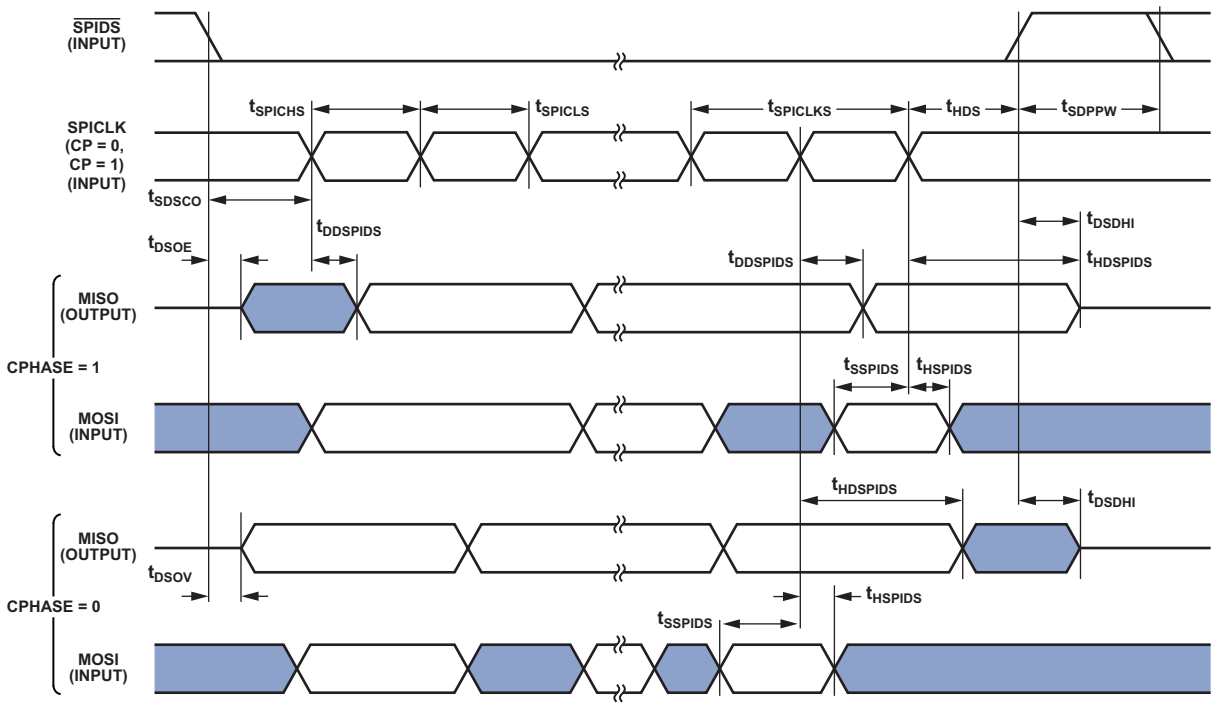


Figure 35. SPI Slave Timing

JTAG Test Access Port and Emulation

Table 41. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = ADDR15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, MISO, MOSI, SPICLK, DAI_Px, and FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, ADDR15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$, and ALE.

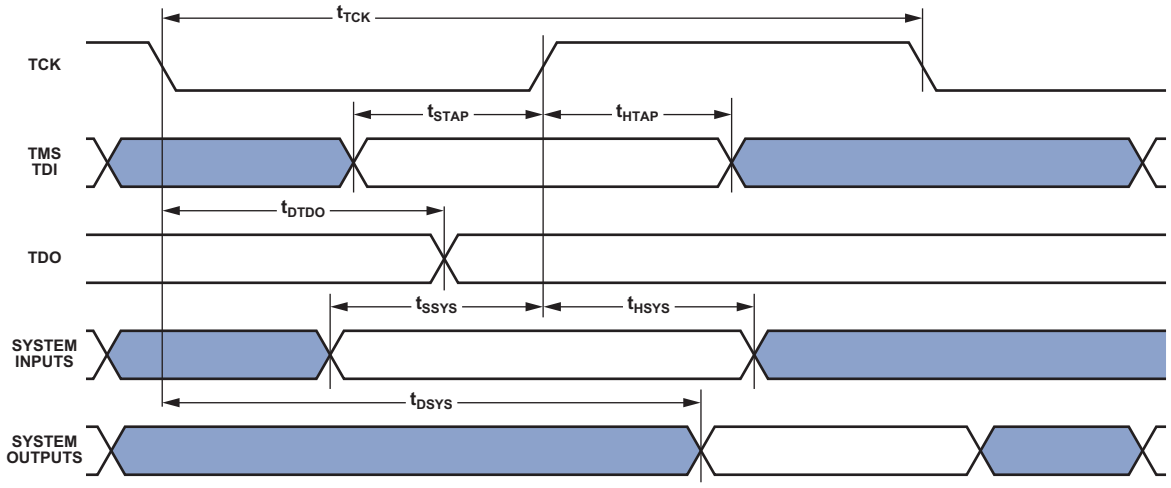


Figure 36. IEEE 1149.1 JTAG Test Access Port

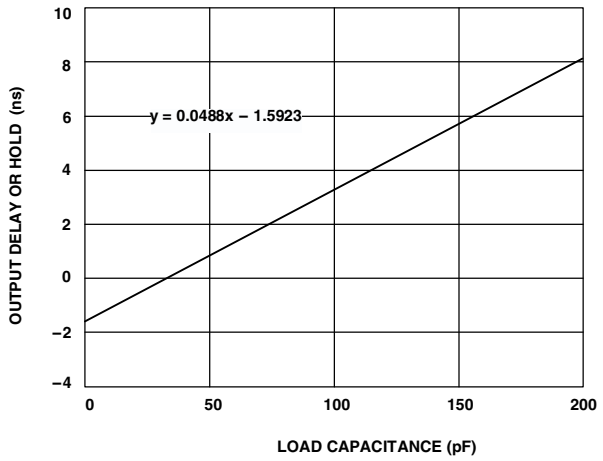


Figure 42. Typical Output Delay or Hold versus Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions on Page 14.

Table 42 through Table 44 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board and thermal via design comply with JEDEC standards JESD51-9 (BGA) and JESD51-5 (LQFP_EP). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

Industrial applications using the BGA package require thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

Industrial applications using the LQFP_EP package require thermal trace squares and thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-5 for more information.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 42 through Table 44.

P_D = power dissipation. See the Engineer-to-Engineer Note "*Estimating Power for the ADSP-21362 SHARC Processors*" (EE-277) for more information.

Values of θ_{JA} are provided for package comparison and PCB design considerations.

Values of θ_{JC} are provided for package comparison and PCB design considerations when an exposed pad is required. Note that the thermal characteristics values provided in Table 42 through Table 44 are modeled values.

Table 42. Thermal Characteristics for BGA (No Thermal vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	25.40	°C/W
θ_{JMA}	Airflow = 1 m/s	21.90	°C/W
θ_{JMA}	Airflow = 2 m/s	20.90	°C/W
θ_{JC}		5.07	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.140	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.330	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.410	°C/W

Table 43. Thermal Characteristics for BGA (Thermal vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	23.40	°C/W
θ_{JMA}	Airflow = 1 m/s	20.00	°C/W
θ_{JMA}	Airflow = 2 m/s	19.20	°C/W
θ_{JC}		5.00	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.130	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.300	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.360	°C/W

Table 44. Thermal Characteristics for LQFP_EP (with Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	16.80	°C/W
θ_{JMA}	Airflow = 1 m/s	14.20	°C/W
θ_{JMA}	Airflow = 2 m/s	13.50	°C/W
θ_{JC}		7.25	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.51	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.72	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.80	°C/W

Table 46. BGA Pin Assignments (Continued)

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
AD5	J01	AD3	K01	AD2	L01	AD0	M01
AD4	J02	V_{DDINT}	K02	AD1	L02	$\overline{WR}$	M02
GND	J04	GND	K04	GND	L04	GND	M03
GND	J05	GND	K05	GND	L05	GND	M12
GND	J06	GND	K06	GND	L06	DAI_P12 (SD3B)	M13
GND	J09	GND	K09	GND	L09	DAI_P13 (SCLK3)	M14
GND	J10	GND	K10	GND	L10		
GND	J11	GND	K11	GND	L11		
V_{DDINT}	J13	GND	K13	GND	L13		
DAI_P16 (SD4B)	J14	DAI_P15 (SD4A)	K14	DAI_P14 (SFS3)	L14		
AD15	N01	AD14	P01				
ALE	N02	AD13	P02				
$\overline{RD}$	N03	AD12	P03				
V_{DDINT}	N04	AD11	P04				
V_{DDEXT}	N05	AD10	P05				
AD8	N06	AD9	P06				
V_{DDINT}	N07	DAI_P1 (SD0A)	P07				
DAI_P2 (SD0B)	N08	DAI_P3 (SCLK0)	P08				
V_{DDEXT}	N09	DAI_P5 (SD1A)	P09				
DAI_P4 (SFS0)	N10	DAI_P6 (SD1B)	P10				
V_{DDINT}	N11	DAI_P7 (SCLK1)	P11				
V_{DDINT}	N12	DAI_P8 (SFS1)	P12				
GND	N13	DAI_P9 (SD2A)	P13				
DAI_P10 (SD2B)	N14	DAI_P11 (SD3A)	P14				

Figure 45 and Figure 46 show BGA pin assignments from the bottom and top, respectively.

Note: Use the center block of ground pins to provide thermal pathways to your printed circuit board's ground plane.

AUTOMOTIVE PRODUCTS

Some ADSP-2136x models are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 48. Automotive Products

Model	Notes	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
AD21362WBBCZ1xx	2	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21362WBSWZ1xx	2	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21362WYSWZ2xx	2	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WBBCZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21363WBSWZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WYSWZ2xx		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WBBCZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21364WBSWZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WYSWZ2xx		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ1xxA	2, 3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ1xxF	2, 3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WYSWZ2xxA	2, 3, 4	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WBBCZ1xxA	3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21366WBSWZ1xxA	3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WYSWZ2xxA	3, 4	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 14 for junction temperature (T_J) specification which is the only temperature specification.

[2] License from DTLA required for these products.

[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/sharc.

[4] License from Dolby Laboratories, Inc., and Digital Theater Systems (DTS) required for these products.