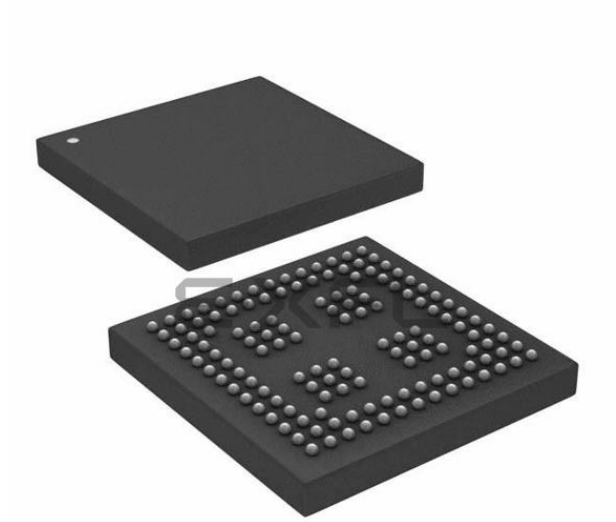


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, SPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	136-LFBGA, CSPBGA
Supplier Device Package	136-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21363kbc-1aa

GENERAL DESCRIPTION

The ADSP-2136x SHARC® processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices, Inc., Super Harvard Architecture. The processor is source code-compatible with the ADSP-2126x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2136x are 32-/40-bit floating-point processors optimized for high performance automotive audio applications. They contain a large on-chip SRAM and ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital audio interface (DAI).

As shown in the functional block diagram on Page 1, the ADSP-2136x uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of signal processing algorithms. With its SIMD computational hardware, the ADSP-2136x can perform two GFLOPS running at 333 MHz.

Table 1 shows performance benchmarks for these devices. Table 2 shows the features of the individual product offerings.

Table 1. Benchmarks (at 333 MHz)

Benchmark Algorithm	Speed (at 333 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	27.9 µs
FIR Filter (per tap)[1]	1.5 ns
IIR Filter (per biquad)[1]	6.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	13.5 ns
[4×4] × [4×1]	23.9 ns
Divide (y/x)	10.5 ns
Inverse Square Root	16.3 ns

[1] Assumes two files in multichannel SIMD mode.

Table 2. ADSP-2136x Family Features

Feature	ADSP-21362	ADSP-21363	ADSP-21364	ADSP-21365	ADSP-21366
RAM	3M bit	3M bit	3M bit	3M bit	3M bit
ROM	4M bit	4M bit	4M bit	4M bit	4M bit
Audio Decoders in ROM[1]	No	No	No	Yes	Yes
Pulse-Width Modulation	Yes	Yes	Yes	Yes	Yes
S/PDIF	Yes	No	Yes	Yes	Yes
DTCP[2]	Yes	No	No	Yes	No
SRC SNR Performance	–128 dB	No SRC	–140 dB	–128 dB	–128 dB

[1] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Pro Logic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[2] The ADSP-21362 and ADSP-21365 processors provide the Digital Transmission Content Protection protocol, a proprietary security protocol. Contact your Analog Devices sales office for more information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-2136x processors. The core clock domain contains the following features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (3M bit)
- On-chip mask-programmable ROM (4M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints, which allow flexible exception handling.

The diagram on Page 1 also shows the following architectural features:

- I/O processor that handles 32-bit DMA for the peripherals
- Six full duplex serial ports
- Two SPI-compatible interface ports—primary on dedicated pins, secondary on DAI pins
- 8-bit or 16-bit parallel port that supports interfaces to off-chip memory peripherals
- Digital audio interface that includes two precision clock generators (PCG), an input data port with eight serial interfaces (IDP), an S/PDIF receiver/transmitter, 8-channel asynchronous sample rate converter (ASRC), DTCP cipher, six serial ports, a 20-bit parallel input data port (PDAP), 10 interrupts, six flag outputs, six flag inputs, three timers, and a flexible signal routing unit (SRU)

audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of two units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A and B, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Peripheral Timers

The following three general-purpose timers can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

Each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

I/O PROCESSOR FEATURES

The processor's I/O provides many channels of DMA and controls the extensive set of peripherals described in the previous sections.

DMA Controller

The processor's on-chip DMA controllers allow data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the parallel port (PP). See Table 4.

Table 4. DMA Channels

Peripheral	ADSP-2136x
SPORTs	12
IDP/PDAP	8
SPI	2
MTM/DTCP	2
Parallel Port	1
Total DMA Channels	25

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the processor boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins in Table 5. Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Table 5. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port Boot via EPROM
11	No booting occurs. Processor executes from internal ROM after reset.

Phase-Locked Loop

The processors use an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK_CFG1–0 pins are used to select ratios of 32:1, 16:1, and 6:1. After booting, numerous other ratios can be selected via software control.

The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 1, 2, 4, and 8.

Power Supplies

The processor has a separate power supply connection for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2 V requirement for K, B, and Y grade models, and the 1.0 V requirement for Y models. (For information on the temperature ranges offered for this product, see Operating Conditions on Page 14, Package Information on Page 16, and Ordering Guide on Page 56.) The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 3. (A recommended ferrite chip is the muRata BLM18AG102SN1D.) To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 3 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the processor's architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference* and the *ADSP-2136x SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
BOOT_CFG1–0	I	Input only	**Boot Configuration Select.** This pin is used to select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. For a description of the boot mode, refer to Table 5, Boot Mode Selection.
$\overline{\text{RESETOUT}}$	O	Output only	**Reset Out.** Drives out the core reset signal to an external device.
$\overline{\text{RESET}}$	I/A	Input only	**Processor Reset.** Resets the ADSP-2136x to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Input only[3]	**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the processors.
TMS	I/S (pu)	Three-state with pull-up enabled	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TDI	I/S (pu)	Three-state with pull-up enabled	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 k internal pull-up resistor.
TDO	O	Three-state[4]	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A (pu)	Three-state with pull-up enabled	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2136x. $\overline{\text{TRST}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D) (pu)	Three-state with pull-up enabled	**Emulation Status.** Must be connected to the processor's JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 kΩ internal pull-up resistor.
V_{DDINT}	P		**Core Power Supply.** Supplies the processor's core.
V_{DDEXT}	P		**I/O Power Supply.**
A_{VDD}	P		**Analog Power Supply.** Supplies the processor's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 8.
A_{VSS}	G		**Analog Power Supply Return.**
GND	G		**Power Supply Return.**

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

[1] $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE are three-stated (and not driven) only when $\overline{\text{RESET}}$ is active.
[2] Output only is a three-state driver with its output path always enabled.
[3] Input only is a three-state driver with both output path and pull-up disabled.
[4] Three-state is a three-state driver with pull-up disabled.

SPECIFICATIONS

Specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter	Description	K Grade			B Grade			Y Grade			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{DDINT}	Internal (Core) Supply Voltage	1.14	1.2	1.26	1.14	1.2	1.26	0.95	1.0	1.05	V
A_{VDD}	Analog (PLL) Supply Voltage	1.14	1.2	1.26	1.14	1.2	1.26	0.95	1.0	1.05	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{IH}[1]	High Level Input Voltage @ V_{DDEXT} = Max	2.0		V_{DDEXT} + 0.5	2.0		V_{DDEXT} + 0.5	2.0		V_{DDEXT} + 0.5	V
V_{IL}[1]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5		+0.8	–0.5		+0.8	–0.5		+0.8	V
V_{IH_CLKIN}[2]	High Level Input Voltage @ V_{DDEXT} = Max	1.74		V_{DDEXT} + 0.5	1.74		V_{DDEXT} + 0.5	1.74		V_{DDEXT} + 0.5	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5		+1.19	–0.5		+1.19	–0.5		+1.19	V
T_J[3, 4]	Junction Temperature 136-Ball CSP_BGA	0		+110	–40		+125	–40		+125	°C
T_J[3, 4]	Junction Temperature 144-Lead LQFP_EP	0		+110	–40		+125	–40		+125	°C

[1] Applies to input and bidirectional pins: AD15–0, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, and $\overline{TRST}$.
[2] Applies to input pin CLKIN.
[3] See Thermal Characteristics on Page 47 for information on thermal specifications.
[4] See the Engineer-to-Engineer Note *"Estimating Power for the ADSP-21362 SHARC Processors"* (EE-277) for further information.

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP pin).

Table 14. Core Timer

Parameter		Min	Unit
Switching Characteristic			
t_{WCTIM}	TMREXP Pulse Width	$2 \times t_{PCLK} - 1$	ns

Figure 11. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 15. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

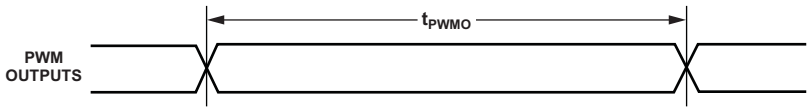


Figure 12. Timer PWM_OUT Timing

Flags

The timing specifications provided below apply to the FLAG3–0 and DAI_P20–1 pins, the parallel port, and the serial peripheral interface (SPI). See Table 6 on Page 11 for more information on flag use.

Table 19. Flags

Parameter		Min	Unit
Timing Requirement			
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$	ns
Switching Characteristic			
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1$	ns

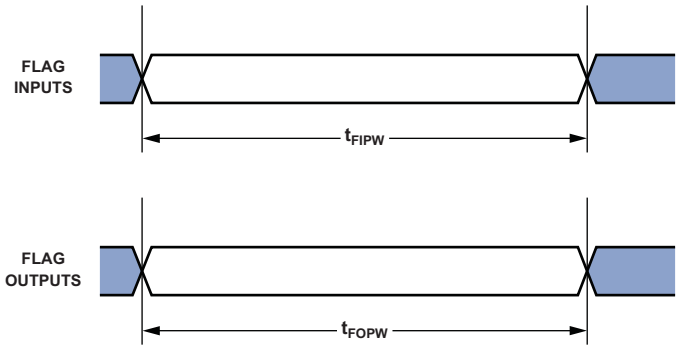


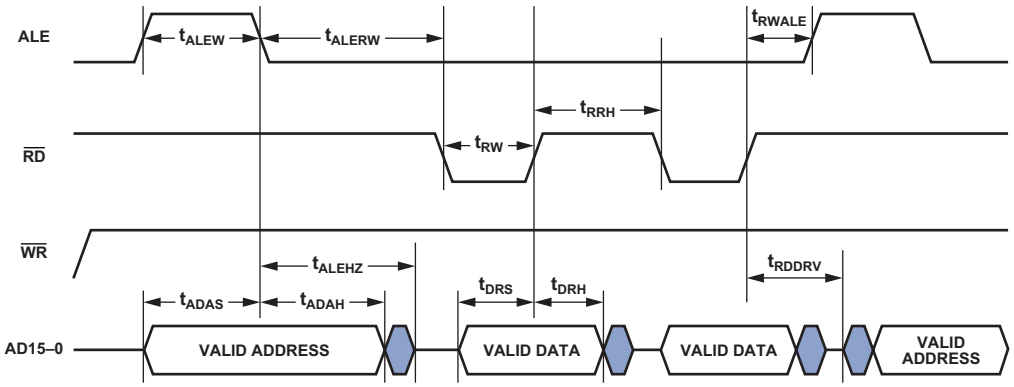
Figure 16. Flags

Table 21. 16-Bit Memory Read Cycle

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{DRS}	AD15–0 Data Setup Before $\overline{RD}$ High	3.3		4.5		ns
t_{DRH}	AD15–0 Data Hold After $\overline{RD}$ High	0		0		ns
Switching Characteristics						
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$		$2 \times t_{PCLK} - 2.0$		ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$		$t_{PCLK} - 2.5$		ns
t_{ALERW}	ALE Deasserted to Read Asserted	$2 \times t_{PCLK} - 3.8$		$2 \times t_{PCLK} - 3.8$		ns
t_{RRH}[2]	Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge	$H + t_{PCLK} - 1.4$		$H + t_{PCLK} - 1.4$		ns
t_{RWALE}	Read Deasserted to ALE Asserted	$F + H + 0.5$		$F + H + 0.5$		ns
t_{RDDRV}	ALE Address Drive After Read High	$F + H + t_{PCLK} - 2.3$		$F + H + t_{PCLK} - 2.3$		ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$		$t_{PCLK} - 2.3$		ns
t_{ALEHZ1}	ALE Deasserted to Address/Data15–0 in High-Z	t_{PCLK}	$t_{PCLK} + 3.0$	t_{PCLK}	$t_{PCLK} + 3.8$	ns
t_{RW}	$\overline{RD}$ Pulse Width	$D - 2.0$		$D - 2.0$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) $\times t_{PCLK}$
$H = t_{PCLK}$ (if a hold cycle is specified, else $H = 0$)
$F = 7 \times t_{PCLK}$ (if FLASH_MODE is set, else $F = 0$)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY READS, WHEN EMPP ≠ 0, ONLY ONE $\overline{RD}$ PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE $\overline{RD}$ PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 18. Read Cycle for 16-Bit Memory Timing

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync (FS) delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 24. Serial Ports—External Clock

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	2.5			ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5			ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 2$			ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$			ns
Switching Characteristics					
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)		9.5	11	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)	2			ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		9.5	11	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2			ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 25. Serial Ports—Internal Clock

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	7			ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7			ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5			ns
Switching Characteristics					
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		3	3.5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0			ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		8	9.5	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0			ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3	4.0	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0			ns
t_{SCLKIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 2$	$2 \times t_{PCLK} + 2$	$2 \times t_{PCLK} + 2$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 29. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the IDP, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, "Input Data Port" chapter.

Note that the most significant 16 bits of external 20-bit PDAP data can be provided through either the parallel port AD15–0 pins or the DAI_P20–5 pins. The remaining 4 bits can only be sourced through DAI_P4–1. The timing below is valid at the DAI_P20–1 pins or at the AD15–0 pins.

Table 29. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Unit
Timing Requirements			
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	2.5	ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	2.5	ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	3.0	ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	2.5	ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$	ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$	ns
Switching Characteristics			
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} - 1$	ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$	ns

[1] Data source pins are AD15–0 and DAI_P4–1, or DAI pins. Source pins for serial clock and frame sync are DAI pins.

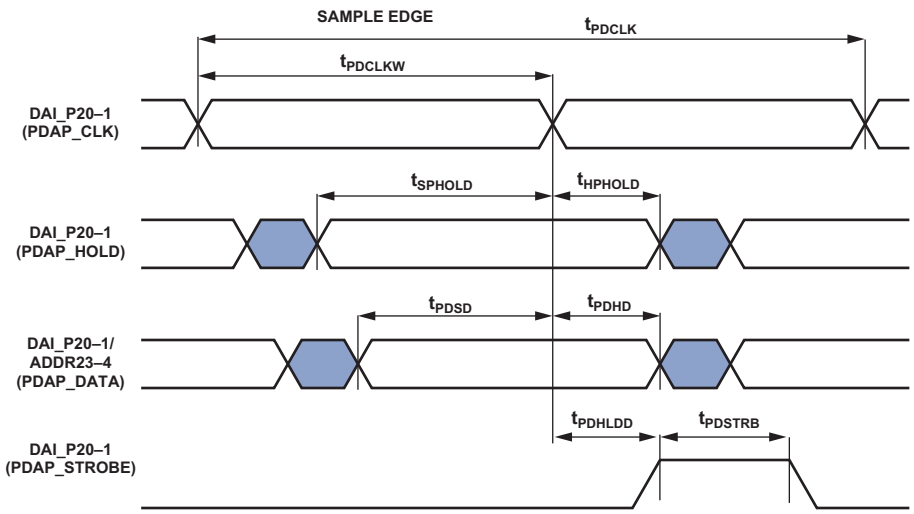


Figure 25. PDAP Timing

Pulse-Width Modulation Generators

Table 30. PWM Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

[1] Note that the PWM output signals are shared on the parallel port bus (AD15-0 pins).

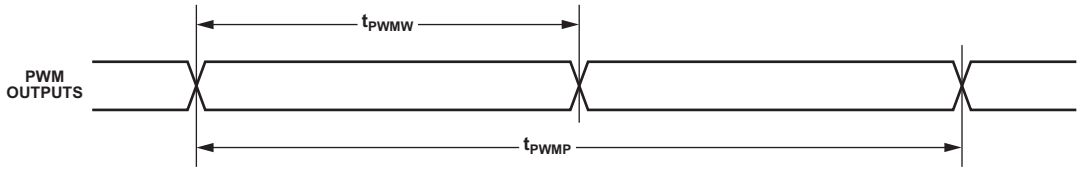


Figure 26. PWM Timing

Sample Rate Converter—Serial Input Port

The SRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 31 are valid at the DAI_P20–1 pins. This feature is not available on the ADSP-21363 models.

Table 31. SRC, Serial Input Port

Parameter		Min	Unit
Timing Requirements			
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3	ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3	ns
t_{SRCSD}[1]	SDATA Setup Before Serial Clock Rising Edge	3	ns
t_{SRCHD}[1]	SDATA Hold After Serial Clock Rising Edge	3	ns
$t_{SRCCLKW}$	Clock Width	36	ns
t_{SRCCLK}	Clock Period	80	ns

[1] The data, serial clock, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via the PCGs or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

Figure 30 shows the default I²S-justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

Table 34. S/PDIF Transmitter I²S Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{I2SD}	FS to MSB Delay in I²S Mode	1	SCLK

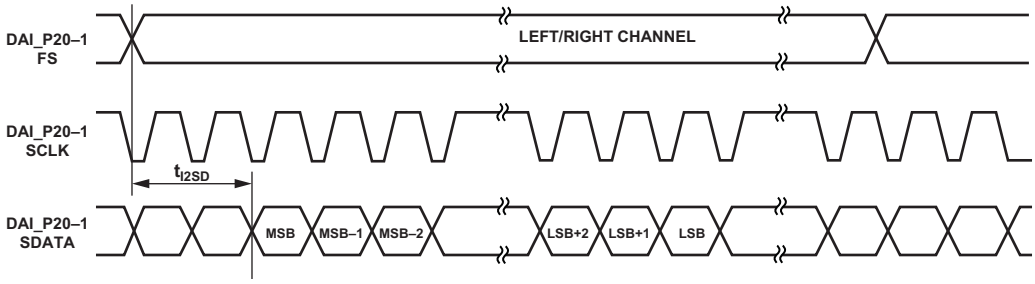


Figure 30. I²S-Justified Mode

Figure 31 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

Table 35. S/PDIF Transmitter Left-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{LJD}	FS to MSB Delay in Left-Justified Mode	0	SCLK

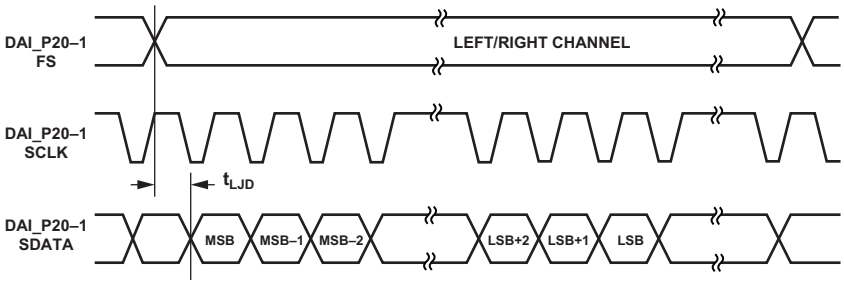


Figure 31. Left-Justified Mode

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver. This feature is not available on the ADSP-21363 processors.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 38. S/PDIF Receiver Output Timing (Internal Digital PLL Mode)

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After Serial Clock		5	ns
t_{HOFSI}	Frame Sync Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	38		ns

[1] Serial clock frequency is 64 ×FS where FS = the frequency of frame sync.

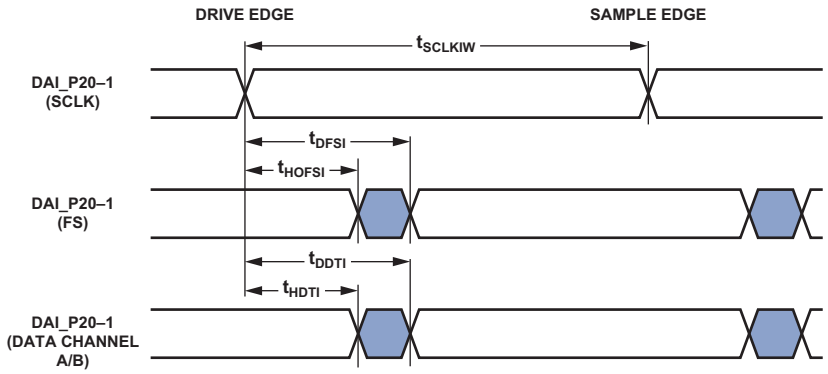


Figure 33. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Slave

Table 40. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$			ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$			ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$			ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge				
	CPHASE = 0	$2 \times t_{PCLK}$			ns
	CPHASE = 1	$2 \times t_{PCLK}$			ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$			ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2			ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2			ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$			ns
Switching Characteristics					
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	5	5	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	8	9	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	5	5.5	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	8.6	10	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	11.0	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$			ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, "Serial Peripheral Interface Port" chapter.

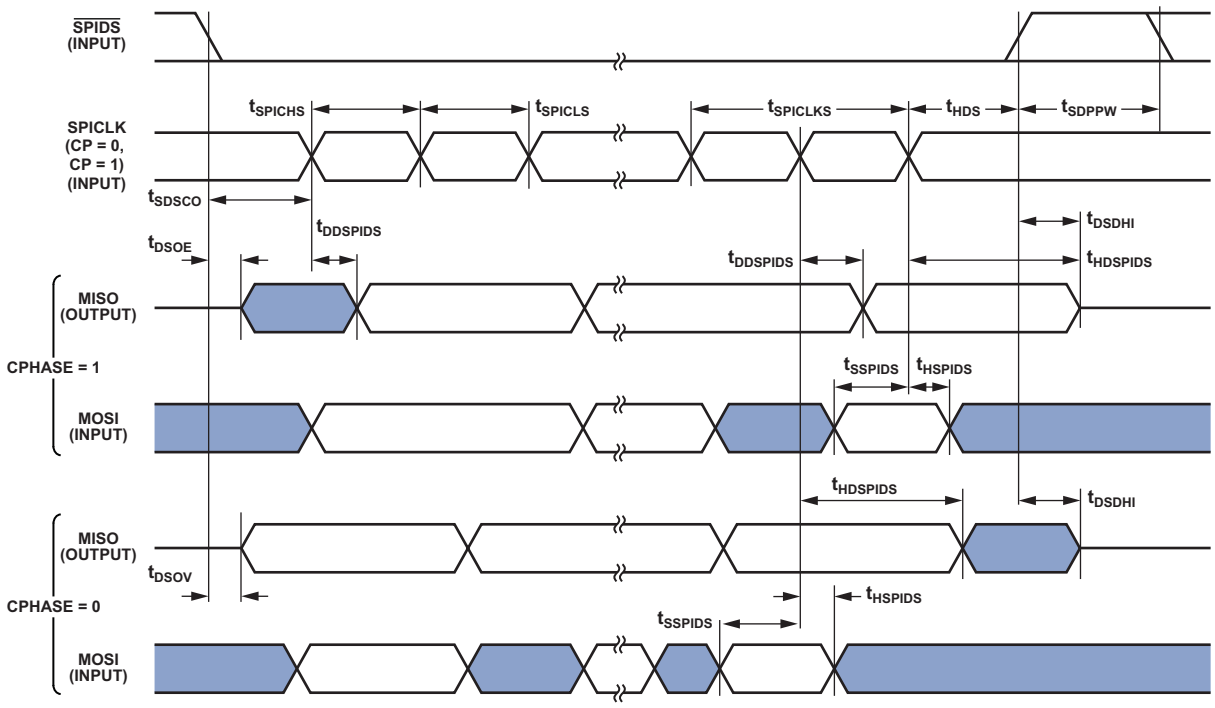


Figure 35. SPI Slave Timing

144-LEAD LQFP_EP PIN CONFIGURATIONS

The following table shows the processor's pin names and, when applicable, their default function after reset in parentheses.

Table 45. LQFP_EP Pin Assignments

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
V_{DDINT}	1	V_{DDINT}	37	V_{DDEXT}	73	GND	109
CLK_CFG0	2	GND	38	GND	74	V_{DDINT}	110
CLK_CFG1	3	$\overline{RD}$	39	V_{DDINT}	75	GND	111
BOOT_CFG0	4	ALE	40	GND	76	V_{DDINT}	112
BOOT_CFG1	5	AD15	41	DAI_P10 (SD2B)	77	GND	113
GND	6	AD14	42	DAI_P11 (SD3A)	78	V_{DDINT}	114
V_{DDEXT}	7	AD13	43	DAI_P12 (SD3B)	79	GND	115
GND	8	GND	44	DAI_P13 (SCLK3)	80	V_{DDEXT}	116
V_{DDINT}	9	V_{DDEXT}	45	DAI_P14 (SFS3)	81	GND	117
GND	10	AD12	46	DAI_P15 (SD4A)	82	V_{DDINT}	118
V_{DDINT}	11	V_{DDINT}	47	V_{DDINT}	83	GND	119
GND	12	GND	48	GND	84	V_{DDINT}	120
V_{DDINT}	13	AD11	49	GND	85	$\overline{RESET}$	121
GND	14	AD10	50	DAI_P16 (SD4B)	86	$\overline{SPIDS}$	122
FLAG0	15	AD9	51	DAI_P17 (SD5A)	87	GND	123
FLAG1	16	AD8	52	DAI_P18 (SD5B)	88	V_{DDINT}	124
AD7	17	DAI_P1 (SD0A)	53	DAI_P19 (SCLK5)	89	SPICLK	125
GND	18	V_{DDINT}	54	V_{DDINT}	90	MISO	126
V_{DDINT}	19	GND	55	GND	91	MOSI	127
GND	20	DAI_P2 (SD0B)	56	GND	92	GND	128
V_{DDEXT}	21	DAI_P3 (SCLK0)	57	V_{DDEXT}	93	V_{DDINT}	129
GND	22	GND	58	DAI_P20 (SFS5)	94	V_{DDEXT}	130
V_{DDINT}	23	V_{DDEXT}	59	GND	95	A_{vdd}	131
AD6	24	V_{DDINT}	60	V_{DDINT}	96	A_{vss}	132
AD5	25	GND	61	FLAG2	97	GND	133
AD4	26	DAI_P4 (SFS0)	62	FLAG3	98	$\overline{RESETOUT}$	134
V_{DDINT}	27	DAI_P5 (SD1A)	63	V_{DDINT}	99	$\overline{EMU}$	135
GND	28	DAI_P6 (SD1B)	64	GND	100	TDO	136
AD3	29	DAI_P7 (SCLK1)	65	V_{DDINT}	101	TDI	137
AD2	30	V_{DDINT}	66	GND	102	$\overline{TRST}$	138
V_{DDEXT}	31	GND	67	V_{DDINT}	103	TCK	139
GND	32	V_{DDINT}	68	GND	104	TMS	140
AD1	33	GND	69	V_{DDINT}	105	GND	141
AD0	34	DAI_P8 (SFS1)	70	GND	106	CLKIN	142
$\overline{WR}$	35	DAI_P9 (SD2A)	71	V_{DDINT}	107	XTAL	143
V_{DDINT}	36	V_{DDINT}	72	V_{DDINT}	108	V_{DDEXT}	144
						GND	145*

*The ePAD is electrically connected to GND inside the chip (see Figure 43 and Figure 44), therefore connecting the pad to GND is optional. For better thermal performance the ePAD should be soldered to the board and thermally connected to the GND plane with vias.

Figure 43 shows the top view of the 144-lead LQFP_EP pin configuration. Figure 44 shows the bottom view of the 144-lead LQFP_EP lead configuration.

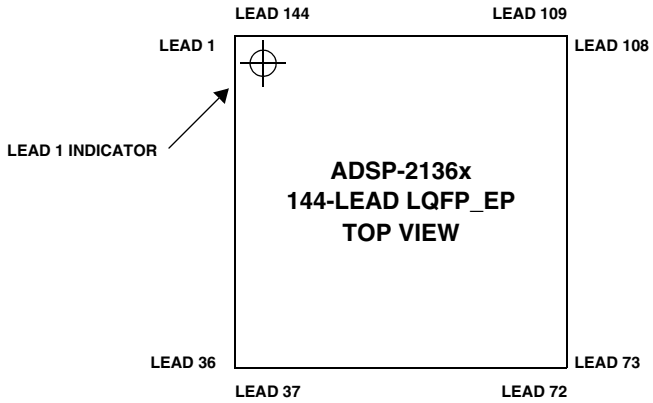


Figure 43. 144-Lead LQFP_EP Lead Configuration (Top View)

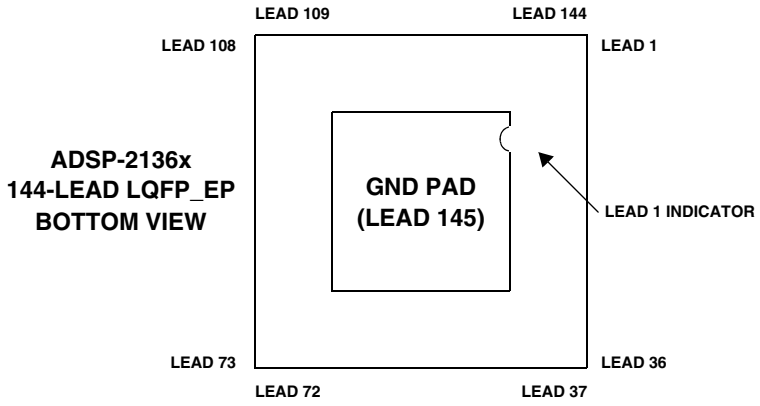
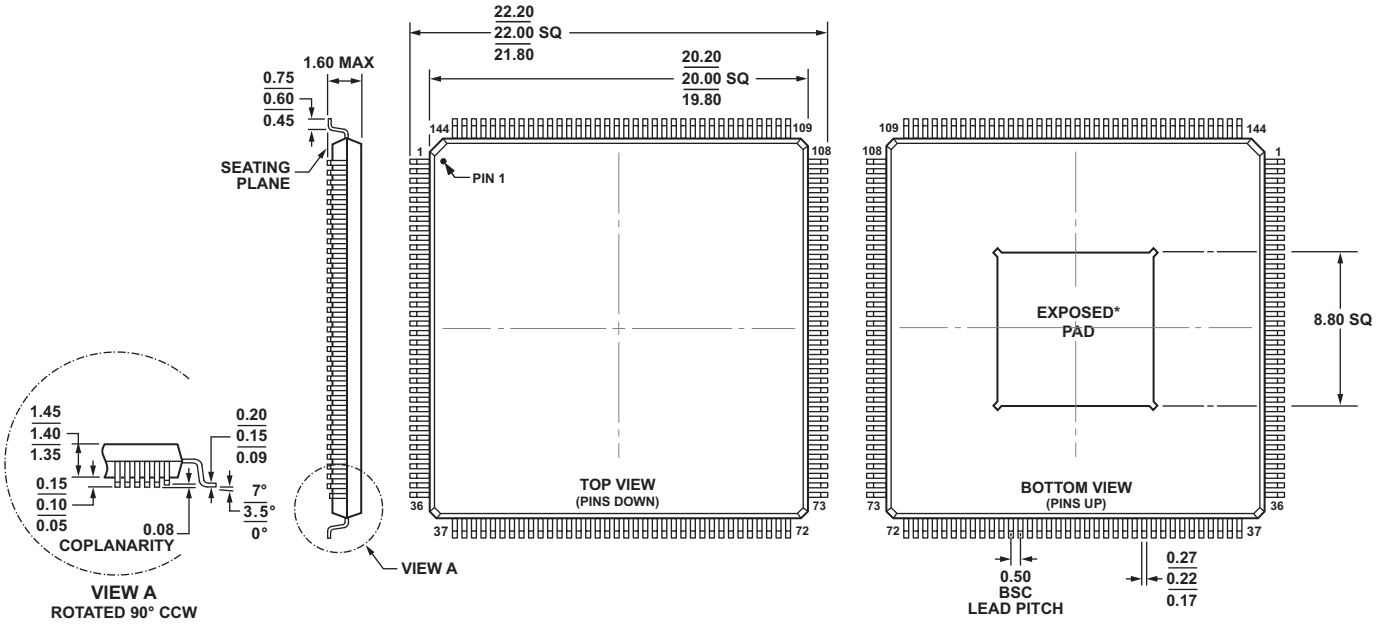


Figure 44. 144-Lead LQFP_EP Lead Configuration (Bottom View)

PACKAGE DIMENSIONS

The processor is available in 136-ball BGA and 144-lead exposed pad (LQFP_EP) packages.



COMPLIANT TO JEDEC STANDARDS MS-026-BFB-HD
*EXPOSED PAD IS COINCIDENT WITH BOTTOM SURFACE AND DOES NOT PROTRUDE BEYOND IT. EXPOSED PAD IS CENTERED.

Figure 47. 144-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP[1]]
(SW-144-1)
Dimensions shown in millimeters

[1] For information relating to the exposed pad on the SW-144-1 package, see the table endnote on Page 48.

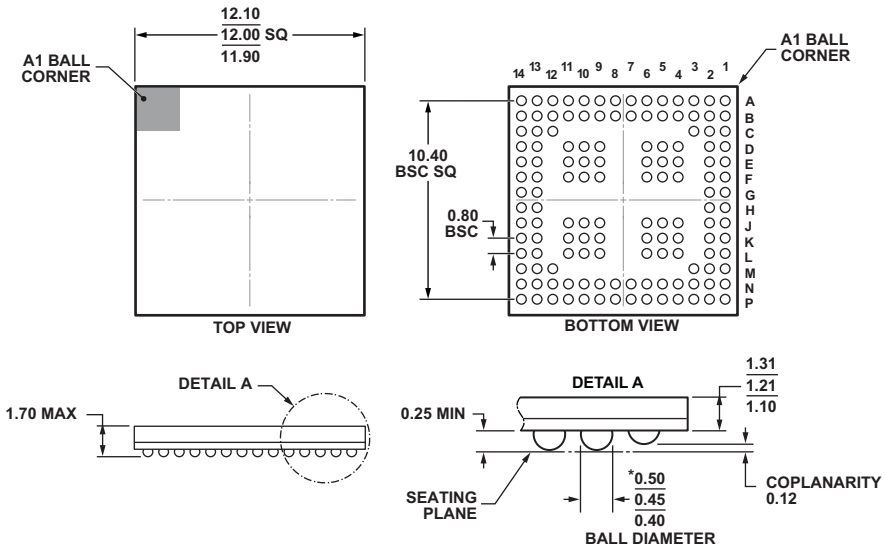


Figure 48. 136-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-136-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 47 is provided as an aid to PCB design. For industry standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 47. BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
136-Ball CSP_BGA (BC-136-1)	Solder Mask Defined	0.40 mm diameter	0.53 mm diameter