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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, SPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-LQFP-EP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21363kswz-1aa

Table 3. ADSP-2136x Internal Memory Space

IOP Registers 0x0000 0000–0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM 0x0004 0000–0x0004 7FFF	Block 0 ROM 0x0008 0000–0x0008 AAA9	Block 0 ROM 0x0008 0000–0x0008 FFFF	Block 0 ROM 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 BFFF		Reserved 0x0009 0000–0x0009 7FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 C000–0x0004 FFFF	Block 0 SRAM 0x0009 0000–0x0009 5554	Block 0 SRAM 0x0009 8000–0x0009 FFFF	Block 0 SRAM 0x0013 0000–0x0013 FFFF
Block 1 ROM 0x0005 0000–0x0005 7FFF	Block 1 ROM 0x000A 0000–0x000A AAA9	Block 1 ROM 0x000A 0000–0x000A FFFF	Block 1 ROM 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 BFFF		Reserved 0x000B 0000–0x000B 7FFF	Reserved 0x0016 0000–0x0016 FFFF
Block 1 SRAM 0x0005 C000–0x0005 FFFF	Block 1 SRAM 0x000B 0000–0x000B 5554	Block 1 SRAM 0x000B 8000–0x000B FFFF	Block 1 SRAM 0x0017 0000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000–0x0006 FFFF		Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF		Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF
			Reserved 0x0020 0000–0xFFFF FFFF

or test access port, is assigned to each customer. The device ignores a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2136x family contains a rich set of peripherals that support a wide variety of applications, including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, monitor control, imaging, and other applications.

Parallel Port

The parallel port provides interfaces to SRAM and peripheral devices. The multiplexed address and data pins (AD15–0) can access 8-bit devices with up to 24 bits of address, or 16-bit devices with up to 16 bits of address. In either mode, 8-bit or 16-bit, the maximum data transfer rate is $f_{PCLK}/4$.

DMA transfers are used to move data to and from internal memory. Access to the core is also facilitated through the parallel port register read/write functions. The $\overline{RD}$, $\overline{WR}$, and ALE (address latch enable) pins are the control pins for the parallel port.

Serial Peripheral (Compatible) Interface

The processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the processor's SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes and can operate at a maximum baud rate of $f_{PCLK}/4$.

The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-2136x SPI-compatible peripheral implementation also features programmable baud rate, clock phase, and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

Pulse-Width Modulation

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can

generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

Digital Audio Interface (DAI)

The digital audio interface (DAI) provides the ability to connect various peripherals to any of the DSP's DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU, shown in Figure 1).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI-associated peripherals for a wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes six serial ports, an S/PDIF receiver/transmitter, a DTCP cipher, a precision clock generator (PCG), eight channels of asynchronous sample rate converters, an input data port (IDP), an SPI port, six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2136x core, configurable as either eight channels of I^2S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports

The processor features six synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and a frame sync and they can operate at maximum $f_{PCLK}/4$. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Left-justified sample pair mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the transmitter can be formatted as left-justified, I^2S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

Digital Transmission Content Protection (DTCP)

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) is protected by this copy protection system. This feature is available on the ADSP-21362 and ADSP-21365 processors only. Licensing through DTLA is required for these products. Visit www.dtcp.com for more information.

Memory-to-Memory (MTM)

If the DTCP module is not used, the memory-to-memory DMA module allows internal memory copies for a standard DMA.

Synchronous/Asynchronous Sample Rate Converter (SRC)

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 140 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC is used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

The S/PDIF and SRC are not available on the ADSP-21363 models.

Input Data Port (IDP)

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive

audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of two units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A and B, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Peripheral Timers

The following three general-purpose timers can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

Each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

I/O PROCESSOR FEATURES

The processor's I/O provides many channels of DMA and controls the extensive set of peripherals described in the previous sections.

DMA Controller

The processor's on-chip DMA controllers allow data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the parallel port (PP). See Table 4.

Table 4. DMA Channels

Peripheral	ADSP-2136x
SPORTs	12
IDP/PDAP	8
SPI	2
MTM/DTCP	2
Parallel Port	1
Total DMA Channels	25

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the processor boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins in Table 5. Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Table 5. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port Boot via EPROM
11	No booting occurs. Processor executes from internal ROM after reset.

Phase-Locked Loop

The processors use an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK_CFG1–0 pins are used to select ratios of 32:1, 16:1, and 6:1. After booting, numerous other ratios can be selected via software control.

The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 1, 2, 4, and 8.

Power Supplies

The processor has a separate power supply connection for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2 V requirement for K, B, and Y grade models, and the 1.0 V requirement for Y models. (For information on the temperature ranges offered for this product, see Operating Conditions on Page 14, Package Information on Page 16, and Ordering Guide on Page 56.) The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 3. (A recommended ferrite chip is the muRata BLM18AG102SN1D.) To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 3 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

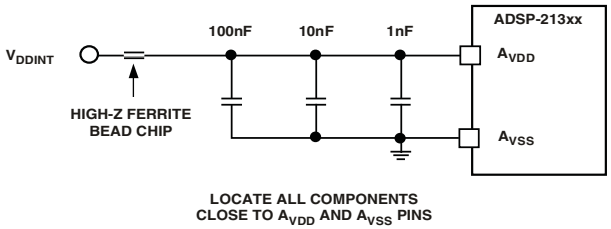


Figure 3. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices' DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processor to monitor and control the target board processor during emulation. Analog Devices' DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator does not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, refer to the appropriate emulator user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and

VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the processor's architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference* and the *ADSP-2136x SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PACKAGE INFORMATION

The information presented in Figure 4 provides details about the package branding for the ADSP-2136x processor. For a complete listing of product availability, see Ordering Guide on Page 56.

Figure 4. Typical Package Brand

Table 7. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See the Engineer-to-Engineer Note *"Estimating Power for the ADSP-21362 SHARC Processors"* (EE-277) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 47.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 8 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. For voltage reference levels, see Figure 39 on Page 46 under Test Conditions.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 5). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 11.

Reset

Table 12. Reset

Parameter		Min	Unit
Timing Requirements			
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$	ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

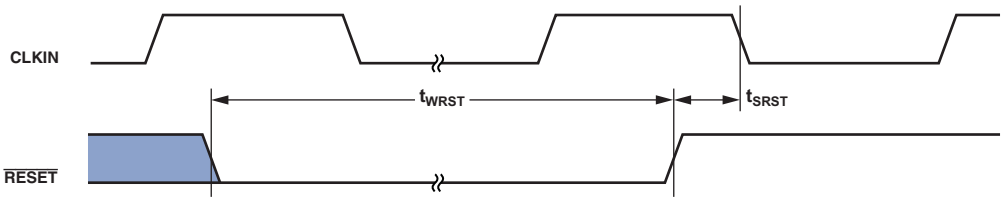


Figure 9. Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts.

Table 13. Interrupts

Parameter		Min	Unit
Timing Requirement			
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$	ns

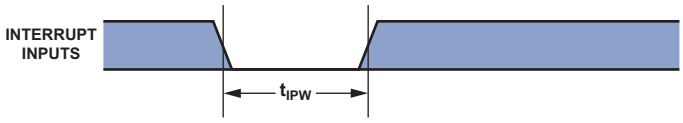


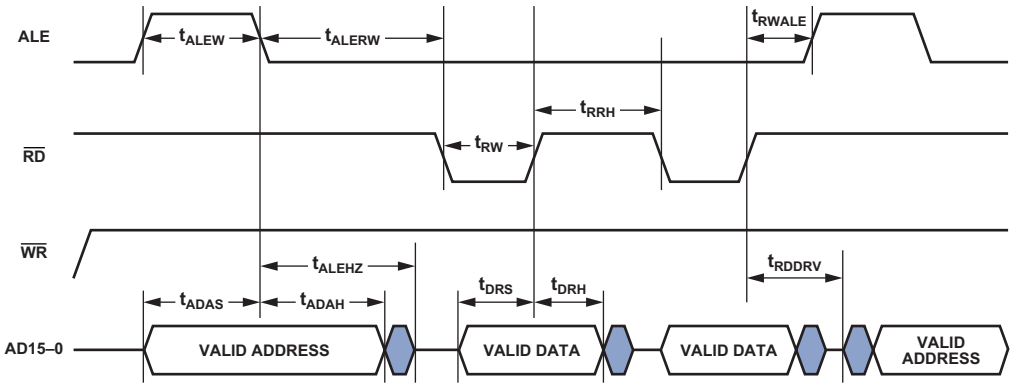
Figure 10. Interrupts

Table 21. 16-Bit Memory Read Cycle

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{DRS}	AD15–0 Data Setup Before $\overline{RD}$ High	3.3		4.5		ns
t_{DRH}	AD15–0 Data Hold After $\overline{RD}$ High	0		0		ns
Switching Characteristics						
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$		$2 \times t_{PCLK} - 2.0$		ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$		$t_{PCLK} - 2.5$		ns
t_{ALERW}	ALE Deasserted to Read Asserted	$2 \times t_{PCLK} - 3.8$		$2 \times t_{PCLK} - 3.8$		ns
t_{RRH}[2]	Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge	$H + t_{PCLK} - 1.4$		$H + t_{PCLK} - 1.4$		ns
t_{RWALE}	Read Deasserted to ALE Asserted	$F + H + 0.5$		$F + H + 0.5$		ns
t_{RDDRV}	ALE Address Drive After Read High	$F + H + t_{PCLK} - 2.3$		$F + H + t_{PCLK} - 2.3$		ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$		$t_{PCLK} - 2.3$		ns
t_{ALEHZ1}	ALE Deasserted to Address/Data15–0 in High-Z	t_{PCLK}	$t_{PCLK} + 3.0$	t_{PCLK}	$t_{PCLK} + 3.8$	ns
t_{RW}	$\overline{RD}$ Pulse Width	$D - 2.0$		$D - 2.0$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) $\times t_{PCLK}$
$H = t_{PCLK}$ (if a hold cycle is specified, else $H = 0$)
$F = 7 \times t_{PCLK}$ (if FLASH_MODE is set, else $F = 0$)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY READS, WHEN EMPP ≠ 0, ONLY ONE $\overline{RD}$ PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE $\overline{RD}$ PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

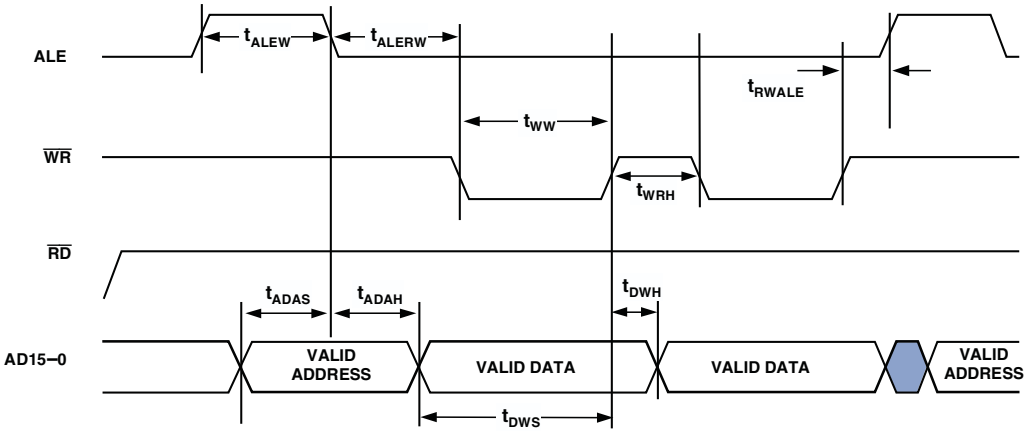
Figure 18. Read Cycle for 16-Bit Memory Timing

Table 23. 16-Bit Memory Write Cycle

Parameter		K and B Grade Min	Y Grade Min	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$	$2 \times t_{PCLK} - 2.0$	ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$	$t_{PCLK} - 2.5$	ns
t_{ALERW}	ALE Deasserted to Write Asserted	$2 \times t_{PCLK} - 3.8$	$2 \times t_{PCLK} - 3.8$	ns
t_{RWALE}	Write Deasserted to ALE Asserted	H + 0.5	H + 0.5	ns
t_{WRH}[2]	Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge	$F + H + t_{PCLK} - 2.3$	$F + H + t_{PCLK} - 2.3$	ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$	$t_{PCLK} - 2.3$	ns
t_{WW}	$\overline{WR}$ Pulse Width	D – F – 2.0	D – F – 2.0	ns
t_{DWS}	AD15–0 Data Setup Before $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns
t_{DWH}	AD15–0 Data Hold After $\overline{WR}$ High	H	H	ns

D = (the value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}.
H = t_{PCLK} (if a hold cycle is specified, else H = 0)
F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0). If FLASH_MODE is set, D must be ≥ 9 × t_{PCLK}.
t_{PCLK} = (peripheral) clock period = 2 × t_{CCLK}

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY WRITES, WHEN EMPP ≠ 0, ONLY ONE $\overline{WR}$ PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE $\overline{WR}$ PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 20. Write Cycle for 16-Bit Memory Timing

Table 26. Serial Ports—External Late Frame Sync

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Switching Characteristics					
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive FS with MCE = 1, MFD = 0		9	10.5	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5			ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as serial mode, and MCE = 1, MFD = 0.

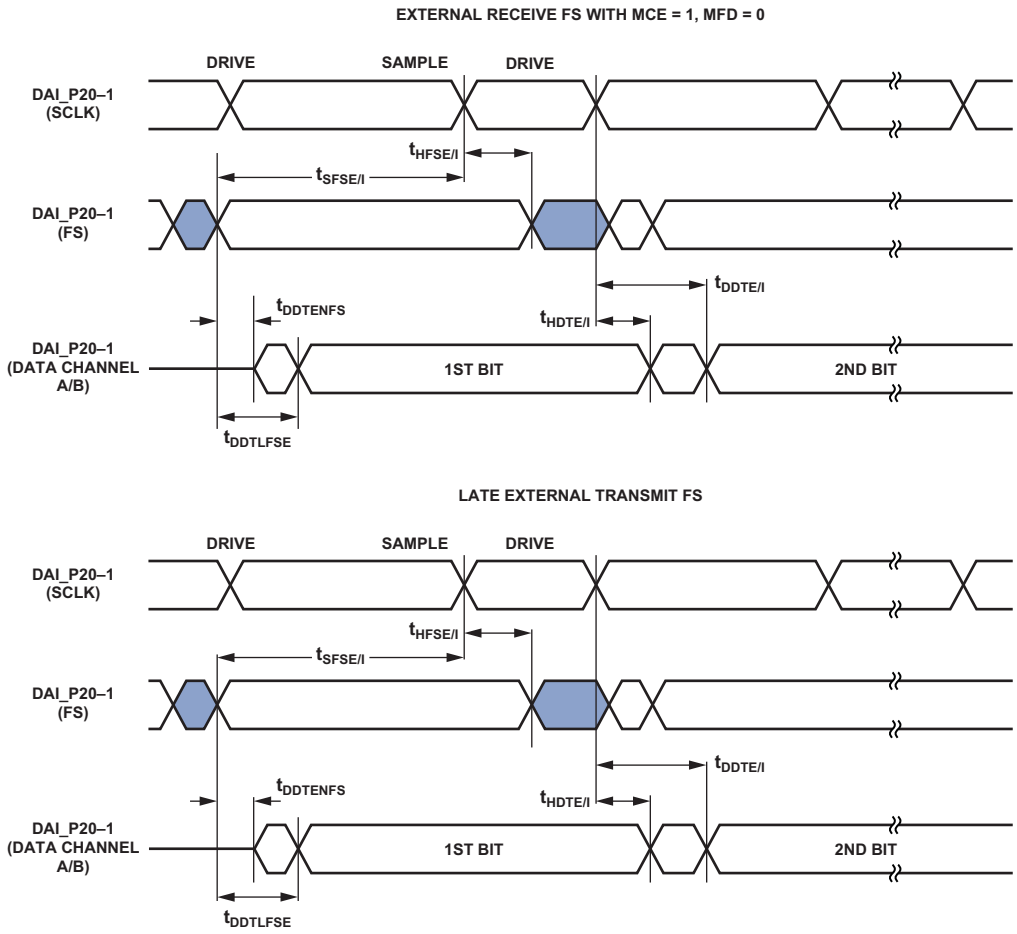


Figure 22. External Late Frame Sync

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 29. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the IDP, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, "Input Data Port" chapter.

Note that the most significant 16 bits of external 20-bit PDAP data can be provided through either the parallel port AD15–0 pins or the DAI_P20–5 pins. The remaining 4 bits can only be sourced through DAI_P4–1. The timing below is valid at the DAI_P20–1 pins or at the AD15–0 pins.

Table 29. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Unit
Timing Requirements			
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	2.5	ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	2.5	ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	3.0	ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	2.5	ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$	ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$	ns
Switching Characteristics			
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} - 1$	ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$	ns

[1] Data source pins are AD15–0 and DAI_P4–1, or DAI pins. Source pins for serial clock and frame sync are DAI pins.

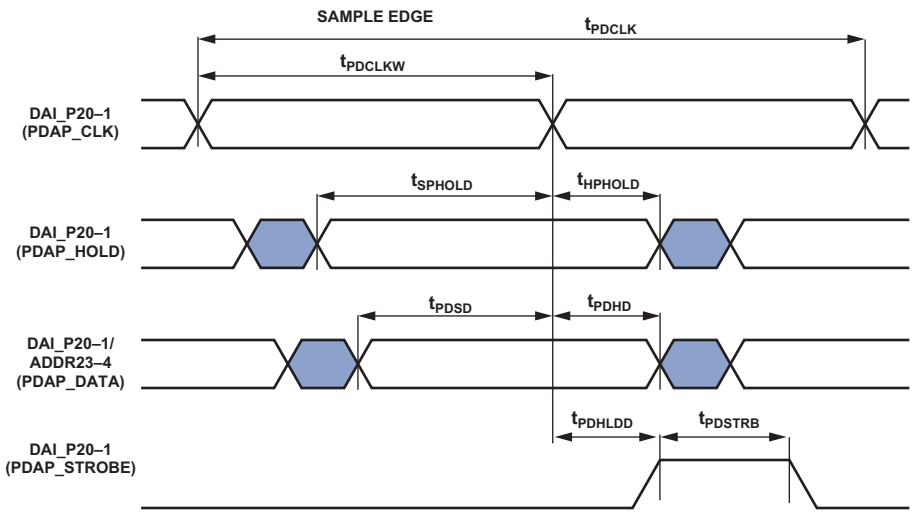


Figure 25. PDAP Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and should meet setup and hold times with regard to the serial clock on the output port. The serial data output has a hold time and delay specification with regard to serial clock. Note that the serial clock rising edge is the sampling edge and the falling edge is the drive edge.

Table 32. SRC, Serial Output Port

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3			ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3			ns
Switching Characteristics					
t_{SRCTDD}[1]	Transmit Data Delay After Serial Clock Falling Edge		10.5	12.5	ns
t_{SRCTDH}[1]	Transmit Data Hold After Serial Clock Falling Edge	2			ns

[1] The data, serial clock, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

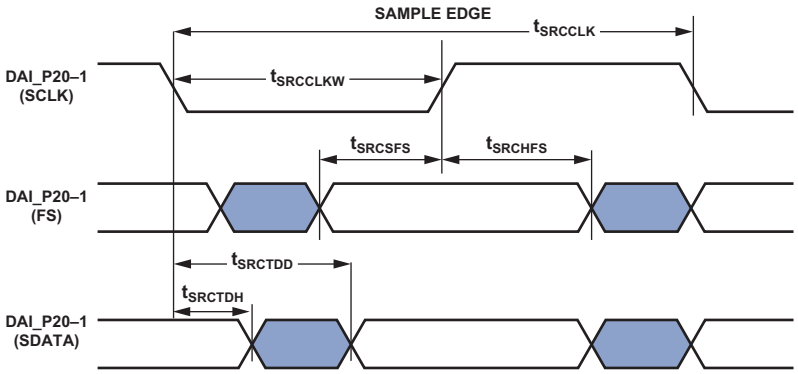


Figure 28. SRC Serial Output Port Timing

SPI Interface—Slave

Table 40. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$			ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$			ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$			ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge				
	CPHASE = 0	$2 \times t_{PCLK}$			ns
	CPHASE = 1	$2 \times t_{PCLK}$			ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$			ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2			ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2			ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$			ns
Switching Characteristics					
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	5	5	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	8	9	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	5	5.5	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	8.6	10	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	11.0	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$			ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, "Serial Peripheral Interface Port" chapter.

OUTPUT DRIVE CURRENTS

Figure 37 shows typical I-V characteristics for the output drivers of the processor. The curves represent the current drive capability of the output drivers as a function of output voltage.

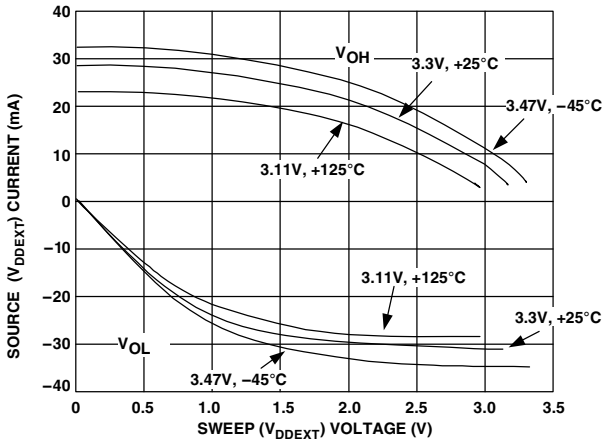


Figure 37. ADSP-2136x Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 12 on Page 20 through Table 41 on Page 45. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 38.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 39. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

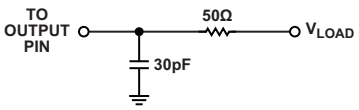


Figure 38. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

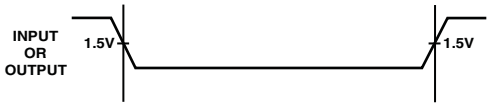


Figure 39. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 38). Figure 42 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 40, Figure 41, and Figure 42 may not be linear outside the ranges shown for Typical Output Delay versus Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) versus Load Capacitance.

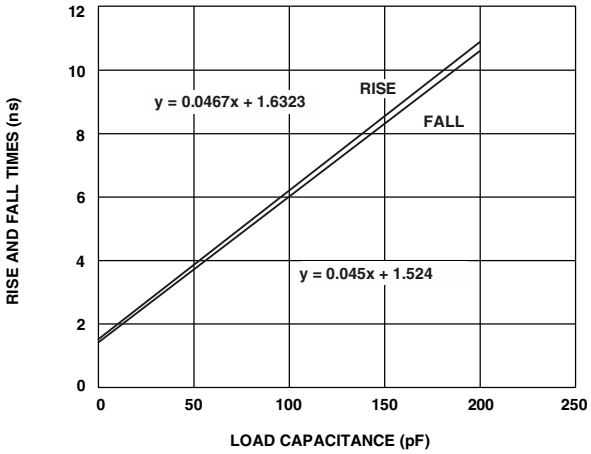


Figure 40. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

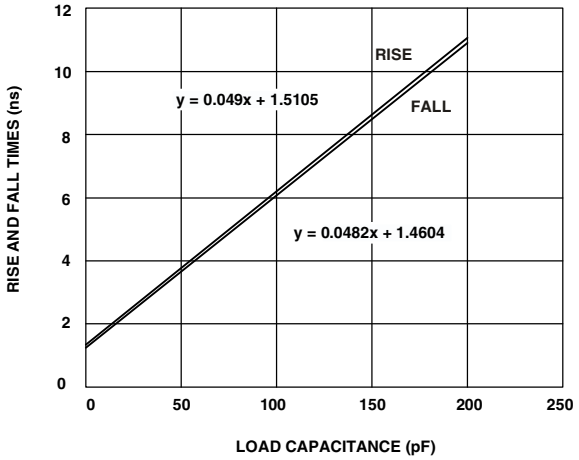


Figure 41. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

144-LEAD LQFP_EP PIN CONFIGURATIONS

The following table shows the processor's pin names and, when applicable, their default function after reset in parentheses.

Table 45. LQFP_EP Pin Assignments

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
V_{DDINT}	1	V_{DDINT}	37	V_{DDEXT}	73	GND	109
CLK_CFG0	2	GND	38	GND	74	V_{DDINT}	110
CLK_CFG1	3	$\overline{RD}$	39	V_{DDINT}	75	GND	111
BOOT_CFG0	4	ALE	40	GND	76	V_{DDINT}	112
BOOT_CFG1	5	AD15	41	DAI_P10 (SD2B)	77	GND	113
GND	6	AD14	42	DAI_P11 (SD3A)	78	V_{DDINT}	114
V_{DDEXT}	7	AD13	43	DAI_P12 (SD3B)	79	GND	115
GND	8	GND	44	DAI_P13 (SCLK3)	80	V_{DDEXT}	116
V_{DDINT}	9	V_{DDEXT}	45	DAI_P14 (SFS3)	81	GND	117
GND	10	AD12	46	DAI_P15 (SD4A)	82	V_{DDINT}	118
V_{DDINT}	11	V_{DDINT}	47	V_{DDINT}	83	GND	119
GND	12	GND	48	GND	84	V_{DDINT}	120
V_{DDINT}	13	AD11	49	GND	85	$\overline{RESET}$	121
GND	14	AD10	50	DAI_P16 (SD4B)	86	$\overline{SPIDS}$	122
FLAG0	15	AD9	51	DAI_P17 (SD5A)	87	GND	123
FLAG1	16	AD8	52	DAI_P18 (SD5B)	88	V_{DDINT}	124
AD7	17	DAI_P1 (SD0A)	53	DAI_P19 (SCLK5)	89	SPICLK	125
GND	18	V_{DDINT}	54	V_{DDINT}	90	MISO	126
V_{DDINT}	19	GND	55	GND	91	MOSI	127
GND	20	DAI_P2 (SD0B)	56	GND	92	GND	128
V_{DDEXT}	21	DAI_P3 (SCLK0)	57	V_{DDEXT}	93	V_{DDINT}	129
GND	22	GND	58	DAI_P20 (SFS5)	94	V_{DDEXT}	130
V_{DDINT}	23	V_{DDEXT}	59	GND	95	A_{vdd}	131
AD6	24	V_{DDINT}	60	V_{DDINT}	96	A_{vss}	132
AD5	25	GND	61	FLAG2	97	GND	133
AD4	26	DAI_P4 (SFS0)	62	FLAG3	98	$\overline{RESETOUT}$	134
V_{DDINT}	27	DAI_P5 (SD1A)	63	V_{DDINT}	99	$\overline{EMU}$	135
GND	28	DAI_P6 (SD1B)	64	GND	100	TDO	136
AD3	29	DAI_P7 (SCLK1)	65	V_{DDINT}	101	TDI	137
AD2	30	V_{DDINT}	66	GND	102	$\overline{TRST}$	138
V_{DDEXT}	31	GND	67	V_{DDINT}	103	TCK	139
GND	32	V_{DDINT}	68	GND	104	TMS	140
AD1	33	GND	69	V_{DDINT}	105	GND	141
AD0	34	DAI_P8 (SFS1)	70	GND	106	CLKIN	142
$\overline{WR}$	35	DAI_P9 (SD2A)	71	V_{DDINT}	107	XTAL	143
V_{DDINT}	36	V_{DDINT}	72	V_{DDINT}	108	V_{DDEXT}	144
						GND	145*

*The ePAD is electrically connected to GND inside the chip (see Figure 43 and Figure 44), therefore connecting the pad to GND is optional. For better thermal performance the ePAD should be soldered to the board and thermally connected to the GND plane with vias.

136-BALL BGA PIN CONFIGURATIONS

The following table shows the processor's ball names and, when applicable, their default function after reset in parentheses.

Table 46. BGA Pin Assignments

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
CLK_CFG0	A01	CLK_CFG1	B01	BOOT_CFG1	C01	V_{DDINT}	D01
XTAL	A02	GND	B02	BOOT_CFG0	C02	GND	D02
TMS	A03	V_{DDEXT}	B03	GND	C03	GND	D04
TCK	A04	CLKIN	B04	GND	C12	GND	D05
TDI	A05	$\overline{TRST}$	B05	GND	C13	GND	D06
$\overline{RESETOUT}$	A06	A_{VSS}	B06	V_{DDINT}	C14	GND	D09
TDO	A07	A_{VDD}	B07			GND	D10
$\overline{EMU}$	A08	V_{DDEXT}	B08			GND	D11
MOSI	A09	SPICLK	B09			GND	D13
MISO	A10	$\overline{RESET}$	B10			V_{DDINT}	D14
$\overline{SPIDS}$	A11	V_{DDINT}	B11				
V_{DDINT}	A12	GND	B12				
GND	A13	GND	B13				
GND	A14	GND	B14				
V_{DDINT}	E01	FLAG1	F01	AD7	G01	AD6	H01
GND	E02	FLAG0	F02	V_{DDINT}	G02	V_{DDEXT}	H02
GND	E04	GND	F04	V_{DDEXT}	G13	DAI_P18 (SD5B)	H13
GND	E05	GND	F05	DAI_P19 (SCLK5)	G14	DAI_P17 (SD5A)	H14
GND	E06	GND	F06				
GND	E09	GND	F09				
GND	E10	GND	F10				
GND	E11	GND	F11				
GND	E13	FLAG2	F13				
FLAG3	E14	DAI_P20 (SFS5)	F14				

Table 46. BGA Pin Assignments (Continued)

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
AD5	J01	AD3	K01	AD2	L01	AD0	M01
AD4	J02	V_{DDINT}	K02	AD1	L02	$\overline{WR}$	M02
GND	J04	GND	K04	GND	L04	GND	M03
GND	J05	GND	K05	GND	L05	GND	M12
GND	J06	GND	K06	GND	L06	DAI_P12 (SD3B)	M13
GND	J09	GND	K09	GND	L09	DAI_P13 (SCLK3)	M14
GND	J10	GND	K10	GND	L10		
GND	J11	GND	K11	GND	L11		
V_{DDINT}	J13	GND	K13	GND	L13		
DAI_P16 (SD4B)	J14	DAI_P15 (SD4A)	K14	DAI_P14 (SFS3)	L14		
AD15	N01	AD14	P01				
ALE	N02	AD13	P02				
$\overline{RD}$	N03	AD12	P03				
V_{DDINT}	N04	AD11	P04				
V_{DDEXT}	N05	AD10	P05				
AD8	N06	AD9	P06				
V_{DDINT}	N07	DAI_P1 (SD0A)	P07				
DAI_P2 (SD0B)	N08	DAI_P3 (SCLK0)	P08				
V_{DDEXT}	N09	DAI_P5 (SD1A)	P09				
DAI_P4 (SFS0)	N10	DAI_P6 (SD1B)	P10				
V_{DDINT}	N11	DAI_P7 (SCLK1)	P11				
V_{DDINT}	N12	DAI_P8 (SFS1)	P12				
GND	N13	DAI_P9 (SD2A)	P13				
DAI_P10 (SD2B)	N14	DAI_P11 (SD3A)	P14				

Figure 45 and Figure 46 show BGA pin assignments from the bottom and top, respectively.

Note: Use the center block of ground pins to provide thermal pathways to your printed circuit board's ground plane.

AUTOMOTIVE PRODUCTS

Some ADSP-2136x models are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 48. Automotive Products

Model	Notes	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
AD21362WBBCZ1xx	2	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21362WBSWZ1xx	2	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21362WYSWZ2xx	2	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WBBCZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21363WBSWZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WYSWZ2xx		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WBBCZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21364WBSWZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WYSWZ2xx		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ1xxA	2, 3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ1xxF	2, 3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WYSWZ2xxA	2, 3, 4	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WBBCZ1xxA	3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21366WBSWZ1xxA	3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WYSWZ2xxA	3, 4	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 14 for junction temperature (T_J) specification which is the only temperature specification.

[2] License from DTLA required for these products.

[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/sharc.

[4] License from Dolby Laboratories, Inc., and Digital Theater Systems (DTS) required for these products.