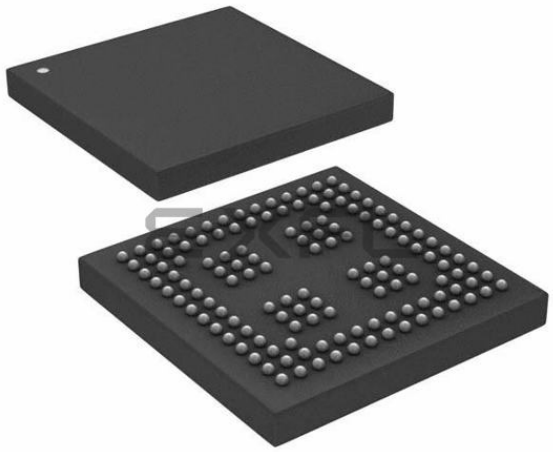

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, SPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	136-LFBGA, CSPBGA
Supplier Device Package	136-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21364bbcz-1aa

GENERAL DESCRIPTION

The ADSP-2136x SHARC® processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices, Inc., Super Harvard Architecture. The processor is source code-compatible with the ADSP-2126x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2136x are 32-/40-bit floating-point processors optimized for high performance automotive audio applications. They contain a large on-chip SRAM and ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital audio interface (DAI).

As shown in the functional block diagram on Page 1, the ADSP-2136x uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of signal processing algorithms. With its SIMD computational hardware, the ADSP-2136x can perform two GFLOPS running at 333 MHz.

Table 1 shows performance benchmarks for these devices. Table 2 shows the features of the individual product offerings.

Table 1. Benchmarks (at 333 MHz)

Benchmark Algorithm	Speed (at 333 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	27.9 µs
FIR Filter (per tap)[1]	1.5 ns
IIR Filter (per biquad)[1]	6.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	13.5 ns
[4×4] × [4×1]	23.9 ns
Divide (y/x)	10.5 ns
Inverse Square Root	16.3 ns

[1] Assumes two files in multichannel SIMD mode.

Table 2. ADSP-2136x Family Features

Feature	ADSP-21362	ADSP-21363	ADSP-21364	ADSP-21365	ADSP-21366
RAM	3M bit	3M bit	3M bit	3M bit	3M bit
ROM	4M bit	4M bit	4M bit	4M bit	4M bit
Audio Decoders in ROM[1]	No	No	No	Yes	Yes
Pulse-Width Modulation	Yes	Yes	Yes	Yes	Yes
S/PDIF	Yes	No	Yes	Yes	Yes
DTCP[2]	Yes	No	No	Yes	No
SRC SNR Performance	–128 dB	No SRC	–140 dB	–128 dB	–128 dB

[1] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Pro Logic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[2] The ADSP-21362 and ADSP-21365 processors provide the Digital Transmission Content Protection protocol, a proprietary security protocol. Contact your Analog Devices sales office for more information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-2136x processors. The core clock domain contains the following features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (3M bit)
- On-chip mask-programmable ROM (4M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints, which allow flexible exception handling.

The diagram on Page 1 also shows the following architectural features:

- I/O processor that handles 32-bit DMA for the peripherals
- Six full duplex serial ports
- Two SPI-compatible interface ports—primary on dedicated pins, secondary on DAI pins
- 8-bit or 16-bit parallel port that supports interfaces to off-chip memory peripherals
- Digital audio interface that includes two precision clock generators (PCG), an input data port with eight serial interfaces (IDP), an S/PDIF receiver/transmitter, 8-channel asynchronous sample rate converter (ASRC), DTCP cipher, six serial ports, a 20-bit parallel input data port (PDAP), 10 interrupts, six flag outputs, six flag inputs, three timers, and a flexible signal routing unit (SRU)

SHARC FAMILY CORE ARCHITECTURE

The ADSP-2136x is code-compatible at the assembly level with the ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2136x shares architectural features with the ADSP-2126x and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The processor contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY can be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive signal processing algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit, single-precision floating-point, 40-bit extended-precision floating-point, and 32-bit fixed-point data formats.

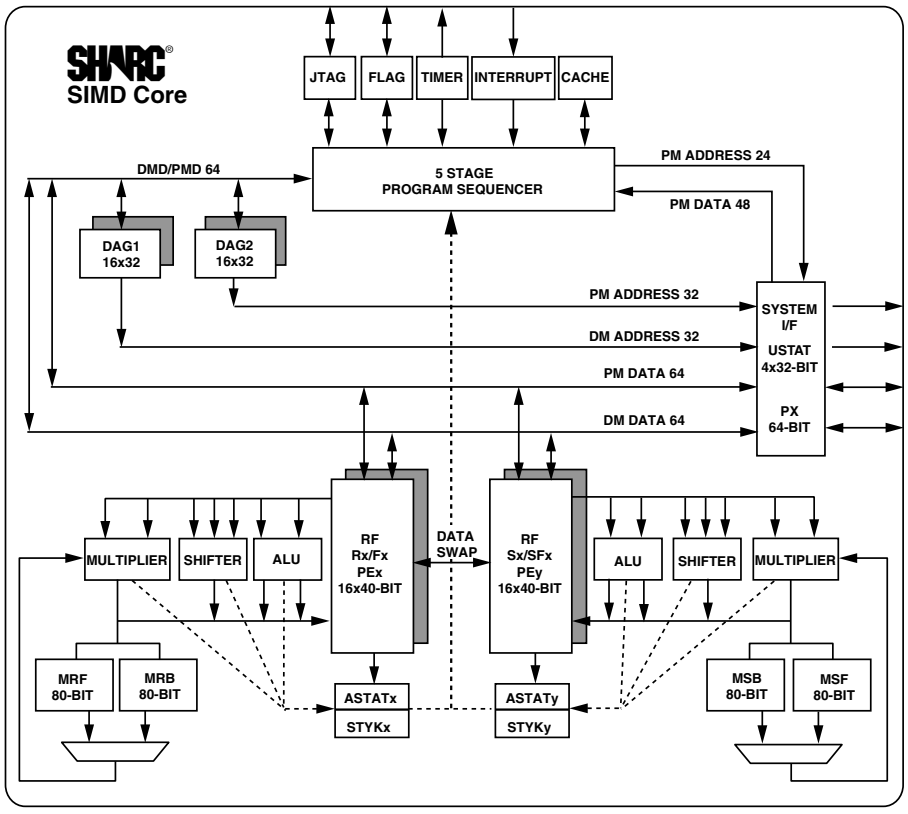


Figure 2. SHARC Core Block Diagram

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) files, combined with the ADSP-2136x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result register all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

Universal Registers

The universal registers are general purpose registers. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all system registers (control/status) of the core.

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

Timer

A core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Single-Cycle Fetch of Instruction and Four Operands

The processor features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With the its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The processor's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the processor can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

On-Chip Memory

The processor contains 3M bits of internal SRAM and 4M bits of internal ROM. Each block can be configured for different combinations of code and data storage (see Table 3). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The processor's memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

The SRAM can be configured as a maximum of 96K words of 32-bit data, 192K words of 16-bit data, 64K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 3M bits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

On-Chip Memory Bandwidth

The internal memory architecture allows three accesses at the same time to any of the four blocks, assuming no block conflicts. The total bandwidth is gained with DMD and PMD buses (2 × 64-bits, core CLK) and the IOD bus (32-bit, PCLK).

ROM-Based Security

The processor has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG

generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

Digital Audio Interface (DAI)

The digital audio interface (DAI) provides the ability to connect various peripherals to any of the DSP's DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU, shown in Figure 1).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI-associated peripherals for a wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes six serial ports, an S/PDIF receiver/transmitter, a DTCP cipher, a precision clock generator (PCG), eight channels of asynchronous sample rate converters, an input data port (IDP), an SPI port, six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2136x core, configurable as either eight channels of I^2S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports

The processor features six synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and a frame sync and they can operate at maximum $f_{PCLK}/4$. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Left-justified sample pair mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the transmitter can be formatted as left-justified, I^2S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

Digital Transmission Content Protection (DTCP)

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) is protected by this copy protection system. This feature is available on the ADSP-21362 and ADSP-21365 processors only. Licensing through DTLA is required for these products. Visit www.dtcp.com for more information.

Memory-to-Memory (MTM)

If the DTCP module is not used, the memory-to-memory DMA module allows internal memory copies for a standard DMA.

Synchronous/Asynchronous Sample Rate Converter (SRC)

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 140 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC is used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

The S/PDIF and SRC are not available on the ADSP-21363 models.

Input Data Port (IDP)

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive

audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of two units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A and B, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Peripheral Timers

The following three general-purpose timers can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

Each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

I/O PROCESSOR FEATURES

The processor's I/O provides many channels of DMA and controls the extensive set of peripherals described in the previous sections.

DMA Controller

The processor's on-chip DMA controllers allow data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the parallel port (PP). See Table 4.

Table 4. DMA Channels

Peripheral	ADSP-2136x
SPORTs	12
IDP/PDAP	8
SPI	2
MTM/DTCP	2
Parallel Port	1
Total DMA Channels	25

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the processor boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins in Table 5. Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Table 5. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port Boot via EPROM
11	No booting occurs. Processor executes from internal ROM after reset.

Phase-Locked Loop

The processors use an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK_CFG1–0 pins are used to select ratios of 32:1, 16:1, and 6:1. After booting, numerous other ratios can be selected via software control.

The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 1, 2, 4, and 8.

Power Supplies

The processor has a separate power supply connection for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2 V requirement for K, B, and Y grade models, and the 1.0 V requirement for Y models. (For information on the temperature ranges offered for this product, see Operating Conditions on Page 14, Package Information on Page 16, and Ordering Guide on Page 56.) The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 3. (A recommended ferrite chip is the muRata BLM18AG102SN1D.) To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 3 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the processor's architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference* and the *ADSP-2136x SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Power-Up Sequencing

The timing requirements for processor startup are given in Table 10. Note that during power-up, when the V_{DDINT} power supply comes up after V_{DDEXT}, a leakage current of the order of three-state leakage current pull-up, pull-down, may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the V_{DDINT} rail has powered up.

Table 10. Power-Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds, depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{\text{RESET}}$ to be held low to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{SRST} specification in Table 12. If setup time is not met, 1 additional CLKIN cycle can be added to the core reset time, resulting in 4097 cycles maximum.

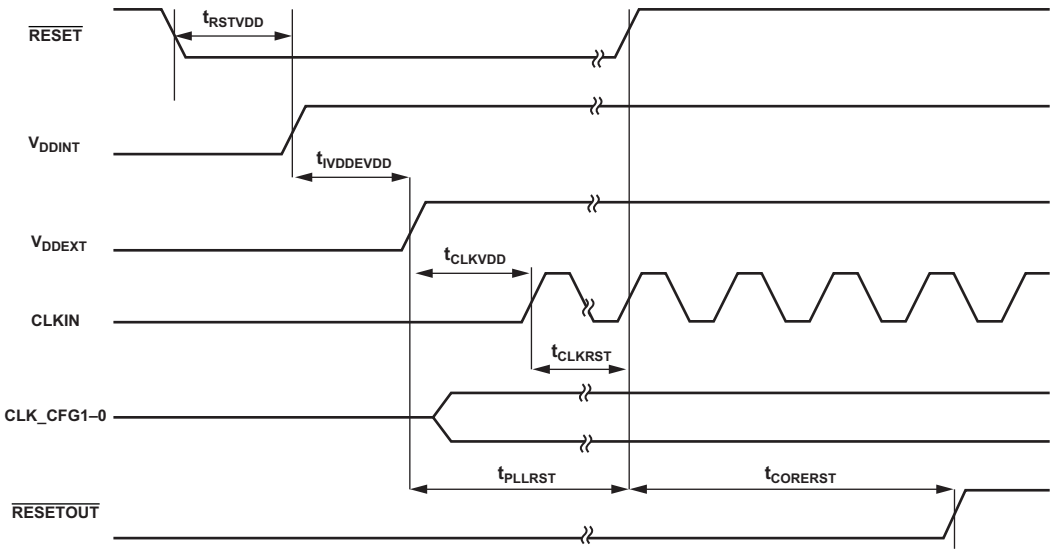


Figure 6. Power-Up Sequencing

Clock Input

Table 11. Clock Input

Parameter		200 MHz[1]		333 MHz[2]		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{CK}	CLKIN Period	30[3]	100	18	100	ns
t_{CKL}	CLKIN Width Low	12.5		7.5		ns
t_{CKH}	CLKIN Width High	12.5		7.5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3	ns
t_{CCLK}[4]	CCLK Period	5.0	10	3.0	10	ns
t_{VCO}[5]	VCO Frequency	200	600	200	800	MHz
t_{CKJ}[6, 7]	CLKIN Jitter Tolerance	–250	+250	–250	+250	ps

[1] Applies to all 200 MHz models. See Ordering Guide on Page 56.
[2] Applies to all 333 MHz models. See Ordering Guide on Page 56.
[3] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in the PMCTL register.
[4] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[5] See Figure 5 on Page 17 for VCO diagram.
[6] Actual input jitter should be combined with AC specifications for accurate timing analysis.
[7] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

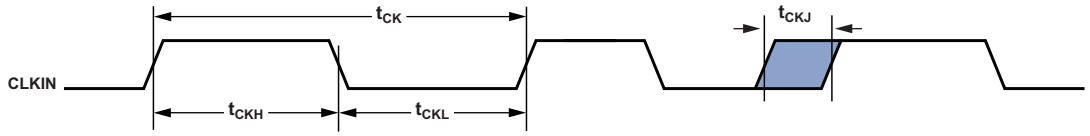


Figure 7. Clock Input

Clock Signals

The processor can use an external clock or a crystal. Refer to the CLKIN pin description in Table 6 on Page 11. The user application program can configure the processor to use its internal clock generator by connecting the necessary components to the CLKIN and XTAL pins. Figure 8 shows the component connections used for a fundamental frequency crystal operating in parallel mode.

Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1. (CCLK:CLKIN achieves a clock speed of 266.72 MHz.) To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

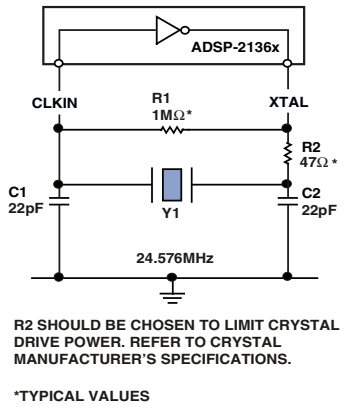


Figure 8. Recommended Circuit for Fundamental Mode Crystal Operation

Timer WDTH_CAP Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specification provided below are valid at the DAI_P20–1 pins.

Table 16. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

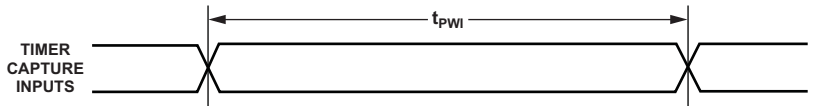


Figure 13. Timer Width Capture Timing

DAI Pin to Pin Direct Routing

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 17. DAI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	10	ns

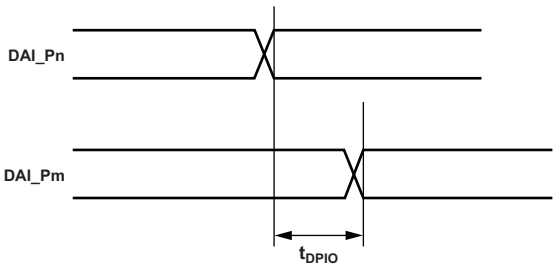


Figure 14. DAI Pin to Pin Direct Routing

Flags

The timing specifications provided below apply to the FLAG3–0 and DAI_P20–1 pins, the parallel port, and the serial peripheral interface (SPI). See Table 6 on Page 11 for more information on flag use.

Table 19. Flags

Parameter		Min	Unit
Timing Requirement			
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$	ns
Switching Characteristic			
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1$	ns

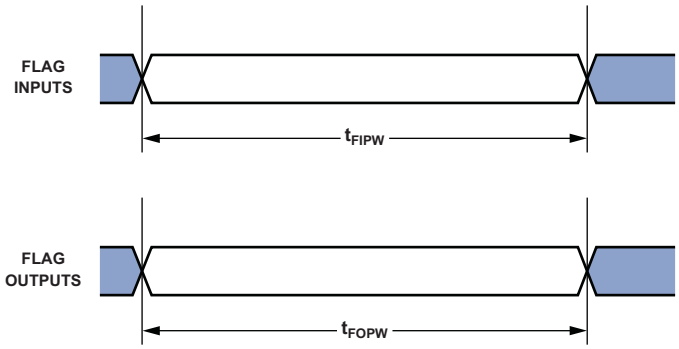


Figure 16. Flags

Memory Read—Parallel Port

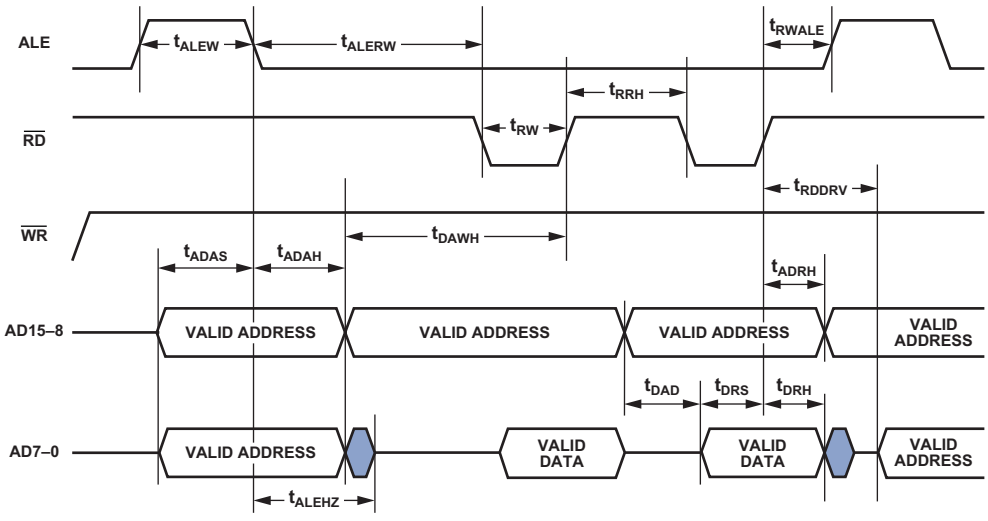
Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the processor is accessing external memory space.

Table 20. 8-Bit Memory Read Cycle

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{DRS}	AD7–0 Data Setup Before $\overline{RD}$ High	3.3		4.5		ns
t_{DRH}	AD7–0 Data Hold After $\overline{RD}$ High	0		0		ns
t_{DAD}	AD15–8 Address to AD7–0 Data Valid		D + t_{PCLK} – 5.0		D + t_{PCLK} – 5.0	ns
Switching Characteristics						
t_{ALEW}	ALE Pulse Width	2 × t_{PCLK} – 2.0		2 × t_{PCLK} – 2.0		ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	t_{PCLK} – 2.5		t_{PCLK} – 2.5		ns
t_{RRH}	Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge	H + t_{PCLK} – 1.4		H + t_{PCLK} – 1.4		ns
t_{ALERW}	ALE Deasserted to Read Asserted	2 × t_{PCLK} – 3.8		2 × t_{PCLK} – 3.8		ns
t_{RWALE}	Read Deasserted to ALE Asserted	F + H + 0.5		F + H + 0.5		ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	t_{PCLK} – 2.3		t_{PCLK} – 2.3		ns
t_{ALEHZ}[1]	ALE Deasserted to AD7–0 Address in High-Z	t_{PCLK}	t_{PCLK} + 3.0	t_{PCLK}	t_{PCLK} + 3.8	ns
t_{RW}	$\overline{RD}$ Pulse Width	D – 2.0		D – 2.0		ns
t_{RDDRV}	AD7–0 ALE Address Drive After Read High	F + H + t_{PCLK} – 2.3		F + H + t_{PCLK} – 2.3		ns
t_{ADRH}	AD15–8 Address Hold After $\overline{RD}$ High	H		H		ns
t_{DAWH}	AD15–8 Address to $\overline{RD}$ High	D + t_{PCLK} – 4.0		D + t_{PCLK} – 4.0		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}
H = t_{PCLK} (if a hold cycle is specified, else H = 0)
F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.



NOTE: MEMORY READS ALWAYS OCCUR IN GROUPS OF FOUR BETWEEN ALE CYCLES. THIS FIGURE SHOWS ONLY TWO MEMORY READS TO PROVIDE THE NECESSARY TIMING INFORMATION.

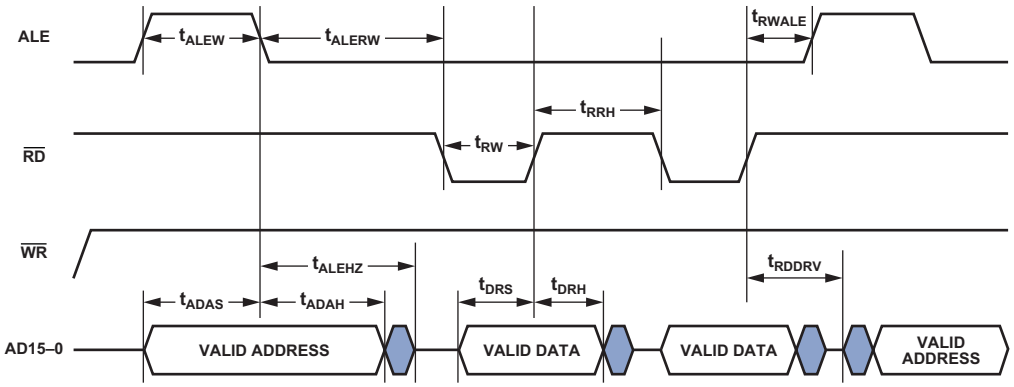
Figure 17. Read Cycle for 8-Bit Memory Timing

Table 21. 16-Bit Memory Read Cycle

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{DRS}	AD15–0 Data Setup Before $\overline{RD}$ High	3.3		4.5		ns
t_{DRH}	AD15–0 Data Hold After $\overline{RD}$ High	0		0		ns
Switching Characteristics						
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$		$2 \times t_{PCLK} - 2.0$		ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$		$t_{PCLK} - 2.5$		ns
t_{ALERW}	ALE Deasserted to Read Asserted	$2 \times t_{PCLK} - 3.8$		$2 \times t_{PCLK} - 3.8$		ns
t_{RRH}[2]	Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge	$H + t_{PCLK} - 1.4$		$H + t_{PCLK} - 1.4$		ns
t_{RWALE}	Read Deasserted to ALE Asserted	$F + H + 0.5$		$F + H + 0.5$		ns
t_{RDDRV}	ALE Address Drive After Read High	$F + H + t_{PCLK} - 2.3$		$F + H + t_{PCLK} - 2.3$		ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$		$t_{PCLK} - 2.3$		ns
t_{ALEHZ1}	ALE Deasserted to Address/Data15–0 in High-Z	t_{PCLK}	$t_{PCLK} + 3.0$	t_{PCLK}	$t_{PCLK} + 3.8$	ns
t_{RW}	$\overline{RD}$ Pulse Width	$D - 2.0$		$D - 2.0$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) $\times t_{PCLK}$
$H = t_{PCLK}$ (if a hold cycle is specified, else $H = 0$)
$F = 7 \times t_{PCLK}$ (if FLASH_MODE is set, else $F = 0$)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY READS, WHEN EMPP ≠ 0, ONLY ONE $\overline{RD}$ PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE $\overline{RD}$ PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 18. Read Cycle for 16-Bit Memory Timing

Memory Write—Parallel Port

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the processor is accessing external memory space.

Table 22. 8-Bit Memory Write Cycle

Parameter		K and B Grade Min	Y Grade Min	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$	$2 \times t_{PCLK} - 2.0$	ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.8$	$t_{PCLK} - 2.8$	ns
t_{ALERW}	ALE Deasserted to Write Asserted	$2 \times t_{PCLK} - 3.8$	$2 \times t_{PCLK} - 3.8$	ns
t_{RWALE}	Write Deasserted to ALE Asserted	H + 0.5	H + 0.5	ns
t_{WRH}	Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge	$F + H + t_{PCLK} - 2.3$	$F + H + t_{PCLK} - 2.3$	ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 0.5$	$t_{PCLK} - 0.5$	ns
t_{WW}	$\overline{WR}$ Pulse Width	D – F – 2.0	D – F – 2.0	ns
t_{ADWL}	AD15–8 Address to $\overline{WR}$ Low	$t_{PCLK} - 2.8$	$t_{PCLK} - 3.5$	ns
t_{ADWH}	AD15–8 Address Hold After $\overline{WR}$ High	H	H	ns
t_{DWS}	AD7–0 Data Setup Before $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns
t_{DWH}	AD7–0 Data Hold After $\overline{WR}$ High	H	H	ns
t_{DAWH}	AD15–8 Address to $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}.
H = t_{PCLK} (if a hold cycle is specified, else H = 0)
F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0). If FLASH_MODE is set, D must be ≥ 9 × t_{PCLK}.

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.

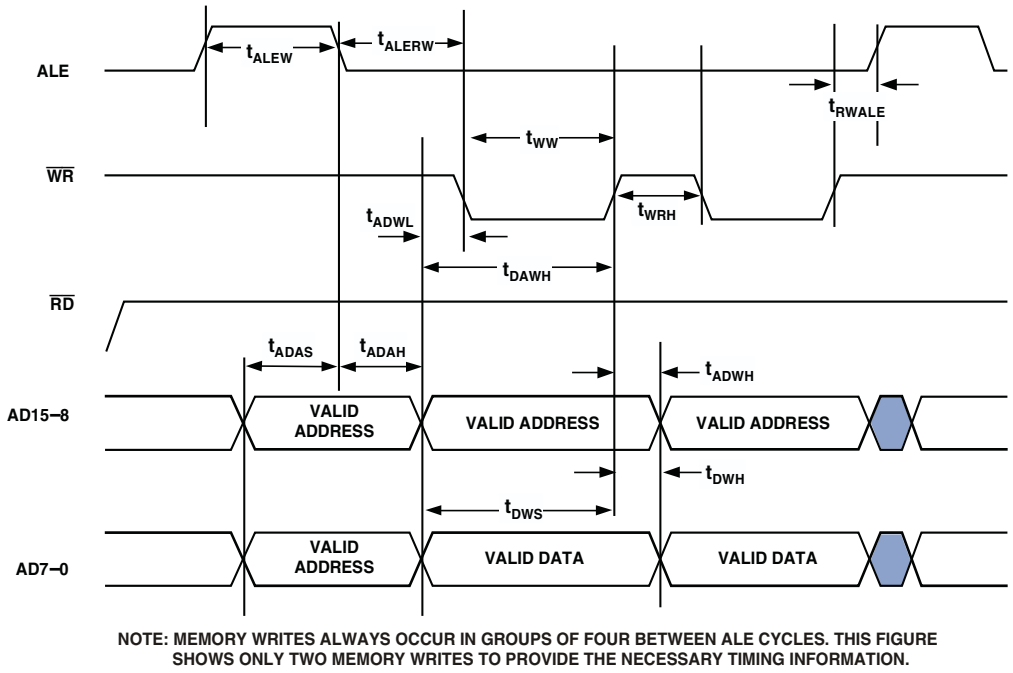


Figure 19. Write Cycle for 8-Bit Memory Timing

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync (FS) delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 24. Serial Ports—External Clock

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	2.5			ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5			ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 2$			ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$			ns
Switching Characteristics					
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)		9.5	11	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)	2			ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		9.5	11	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2			ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 25. Serial Ports—Internal Clock

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	7			ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5			ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7			ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5			ns
Switching Characteristics					
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		3	3.5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0			ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		8	9.5	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0			ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3	4.0	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0			ns
t_{SCLKIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 2$	$2 \times t_{PCLK} + 2$	$2 \times t_{PCLK} + 2$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

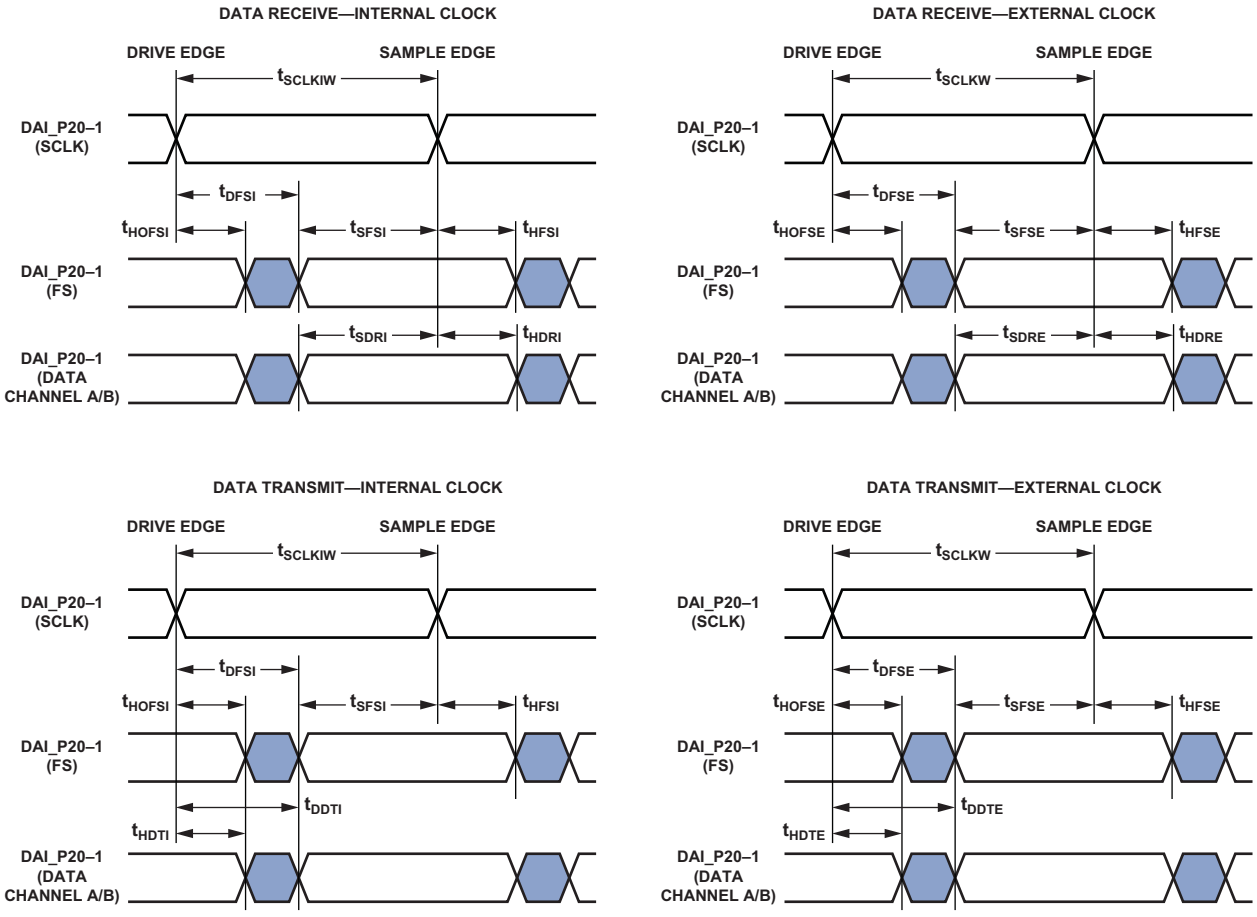


Figure 21. Serial Ports

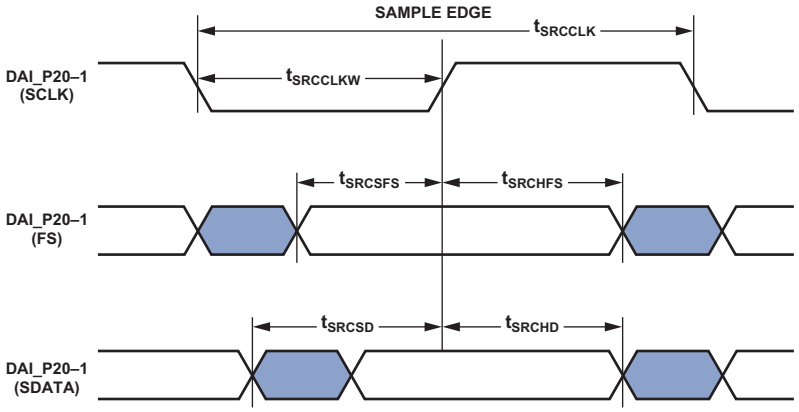


Figure 27. SRC Serial Input Port Timing

Figure 30 shows the default I²S-justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

Table 34. S/PDIF Transmitter I²S Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{I2SD}	FS to MSB Delay in I²S Mode	1	SCLK

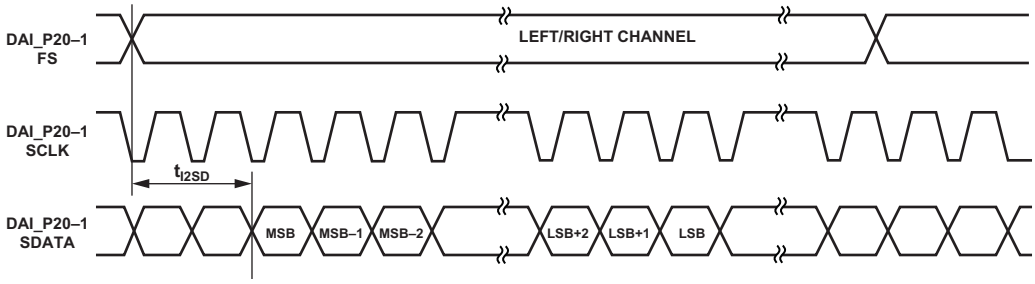


Figure 30. I²S-Justified Mode

Figure 31 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

Table 35. S/PDIF Transmitter Left-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{LJD}	FS to MSB Delay in Left-Justified Mode	0	SCLK

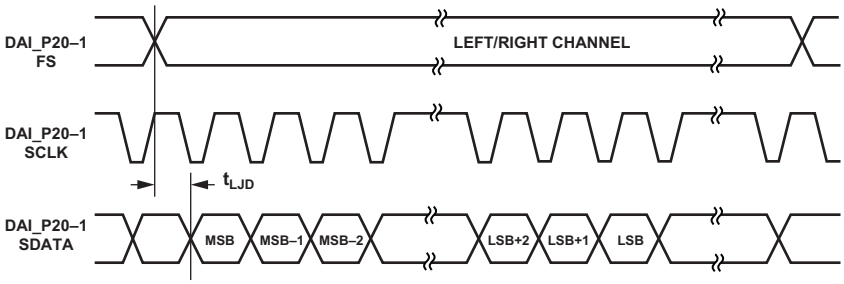


Figure 31. Left-Justified Mode

136-BALL BGA PIN CONFIGURATIONS

The following table shows the processor's ball names and, when applicable, their default function after reset in parentheses.

Table 46. BGA Pin Assignments

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
CLK_CFG0	A01	CLK_CFG1	B01	BOOT_CFG1	C01	V_{DDINT}	D01
XTAL	A02	GND	B02	BOOT_CFG0	C02	GND	D02
TMS	A03	V_{DDEXT}	B03	GND	C03	GND	D04
TCK	A04	CLKIN	B04	GND	C12	GND	D05
TDI	A05	$\overline{TRST}$	B05	GND	C13	GND	D06
$\overline{RESETOUT}$	A06	A_{VSS}	B06	V_{DDINT}	C14	GND	D09
TDO	A07	A_{VDD}	B07			GND	D10
$\overline{EMU}$	A08	V_{DDEXT}	B08			GND	D11
MOSI	A09	SPICLK	B09			GND	D13
MISO	A10	$\overline{RESET}$	B10			V_{DDINT}	D14
$\overline{SPIDS}$	A11	V_{DDINT}	B11				
V_{DDINT}	A12	GND	B12				
GND	A13	GND	B13				
GND	A14	GND	B14				
V_{DDINT}	E01	FLAG1	F01	AD7	G01	AD6	H01
GND	E02	FLAG0	F02	V_{DDINT}	G02	V_{DDEXT}	H02
GND	E04	GND	F04	V_{DDEXT}	G13	DAI_P18 (SD5B)	H13
GND	E05	GND	F05	DAI_P19 (SCLK5)	G14	DAI_P17 (SD5A)	H14
GND	E06	GND	F06				
GND	E09	GND	F09				
GND	E10	GND	F10				
GND	E11	GND	F11				
GND	E13	FLAG2	F13				
FLAG3	E14	DAI_P20 (SFS5)	F14				

Table 46. BGA Pin Assignments (Continued)

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
AD5	J01	AD3	K01	AD2	L01	AD0	M01
AD4	J02	V_{DDINT}	K02	AD1	L02	$\overline{WR}$	M02
GND	J04	GND	K04	GND	L04	GND	M03
GND	J05	GND	K05	GND	L05	GND	M12
GND	J06	GND	K06	GND	L06	DAI_P12 (SD3B)	M13
GND	J09	GND	K09	GND	L09	DAI_P13 (SCLK3)	M14
GND	J10	GND	K10	GND	L10		
GND	J11	GND	K11	GND	L11		
V_{DDINT}	J13	GND	K13	GND	L13		
DAI_P16 (SD4B)	J14	DAI_P15 (SD4A)	K14	DAI_P14 (SFS3)	L14		
AD15	N01	AD14	P01				
ALE	N02	AD13	P02				
$\overline{RD}$	N03	AD12	P03				
V_{DDINT}	N04	AD11	P04				
V_{DDEXT}	N05	AD10	P05				
AD8	N06	AD9	P06				
V_{DDINT}	N07	DAI_P1 (SD0A)	P07				
DAI_P2 (SD0B)	N08	DAI_P3 (SCLK0)	P08				
V_{DDEXT}	N09	DAI_P5 (SD1A)	P09				
DAI_P4 (SFS0)	N10	DAI_P6 (SD1B)	P10				
V_{DDINT}	N11	DAI_P7 (SCLK1)	P11				
V_{DDINT}	N12	DAI_P8 (SFS1)	P12				
GND	N13	DAI_P9 (SD2A)	P13				
DAI_P10 (SD2B)	N14	DAI_P11 (SD3A)	P14				

Figure 45 and Figure 46 show BGA pin assignments from the bottom and top, respectively.

Note: Use the center block of ground pins to provide thermal pathways to your printed circuit board's ground plane.