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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, SPI
Clock Rate	333MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-LQFP-EP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21364kswz-1aa

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GENERAL DESCRIPTION

The ADSP-2136x SHARC® processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices, Inc., Super Harvard Architecture. The processor is source code-compatible with the ADSP-2126x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2136x are 32-/40-bit floating-point processors optimized for high performance automotive audio applications. They contain a large on-chip SRAM and ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital audio interface (DAI).

As shown in the functional block diagram on Page 1, the ADSP-2136x uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of signal processing algorithms. With its SIMD computational hardware, the ADSP-2136x can perform two GFLOPS running at 333 MHz.

Table 1 shows performance benchmarks for these devices. Table 2 shows the features of the individual product offerings.

Table 1. Benchmarks (at 333 MHz)

Benchmark Algorithm	Speed (at 333 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	27.9 µs
FIR Filter (per tap)[1]	1.5 ns
IIR Filter (per biquad)[1]	6.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	13.5 ns
[4×4] × [4×1]	23.9 ns
Divide (y/x)	10.5 ns
Inverse Square Root	16.3 ns

[1] Assumes two files in multichannel SIMD mode.

Table 2. ADSP-2136x Family Features

Feature	ADSP-21362	ADSP-21363	ADSP-21364	ADSP-21365	ADSP-21366
RAM	3M bit	3M bit	3M bit	3M bit	3M bit
ROM	4M bit	4M bit	4M bit	4M bit	4M bit
Audio Decoders in ROM[1]	No	No	No	Yes	Yes
Pulse-Width Modulation	Yes	Yes	Yes	Yes	Yes
S/PDIF	Yes	No	Yes	Yes	Yes
DTCP[2]	Yes	No	No	Yes	No
SRC SNR Performance	–128 dB	No SRC	–140 dB	–128 dB	–128 dB

[1] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Pro Logic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[2] The ADSP-21362 and ADSP-21365 processors provide the Digital Transmission Content Protection protocol, a proprietary security protocol. Contact your Analog Devices sales office for more information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-2136x processors. The core clock domain contains the following features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (3M bit)
- On-chip mask-programmable ROM (4M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints, which allow flexible exception handling.

The diagram on Page 1 also shows the following architectural features:

- I/O processor that handles 32-bit DMA for the peripherals
- Six full duplex serial ports
- Two SPI-compatible interface ports—primary on dedicated pins, secondary on DAI pins
- 8-bit or 16-bit parallel port that supports interfaces to off-chip memory peripherals
- Digital audio interface that includes two precision clock generators (PCG), an input data port with eight serial interfaces (IDP), an S/PDIF receiver/transmitter, 8-channel asynchronous sample rate converter (ASRC), DTCP cipher, six serial ports, a 20-bit parallel input data port (PDAP), 10 interrupts, six flag outputs, six flag inputs, three timers, and a flexible signal routing unit (SRU)

Table 3. ADSP-2136x Internal Memory Space

IOP Registers 0x0000 0000–0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM 0x0004 0000–0x0004 7FFF	Block 0 ROM 0x0008 0000–0x0008 AAA9	Block 0 ROM 0x0008 0000–0x0008 FFFF	Block 0 ROM 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 BFFF		Reserved 0x0009 0000–0x0009 7FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 C000–0x0004 FFFF	Block 0 SRAM 0x0009 0000–0x0009 5554	Block 0 SRAM 0x0009 8000–0x0009 FFFF	Block 0 SRAM 0x0013 0000–0x0013 FFFF
Block 1 ROM 0x0005 0000–0x0005 7FFF	Block 1 ROM 0x000A 0000–0x000A AAA9	Block 1 ROM 0x000A 0000–0x000A FFFF	Block 1 ROM 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 BFFF		Reserved 0x000B 0000–0x000B 7FFF	Reserved 0x0016 0000–0x0016 FFFF
Block 1 SRAM 0x0005 C000–0x0005 FFFF	Block 1 SRAM 0x000B 0000–0x000B 5554	Block 1 SRAM 0x000B 8000–0x000B FFFF	Block 1 SRAM 0x0017 0000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000–0x0006 FFFF		Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF		Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF
			Reserved 0x0020 0000–0xFFFF FFFF

or test access port, is assigned to each customer. The device ignores a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2136x family contains a rich set of peripherals that support a wide variety of applications, including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, monitor control, imaging, and other applications.

Parallel Port

The parallel port provides interfaces to SRAM and peripheral devices. The multiplexed address and data pins (AD15–0) can access 8-bit devices with up to 24 bits of address, or 16-bit devices with up to 16 bits of address. In either mode, 8-bit or 16-bit, the maximum data transfer rate is $f_{PCLK}/4$.

DMA transfers are used to move data to and from internal memory. Access to the core is also facilitated through the parallel port register read/write functions. The $\overline{RD}$, $\overline{WR}$, and ALE (address latch enable) pins are the control pins for the parallel port.

Serial Peripheral (Compatible) Interface

The processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the processor's SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes and can operate at a maximum baud rate of $f_{PCLK}/4$.

The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-2136x SPI-compatible peripheral implementation also features programmable baud rate, clock phase, and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

Pulse-Width Modulation

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can

audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of two units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A and B, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Peripheral Timers

The following three general-purpose timers can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

Each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

I/O PROCESSOR FEATURES

The processor's I/O provides many channels of DMA and controls the extensive set of peripherals described in the previous sections.

DMA Controller

The processor's on-chip DMA controllers allow data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the parallel port (PP). See Table 4.

Table 4. DMA Channels

Peripheral	ADSP-2136x
SPORTs	12
IDP/PDAP	8
SPI	2
MTM/DTCP	2
Parallel Port	1
Total DMA Channels	25

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the processor boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins in Table 5. Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Table 5. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port Boot via EPROM
11	No booting occurs. Processor executes from internal ROM after reset.

Phase-Locked Loop

The processors use an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK_CFG1–0 pins are used to select ratios of 32:1, 16:1, and 6:1. After booting, numerous other ratios can be selected via software control.

The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 1, 2, 4, and 8.

Power Supplies

The processor has a separate power supply connection for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2 V requirement for K, B, and Y grade models, and the 1.0 V requirement for Y models. (For information on the temperature ranges offered for this product, see Operating Conditions on Page 14, Package Information on Page 16, and Ordering Guide on Page 56.) The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 3. (A recommended ferrite chip is the muRata BLM18AG102SN1D.) To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 3 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
SPICLK	I/O (pu)	Three-state with pull-up enabled, driven high in SPI-master boot mode	**Serial Peripheral Interface Clock Signal.** Driven by the master, this signal controls the rate at which data is transferred. The master can transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (high). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{SPIDS}}$	I	Input only	**Serial Peripheral Interface Slave Device Select.** An active low signal used to select the processor as an SPI slave device. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode the processor's $\overline{\text{SPIDS}}$ signal can be driven by a slave device to signal to the processor (as SPI master) that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where flag pins are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For processor to processor SPI interaction, any of the master processor's flag pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the SPI slave device.
MOSI	I/O (O/D) (pu)	Three-state with pull-up enabled, driven low in SPI-master boot mode	**SPI Master Out Slave In.** If the ADSP-2136x is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the processor is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has a 22.5 kΩ internal pull-up resistor.
MISO	I/O (O/D) (pu)	Three-state with pull-up enabled	**SPI Master In Slave Out.** If the ADSP-2136x is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the processor is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has a 22.5 kΩ internal pull-up resistor. MISO can be configured as O/D by setting the OPD bit in the SPICTL register. **Note:** *Only one slave is allowed to transmit data at any given time.* To enable broadcast transmission to multiple SPI slaves, the processor's MISO pin can be disabled by setting Bit 5 (DMISO) of the SPICTL register equal to 1.
CLKIN	I	Input only	**Local Clock In.** Used in conjunction with XTAL. CLKIN is the ADSP-2136x clock input. It configures the ADSP-2136x to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. The core is clocked either by the PLL output or this clock input depending on the CLK_CFG1–0 pin settings. CLKIN should not be halted, changed, or operated below the specified frequency.
XTAL	O	Output only[2]	**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
CLK_CFG1–0	I	Input only	**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are: 00 = 6:1 01 = 32:1 10 = 16:1 11 = reserved.

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
BOOT_CFG1–0	I	Input only	**Boot Configuration Select.** This pin is used to select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. For a description of the boot mode, refer to Table 5, Boot Mode Selection.
$\overline{\text{RESETOUT}}$	O	Output only	**Reset Out.** Drives out the core reset signal to an external device.
$\overline{\text{RESET}}$	I/A	Input only	**Processor Reset.** Resets the ADSP-2136x to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Input only[3]	**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the processors.
TMS	I/S (pu)	Three-state with pull-up enabled	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TDI	I/S (pu)	Three-state with pull-up enabled	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 k internal pull-up resistor.
TDO	O	Three-state[4]	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A (pu)	Three-state with pull-up enabled	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2136x. $\overline{\text{TRST}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D) (pu)	Three-state with pull-up enabled	**Emulation Status.** Must be connected to the processor's JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 kΩ internal pull-up resistor.
V_{DDINT}	P		**Core Power Supply.** Supplies the processor's core.
V_{DDEXT}	P		**I/O Power Supply.**
A_{VDD}	P		**Analog Power Supply.** Supplies the processor's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 8.
A_{VSS}	G		**Analog Power Supply Return.**
GND	G		**Power Supply Return.**

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

[1] $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE are three-stated (and not driven) only when $\overline{\text{RESET}}$ is active.
[2] Output only is a three-state driver with its output path always enabled.
[3] Input only is a three-state driver with both output path and pull-up disabled.
[4] Three-state is a three-state driver with pull-up disabled.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[2]	2.4		V
V_{OL}[1]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[2]		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU}[4]	Low Level Input Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
I_{OZH}[5, 6]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU}[6]	Three-State Leakage Current Pull-Up	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$[7, 8]	Supply Current (Internal)	t_{CCLK} = Min, V_{DDINT} = Nom		800	mA
I_{AVDD}[9]	Supply Current (Analog)	A_{VDD} = Max		10	mA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.2 V		4.7	pF

[1] Applies to output and bidirectional pins: AD15–0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{EMU}$, TDO, and XTAL.
[2] See Output Drive Currents on Page 46 for typical drive current capabilities.
[3] Applies to input pins: $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, and CLKIN.
[4] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[5] Applies to three-stateable pins: FLAG3–0.
[6] Applies to three-stateable pins with 22.5 kΩ pull-ups: AD15–0, DAI_Px, SPICLK, $\overline{EMU}$, $\overline{MISO}$, and $\overline{MOSI}$.
[7] Typical internal current data reflects nominal operating conditions.
[8] See the Engineer-to-Engineer Note *"Estimating Power for the ADSP-21362 SHARC Processors"* (EE-277) for further information.
[9] Characterized, but not tested.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 4 provides details about the package branding for the ADSP-2136x processor. For a complete listing of product availability, see Ordering Guide on Page 56.

Figure 4. Typical Package Brand

Table 7. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See the Engineer-to-Engineer Note *"Estimating Power for the ADSP-21362 SHARC Processors"* (EE-277) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 47.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 8 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. For voltage reference levels, see Figure 39 on Page 46 under Test Conditions.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 5). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 11.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 10. Note that during power-up, when the V_{DDINT} power supply comes up after V_{DDEXT}, a leakage current of the order of three-state leakage current pull-up, pull-down, may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the V_{DDINT} rail has powered up.

Table 10. Power-Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds, depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{\text{RESET}}$ to be held low to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{SRST} specification in Table 12. If setup time is not met, 1 additional CLKIN cycle can be added to the core reset time, resulting in 4097 cycles maximum.

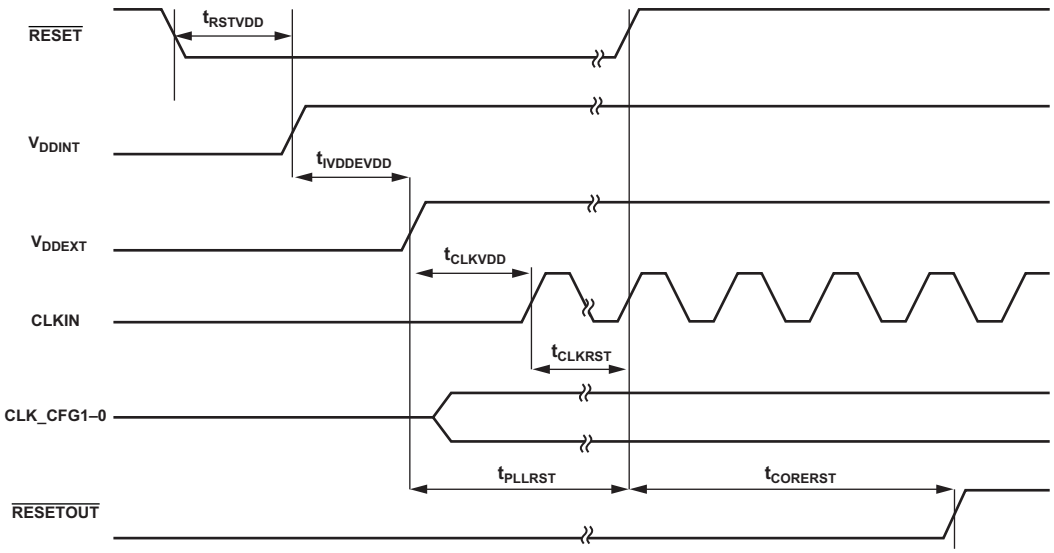


Figure 6. Power-Up Sequencing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 through DAI_P20).

Table 18. Precision Clock Generator (Direct Pin Routing)

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$			ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5			ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3			ns
Switching Characteristics					
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	$12 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	$12 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOP}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$			ns

D = FSxDIV, PH = FSxPHASE. For more information, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, "Precision Clock Generators" chapter.

[1] In normal mode, t_{PCGOP} (min) = $2 \times t_{PCGIP}$.

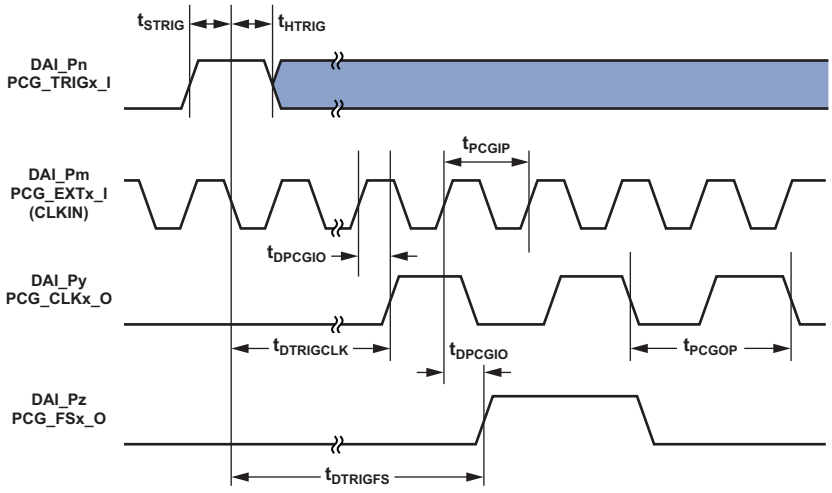


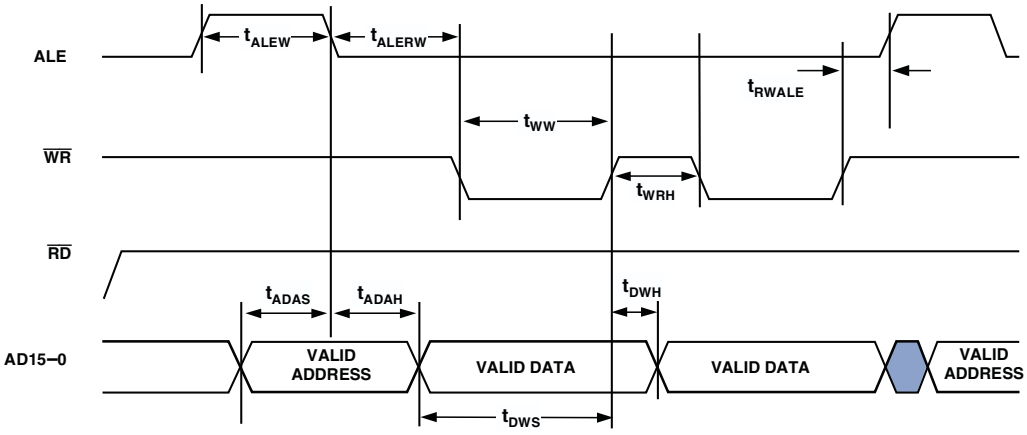
Figure 15. Precision Clock Generator (Direct Pin Routing)

Table 23. 16-Bit Memory Write Cycle

Parameter		K and B Grade Min	Y Grade Min	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$	$2 \times t_{PCLK} - 2.0$	ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$	$t_{PCLK} - 2.5$	ns
t_{ALERW}	ALE Deasserted to Write Asserted	$2 \times t_{PCLK} - 3.8$	$2 \times t_{PCLK} - 3.8$	ns
t_{RWALE}	Write Deasserted to ALE Asserted	H + 0.5	H + 0.5	ns
t_{WRH}[2]	Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge	$F + H + t_{PCLK} - 2.3$	$F + H + t_{PCLK} - 2.3$	ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$	$t_{PCLK} - 2.3$	ns
t_{WW}	$\overline{WR}$ Pulse Width	D – F – 2.0	D – F – 2.0	ns
t_{DWS}	AD15–0 Data Setup Before $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns
t_{DWH}	AD15–0 Data Hold After $\overline{WR}$ High	H	H	ns

D = (the value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}.
H = t_{PCLK} (if a hold cycle is specified, else H = 0)
F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0). If FLASH_MODE is set, D must be ≥ 9 × t_{PCLK}.
t_{PCLK} = (peripheral) clock period = 2 × t_{CCLK}

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY WRITES, WHEN EMPP ≠ 0, ONLY ONE $\overline{WR}$ PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE $\overline{WR}$ PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 20. Write Cycle for 16-Bit Memory Timing

Pulse-Width Modulation Generators

Table 30. PWM Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

[1] Note that the PWM output signals are shared on the parallel port bus (AD15-0 pins).

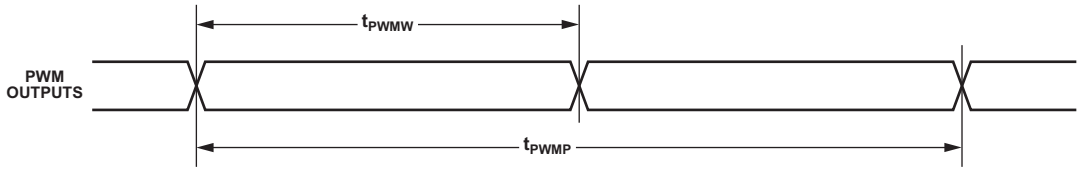


Figure 26. PWM Timing

Sample Rate Converter—Serial Input Port

The SRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 31 are valid at the DAI_P20–1 pins. This feature is not available on the ADSP-21363 models.

Table 31. SRC, Serial Input Port

Parameter		Min	Unit
Timing Requirements			
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3	ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3	ns
t_{SRCSD}[1]	SDATA Setup Before Serial Clock Rising Edge	3	ns
t_{SRCHD}[1]	SDATA Hold After Serial Clock Rising Edge	3	ns
$t_{SRCCLKW}$	Clock Width	36	ns
t_{SRCCLK}	Clock Period	80	ns

[1] The data, serial clock, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via the PCGs or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

SPI Interface—Master

The processor contains two SPI ports. The primary has dedicated pins and the secondary is available through the DAI. The timing provided in Table 39 and Table 40 applies to both ports.

Table 39. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	5.2		6.2		ns
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time) (SPI2)	8.2		9.5		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		2		ns
Switching Characteristics						
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		3.0		3.0	ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time) (SPI2)		8.0		9.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2.5$		$4 \times t_{PCLK} - 3.0$		ns
t_{SDSCIM}	FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge (SPI2)	$4 \times t_{PCLK} - 2.5$		$4 \times t_{PCLK} - 3.0$		ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0IN High	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		$4 \times t_{PCLK} - 1$		ns

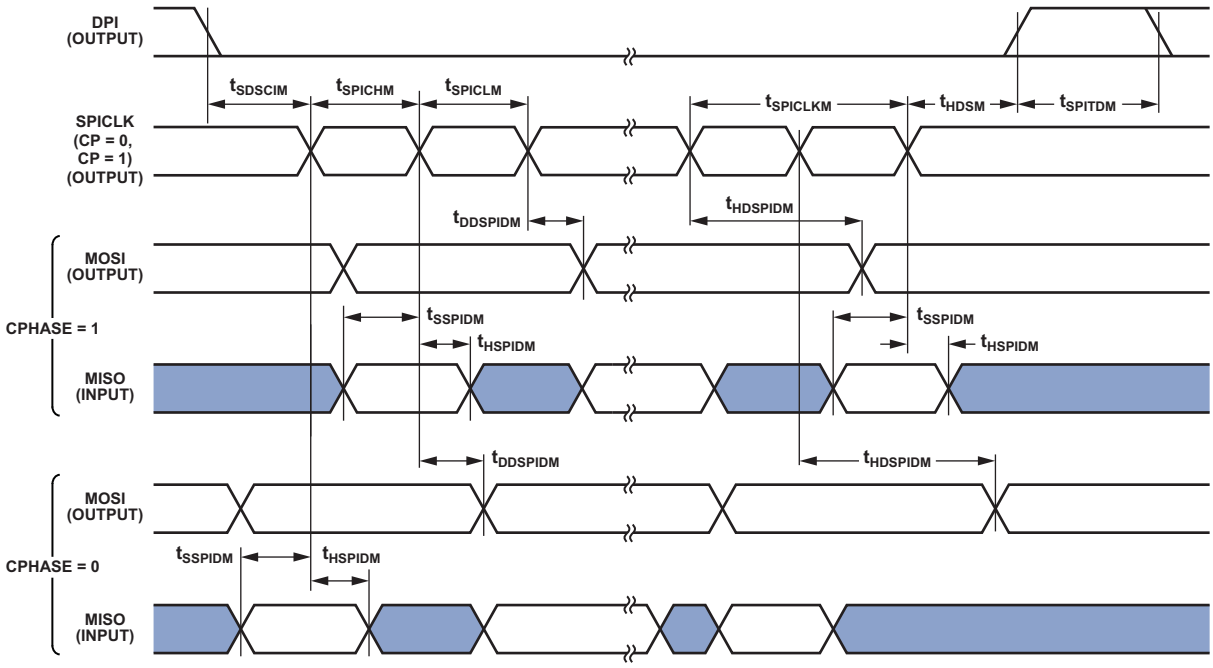


Figure 34. SPI Master Timing

SPI Interface—Slave

Table 40. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$			ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$			ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$			ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge				
	CPHASE = 0	$2 \times t_{PCLK}$			ns
	CPHASE = 1	$2 \times t_{PCLK}$			ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$			ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2			ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2			ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$			ns
Switching Characteristics					
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	5	5	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	8	9	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	5	5.5	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	8.6	10	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	11.0	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$			ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, "Serial Peripheral Interface Port" chapter.

JTAG Test Access Port and Emulation

Table 41. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = ADDR15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, MISO, MOSI, SPICLK, DAI_Px, and FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, ADDR15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$, and ALE.

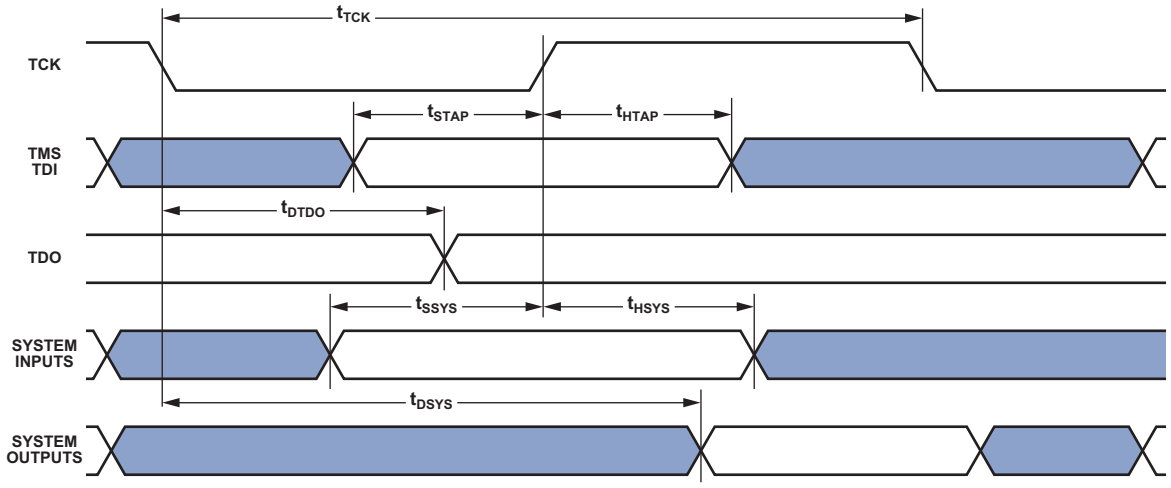


Figure 36. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 37 shows typical I-V characteristics for the output drivers of the processor. The curves represent the current drive capability of the output drivers as a function of output voltage.

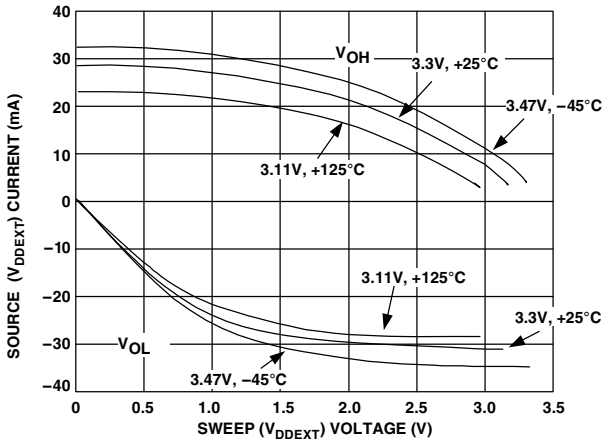


Figure 37. ADSP-2136x Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 12 on Page 20 through Table 41 on Page 45. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 38.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 39. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

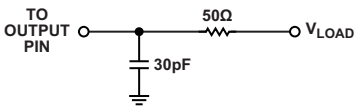


Figure 38. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

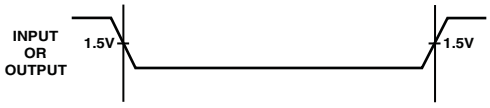


Figure 39. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 38). Figure 42 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 40, Figure 41, and Figure 42 may not be linear outside the ranges shown for Typical Output Delay versus Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) versus Load Capacitance.

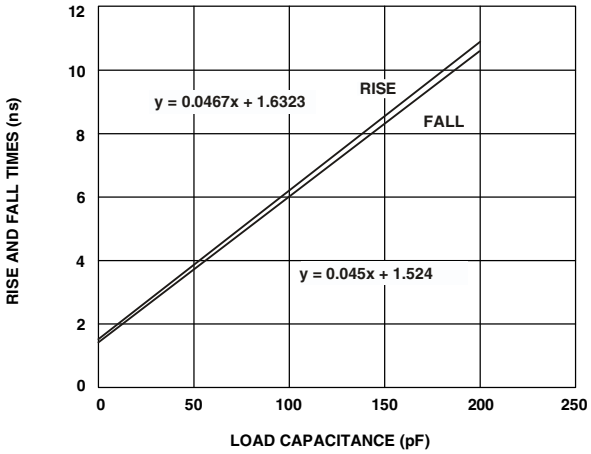


Figure 40. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

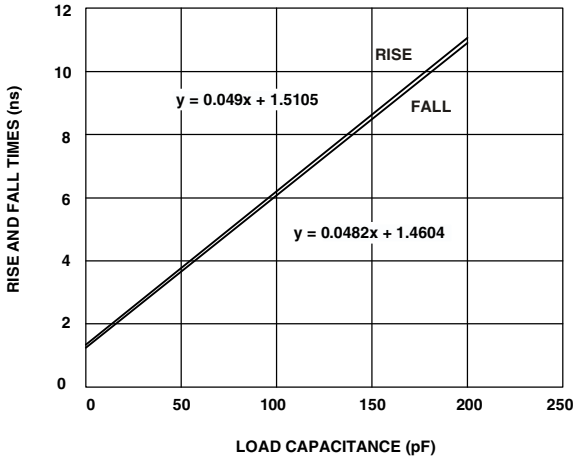


Figure 41. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

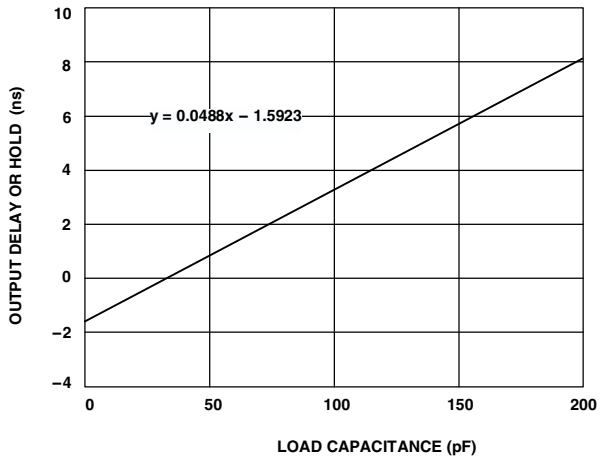


Figure 42. Typical Output Delay or Hold versus Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions on Page 14.

Table 42 through Table 44 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board and thermal via design comply with JEDEC standards JESD51-9 (BGA) and JESD51-5 (LQFP_EP). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

Industrial applications using the BGA package require thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

Industrial applications using the LQFP_EP package require thermal trace squares and thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-5 for more information.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 42 through Table 44.

P_D = power dissipation. See the Engineer-to-Engineer Note "*Estimating Power for the ADSP-21362 SHARC Processors*" (EE-277) for more information.

Values of θ_{JA} are provided for package comparison and PCB design considerations.

Values of θ_{JC} are provided for package comparison and PCB design considerations when an exposed pad is required. Note that the thermal characteristics values provided in Table 42 through Table 44 are modeled values.

Table 42. Thermal Characteristics for BGA (No Thermal vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	25.40	°C/W
θ_{JMA}	Airflow = 1 m/s	21.90	°C/W
θ_{JMA}	Airflow = 2 m/s	20.90	°C/W
θ_{JC}		5.07	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.140	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.330	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.410	°C/W

Table 43. Thermal Characteristics for BGA (Thermal vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	23.40	°C/W
θ_{JMA}	Airflow = 1 m/s	20.00	°C/W
θ_{JMA}	Airflow = 2 m/s	19.20	°C/W
θ_{JC}		5.00	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.130	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.300	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.360	°C/W

Table 44. Thermal Characteristics for LQFP_EP (with Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	16.80	°C/W
θ_{JMA}	Airflow = 1 m/s	14.20	°C/W
θ_{JMA}	Airflow = 2 m/s	13.50	°C/W
θ_{JC}		7.25	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.51	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.72	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.80	°C/W

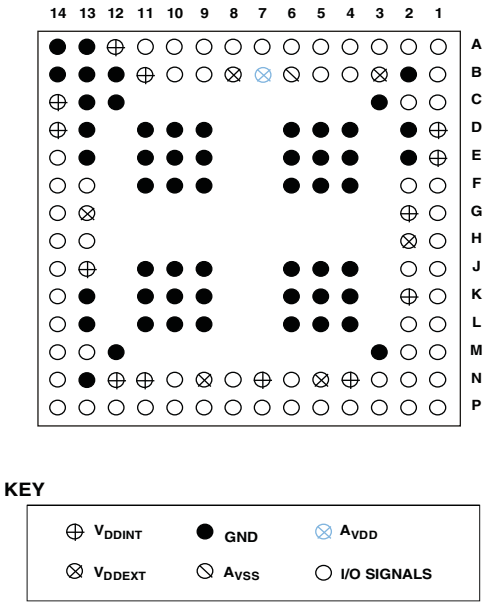


Figure 45. BGA Pin Assignments (Bottom View, Summary)

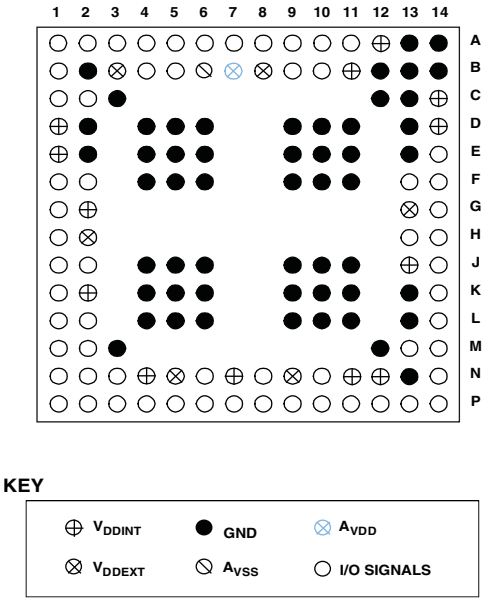


Figure 46. BGA Pin Assignments (Top View, Summary)

ORDERING GUIDE

Model[1]	Notes	Temperature Range[2]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21363KBC-1AA		0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
ADSP-21363KBCZ-1AA		0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
ADSP-21363KSWZ-1AA		0°C to +70°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21363BBC-1AA		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
ADSP-21363BBCZ-1AA		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
ADSP-21363BSWZ-1AA		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21363YSWZ-2AA	3	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21364KBCZ-1AA		0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
ADSP-21364KSWZ-1AA		0°C to +70°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21364BBCZ-1AA		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
ADSP-21364BSWZ-1AA		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21364YSWZ-2AA		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
ADSP-21366KBCZ-1AR	3, 4, 5	0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
ADSP-21366KBCZ-1AA	3, 4	0°C to +70°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
ADSP-21366KSWZ-1AA	3, 4	0°C to +70°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 14 for junction temperature (T_J) specification which is the only temperature specification.

[3] License from Dolby Laboratories, Inc., and Digital Theater Systems (DTS) required for these products.

[4] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/sharc.

[5] R = Tape and reel.