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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-LQFP-EP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21366yswz-2aa

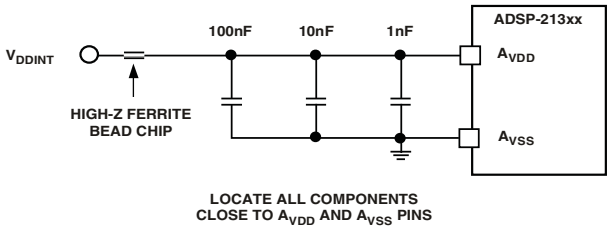


Figure 3. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices' DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processor to monitor and control the target board processor during emulation. Analog Devices' DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator does not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, refer to the appropriate emulator user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and

VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the processor's architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference* and the *ADSP-2136x SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
BOOT_CFG1–0	I	Input only	**Boot Configuration Select.** This pin is used to select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. For a description of the boot mode, refer to Table 5, Boot Mode Selection.
$\overline{\text{RESETOUT}}$	O	Output only	**Reset Out.** Drives out the core reset signal to an external device.
$\overline{\text{RESET}}$	I/A	Input only	**Processor Reset.** Resets the ADSP-2136x to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Input only[3]	**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the processors.
TMS	I/S (pu)	Three-state with pull-up enabled	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TDI	I/S (pu)	Three-state with pull-up enabled	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 k internal pull-up resistor.
TDO	O	Three-state[4]	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A (pu)	Three-state with pull-up enabled	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2136x. $\overline{\text{TRST}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D) (pu)	Three-state with pull-up enabled	**Emulation Status.** Must be connected to the processor's JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 kΩ internal pull-up resistor.
V_{DDINT}	P		**Core Power Supply.** Supplies the processor's core.
V_{DDEXT}	P		**I/O Power Supply.**
A_{VDD}	P		**Analog Power Supply.** Supplies the processor's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 8.
A_{VSS}	G		**Analog Power Supply Return.**
GND	G		**Power Supply Return.**

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

[1] $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE are three-stated (and not driven) only when $\overline{\text{RESET}}$ is active.
[2] Output only is a three-state driver with its output path always enabled.
[3] Input only is a three-state driver with both output path and pull-up disabled.
[4] Three-state is a three-state driver with pull-up disabled.

Reset

Table 12. Reset

Parameter		Min	Unit
Timing Requirements			
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$	ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

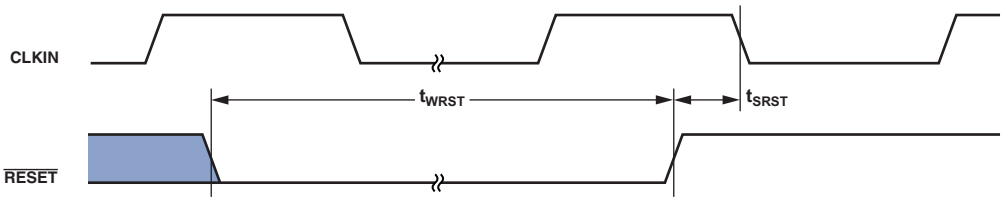


Figure 9. Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts.

Table 13. Interrupts

Parameter		Min	Unit
Timing Requirement			
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$	ns

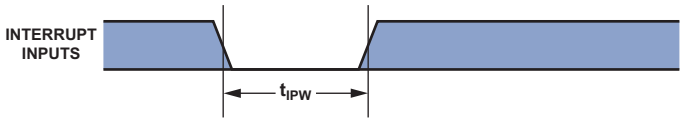


Figure 10. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP pin).

Table 14. Core Timer

Parameter		Min	Unit
Switching Characteristic			
t_{WCTIM}	TMREXP Pulse Width	$2 \times t_{PCLK} - 1$	ns

Figure 11. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 15. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

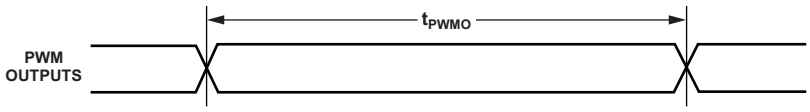


Figure 12. Timer PWM_OUT Timing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 through DAI_P20).

Table 18. Precision Clock Generator (Direct Pin Routing)

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Timing Requirements					
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$			ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5			ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3			ns
Switching Characteristics					
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	$12 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	$12 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOP}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$			ns

D = FSxDIV, PH = FSxPHASE. For more information, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, "Precision Clock Generators" chapter.

[1] In normal mode, t_{PCGOP} (min) = $2 \times t_{PCGIP}$.

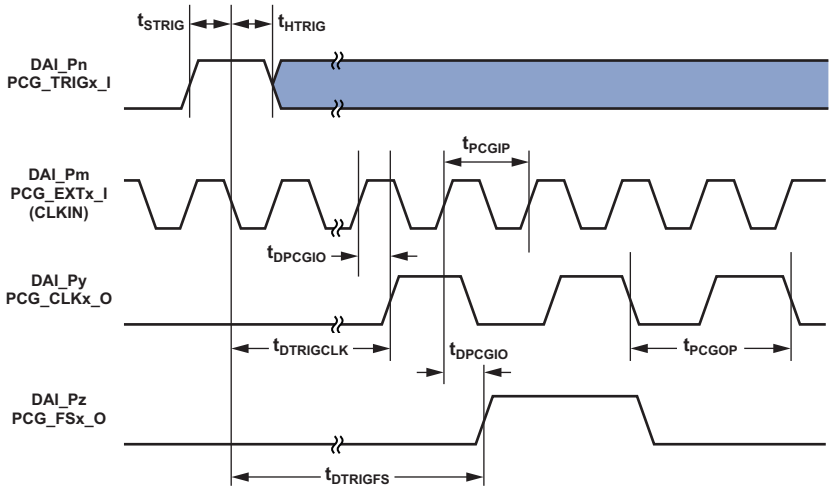


Figure 15. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3–0 and DAI_P20–1 pins, the parallel port, and the serial peripheral interface (SPI). See Table 6 on Page 11 for more information on flag use.

Table 19. Flags

Parameter		Min	Unit
Timing Requirement			
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$	ns
Switching Characteristic			
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 1$	ns

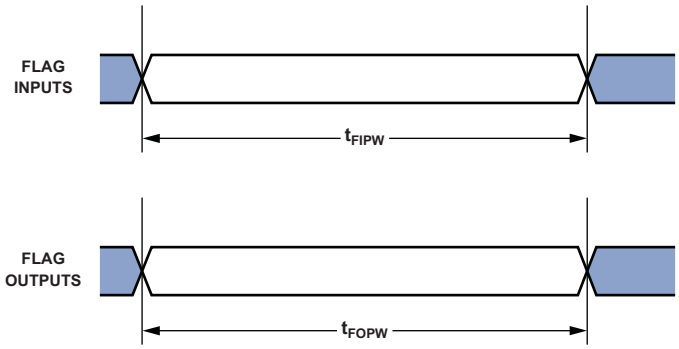


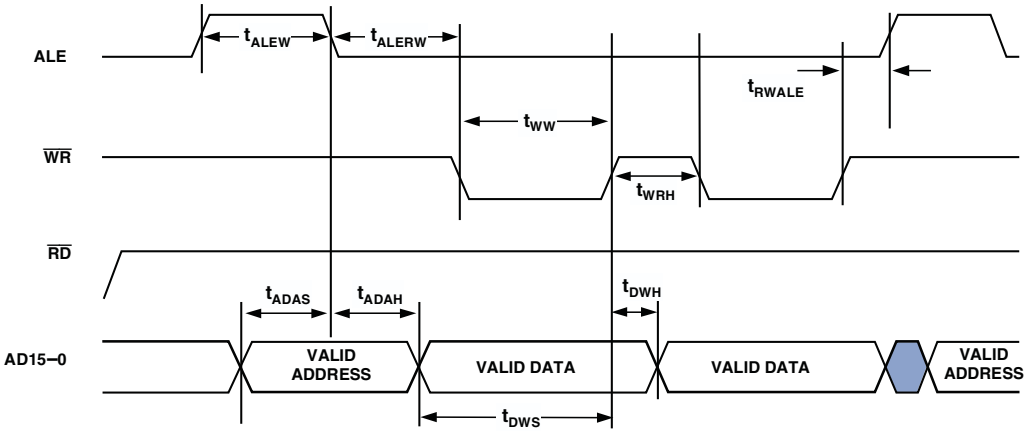
Figure 16. Flags

Table 23. 16-Bit Memory Write Cycle

Parameter		K and B Grade Min	Y Grade Min	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{PCLK} - 2.0$	$2 \times t_{PCLK} - 2.0$	ns
t_{ADAS}[1]	AD15–0 Address Setup Before ALE Deasserted	$t_{PCLK} - 2.5$	$t_{PCLK} - 2.5$	ns
t_{ALERW}	ALE Deasserted to Write Asserted	$2 \times t_{PCLK} - 3.8$	$2 \times t_{PCLK} - 3.8$	ns
t_{RWALE}	Write Deasserted to ALE Asserted	H + 0.5	H + 0.5	ns
t_{WRH}[2]	Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge	$F + H + t_{PCLK} - 2.3$	$F + H + t_{PCLK} - 2.3$	ns
t_{ADAH}[1]	AD15–0 Address Hold After ALE Deasserted	$t_{PCLK} - 2.3$	$t_{PCLK} - 2.3$	ns
t_{WW}	$\overline{WR}$ Pulse Width	D – F – 2.0	D – F – 2.0	ns
t_{DWS}	AD15–0 Data Setup Before $\overline{WR}$ High	$D - F + t_{PCLK} - 4.0$	$D - F + t_{PCLK} - 4.0$	ns
t_{DWH}	AD15–0 Data Hold After $\overline{WR}$ High	H	H	ns

D = (the value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{PCLK}.
H = t_{PCLK} (if a hold cycle is specified, else H = 0)
F = 7 × t_{PCLK} (if FLASH_MODE is set, else F = 0). If FLASH_MODE is set, D must be ≥ 9 × t_{PCLK}.
t_{PCLK} = (peripheral) clock period = 2 × t_{CCLK}

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.
[2] This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY WRITES, WHEN EMPP ≠ 0, ONLY ONE $\overline{WR}$ PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE $\overline{WR}$ PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 20. Write Cycle for 16-Bit Memory Timing

Table 26. Serial Ports—External Late Frame Sync

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Max	Unit
Switching Characteristics					
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive FS with MCE = 1, MFD = 0		9	10.5	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5			ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as serial mode, and MCE = 1, MFD = 0.

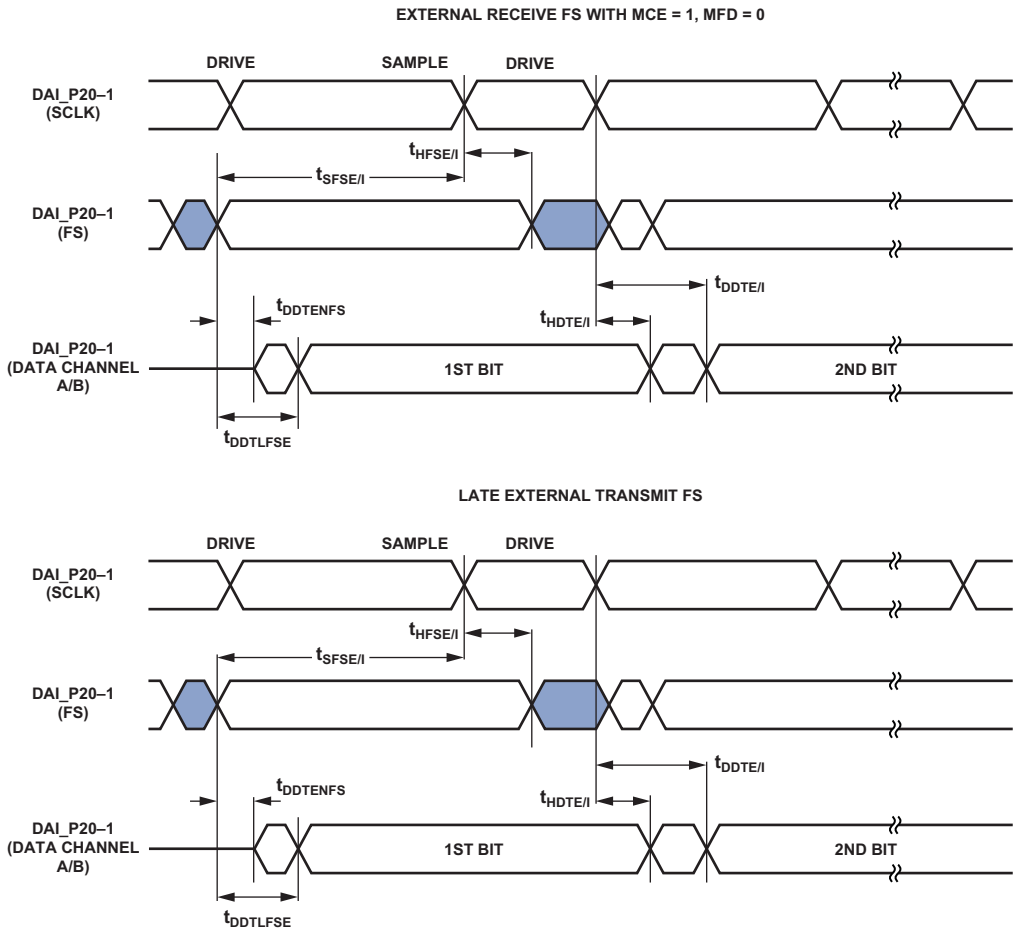


Figure 22. External Late Frame Sync

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 28. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 28. IDP

Parameter		Min	Unit
Timing Requirements			
t_{SISFS}[1]	Frame Sync Setup Before Clock Rising Edge	3	ns
t_{SIHFS}[1]	Frame Sync Hold After Clock Rising Edge	3	ns
t_{SISD}[1]	Data Setup Before Clock Rising Edge	3	ns
t_{SIHD}[1]	Data Hold After Clock Rising Edge	3	ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$	ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$	ns

[1] The data, clock, and frame sync signals can come from any of the DAI pins. Clock and frame sync can also come via the PCGs or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

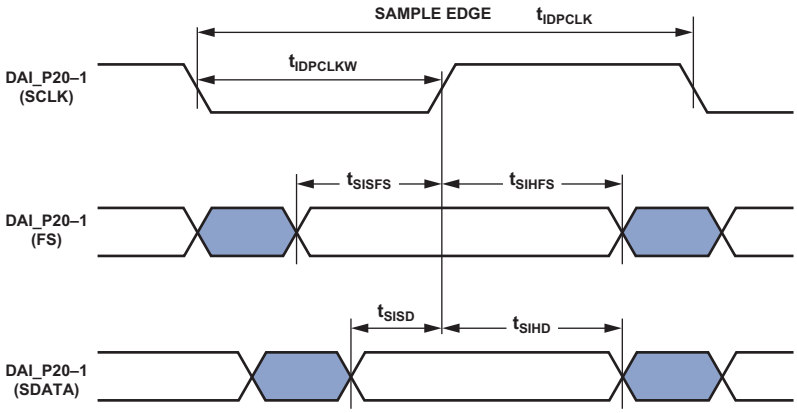


Figure 24. IDP Master Timing

Figure 30 shows the default I²S-justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

Table 34. S/PDIF Transmitter I²S Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{I2SD}	FS to MSB Delay in I²S Mode	1	SCLK

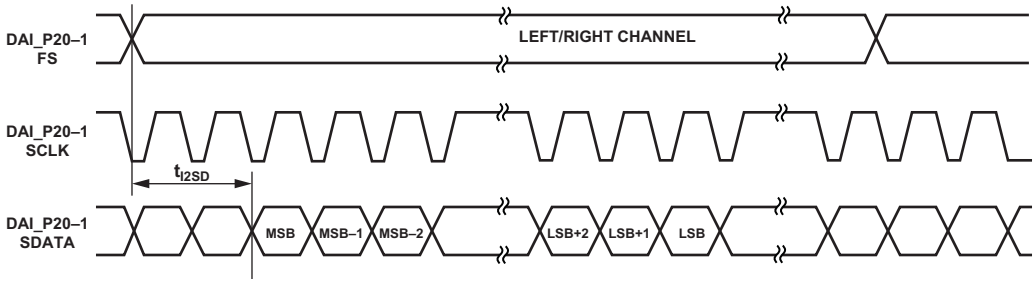


Figure 30. I²S-Justified Mode

Figure 31 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

Table 35. S/PDIF Transmitter Left-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{LJD}	FS to MSB Delay in Left-Justified Mode	0	SCLK

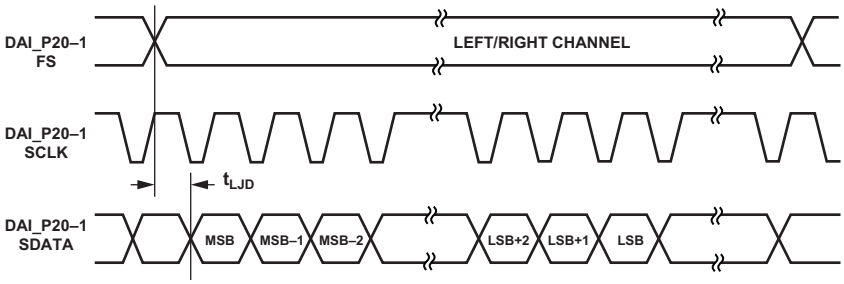


Figure 31. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 36. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 36. S/PDIF Transmitter Input Data Timing

Parameter		K Grade Min	K Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		9.5		ns
$t_{SITXCLK}$	Transmit Clock Period	20		20		ns
$t_{SISCLKW}$	Clock Width	36		36		ns
t_{SISCLK}	Clock Period	80		80		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins.The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

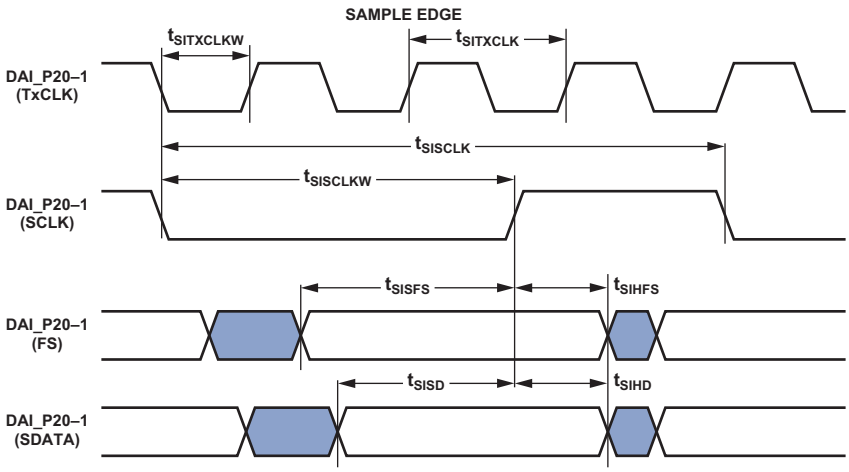


Figure 32. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 37. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Max	Unit
Frequency for TxCLK = 384 × Frame Sync	Oversampling Ratio × Frame Sync <= $1/t_{SITXCLK}$	MHz
Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

SPI Interface—Master

The processor contains two SPI ports. The primary has dedicated pins and the secondary is available through the DAI. The timing provided in Table 39 and Table 40 applies to both ports.

Table 39. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		K and B Grade Min	K and B Grade Max	Y Grade Min	Y Grade Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	5.2		6.2		ns
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time) (SPI2)	8.2		9.5		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		2		ns
Switching Characteristics						
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		3.0		3.0	ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time) (SPI2)		8.0		9.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2.5$		$4 \times t_{PCLK} - 3.0$		ns
t_{SDSCIM}	FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge (SPI2)	$4 \times t_{PCLK} - 2.5$		$4 \times t_{PCLK} - 3.0$		ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0IN High	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		$4 \times t_{PCLK} - 1$		ns

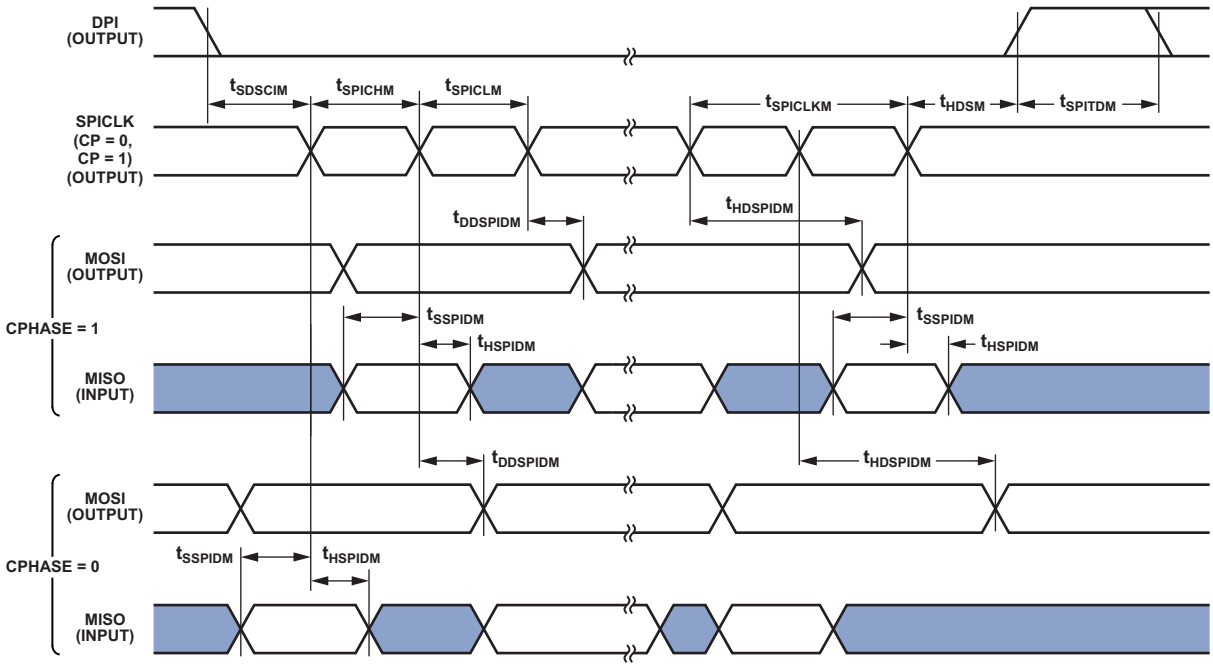


Figure 34. SPI Master Timing

OUTPUT DRIVE CURRENTS

Figure 37 shows typical I-V characteristics for the output drivers of the processor. The curves represent the current drive capability of the output drivers as a function of output voltage.

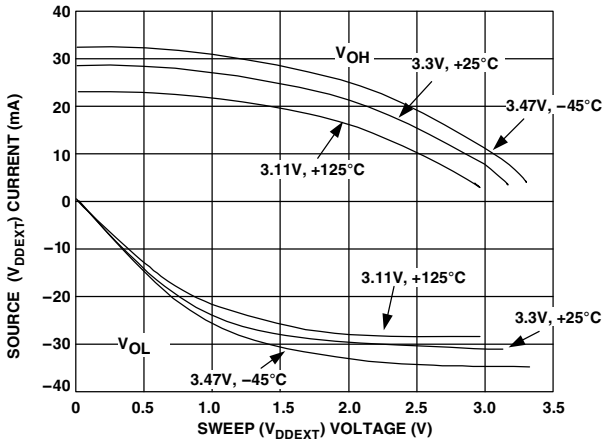


Figure 37. ADSP-2136x Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 12 on Page 20 through Table 41 on Page 45. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 38.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 39. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

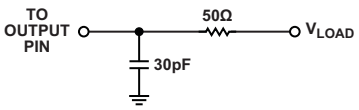


Figure 38. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

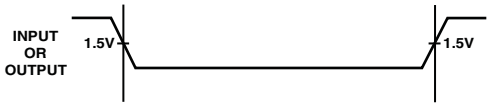


Figure 39. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 38). Figure 42 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 40, Figure 41, and Figure 42 may not be linear outside the ranges shown for Typical Output Delay versus Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) versus Load Capacitance.

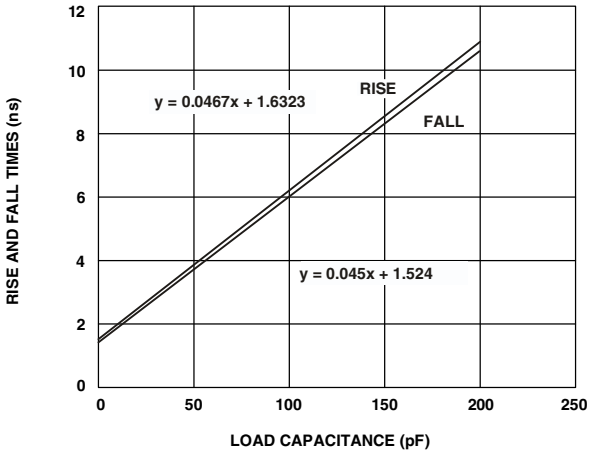


Figure 40. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

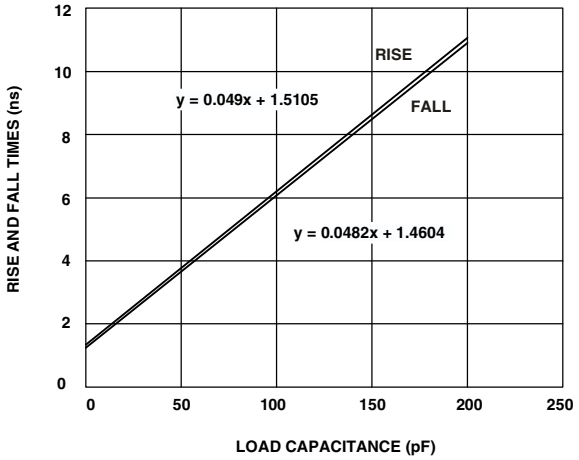


Figure 41. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

Table 46. BGA Pin Assignments (Continued)

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
AD5	J01	AD3	K01	AD2	L01	AD0	M01
AD4	J02	V_{DDINT}	K02	AD1	L02	$\overline{WR}$	M02
GND	J04	GND	K04	GND	L04	GND	M03
GND	J05	GND	K05	GND	L05	GND	M12
GND	J06	GND	K06	GND	L06	DAI_P12 (SD3B)	M13
GND	J09	GND	K09	GND	L09	DAI_P13 (SCLK3)	M14
GND	J10	GND	K10	GND	L10		
GND	J11	GND	K11	GND	L11		
V_{DDINT}	J13	GND	K13	GND	L13		
DAI_P16 (SD4B)	J14	DAI_P15 (SD4A)	K14	DAI_P14 (SFS3)	L14		
AD15	N01	AD14	P01				
ALE	N02	AD13	P02				
$\overline{RD}$	N03	AD12	P03				
V_{DDINT}	N04	AD11	P04				
V_{DDEXT}	N05	AD10	P05				
AD8	N06	AD9	P06				
V_{DDINT}	N07	DAI_P1 (SD0A)	P07				
DAI_P2 (SD0B)	N08	DAI_P3 (SCLK0)	P08				
V_{DDEXT}	N09	DAI_P5 (SD1A)	P09				
DAI_P4 (SFS0)	N10	DAI_P6 (SD1B)	P10				
V_{DDINT}	N11	DAI_P7 (SCLK1)	P11				
V_{DDINT}	N12	DAI_P8 (SFS1)	P12				
GND	N13	DAI_P9 (SD2A)	P13				
DAI_P10 (SD2B)	N14	DAI_P11 (SD3A)	P14				

Figure 45 and Figure 46 show BGA pin assignments from the bottom and top, respectively.

Note: Use the center block of ground pins to provide thermal pathways to your printed circuit board's ground plane.

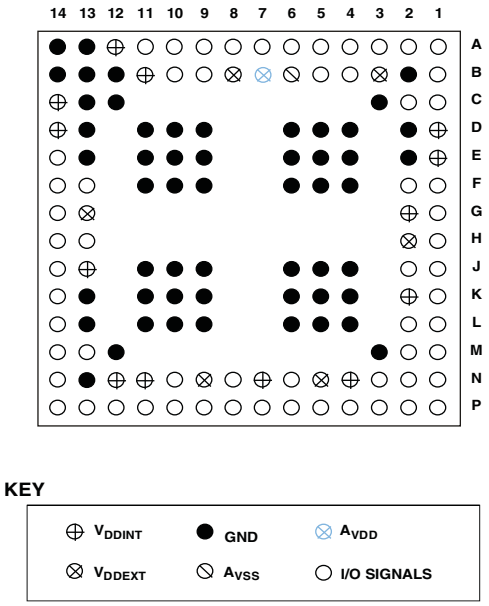


Figure 45. BGA Pin Assignments (Bottom View, Summary)

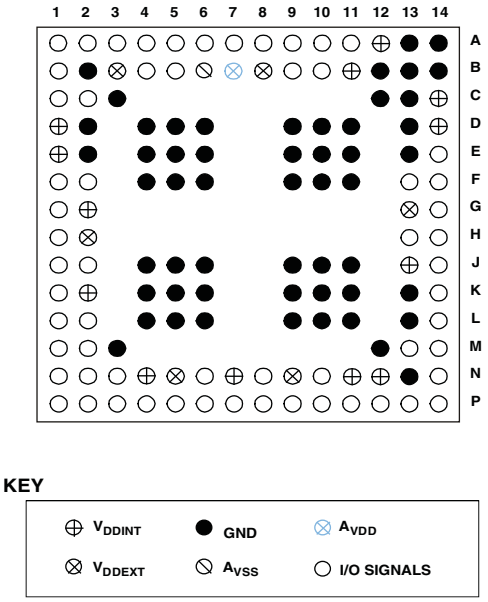
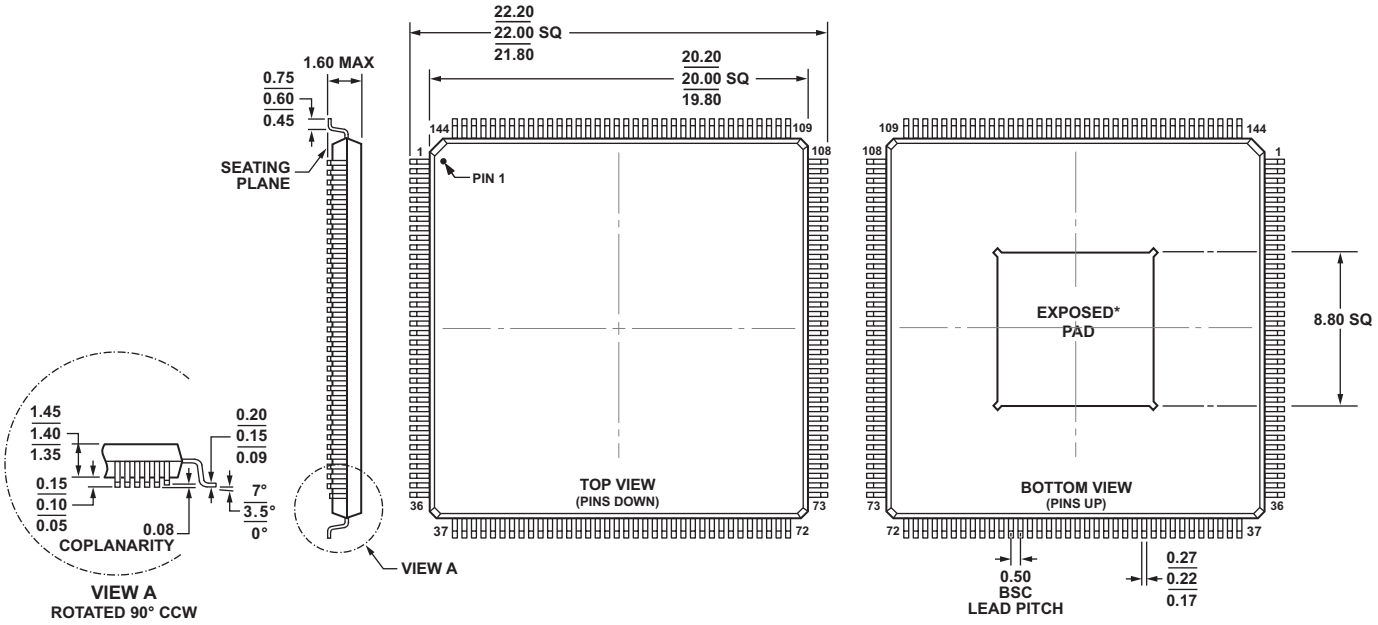


Figure 46. BGA Pin Assignments (Top View, Summary)

PACKAGE DIMENSIONS

The processor is available in 136-ball BGA and 144-lead exposed pad (LQFP_EP) packages.



COMPLIANT TO JEDEC STANDARDS MS-026-BFB-HD
*EXPOSED PAD IS COINCIDENT WITH BOTTOM SURFACE AND DOES NOT PROTRUDE BEYOND IT. EXPOSED PAD IS CENTERED.

Figure 47. 144-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP[1]]
(SW-144-1)
Dimensions shown in millimeters

[1] For information relating to the exposed pad on the SW-144-1 package, see the table endnote on Page 48.

AUTOMOTIVE PRODUCTS

Some ADSP-2136x models are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 48. Automotive Products

Model	Notes	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
AD21362WBBCZ1xx	2	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21362WBSWZ1xx	2	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21362WYSWZ2xx	2	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WBBCZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21363WBSWZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21363WYSWZ2xx		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WBBCZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21364WBSWZ1xx		–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21364WYSWZ2xx		–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ1xxA	2, 3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WBSWZ1xxF	2, 3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21365WYSWZ2xxA	2, 3, 4	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WBBCZ1xxA	3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	136-Ball CSP_BGA	BC-136-1
AD21366WBSWZ1xxA	3, 4	–40°C to +85°C	333 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1
AD21366WYSWZ2xxA	3, 4	–40°C to +105°C	200 MHz	3M Bit	4M Bit	144-Lead LQFP_EP	SW-144-1

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 14 for junction temperature (T_J) specification which is the only temperature specification.

[2] License from DTLA required for these products.

[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/sharc.

[4] License from Dolby Laboratories, Inc., and Digital Theater Systems (DTS) required for these products.