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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	4.2MHz
Connectivity	I ² C, SSP, UART/USART
Peripherals	LCD, Melody Driver, POR, PWM, WDT
Number of I/O	14
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 2x12b, 2x24b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q422-nnntbz03a7

- LCD driver
 - Dot matrix can be supported.
 - ML610Q421: 400 dots max. (50 seg × 8 com), 1/1 to 1/8 duty
 - ML610Q422: 800 dots max. (50 seg × 16 com), 1/1 to 1/16 duty
 - 1/3 or 1/4 bias (built-in bias generation circuit)
 - Frame frequency selectable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
 - Bias voltage multiplying clock selectable (8 types)
 - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
 - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
 - Programmable display allocation function (available only when 1/1~1/8 duty is selected)
- Reset
 - Reset through the RESET_N pin
 - Power-on reset generation when powered on
 - Reset when oscillation stop of the low-speed clock is detected
 - Reset by the watchdog timer (WDT) overflow
- Power supply voltage detect function
 - Judgment voltages: One of 16 levels
 - Judgment accuracy: ±2% (Typ.)
- Clock
 - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
 - Crystal oscillation (32.768 kHz)
 - High-speed clock:
 - Built-in RC oscillation (500 kHz)
 - Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
 - Selection of high-speed clock mode by software:
 - Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
 - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.
- Guaranteed operating range
 - Operating temperature: –20°C to 70°C (P version: –40°C to +85°C)
 - Operating voltage: $V_{DD} = 1.1V$ to 3.6V, $AV_{DD} = 2.2V$ to 3.6V

●Product name – Supported Function

The line-up of the ML610Q421 and the ML610Q422 is below.

- Chip (Die) -	ROM type	Operating temperature	Product availability
ML610Q421-xxxWA	Flash ROM	-20°C to +70°C	Yes
ML610Q422-xxxWA	Flash ROM	-20°C to +70°C	Yes
ML610Q421P-xxxWA	Flash ROM	-40°C to +85°C	Yes
ML610Q422P-xxxWA	Flash ROM	-40°C to +85°C	Yes

-120-pin plastic TQFP -	ROM type	Operating temperature	Product availability
ML610Q421-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q422-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q421P-xxxTB	Flash ROM	-40°C to +85°C	Yes
ML610Q422P-xxxTB	Flash ROM	-40°C to +85°C	Yes

xxx: ROM code number (xxx of the blank product is NNN)

Q: Flash ROM version

P: Wide range temperature version (P version)

WA: Chip (Die),

TB: TQFP

ML610Q422 Block Diagram

Figure 2 show the block diagram of the ML610Q422.

"*" indicates the secondary function of each port.

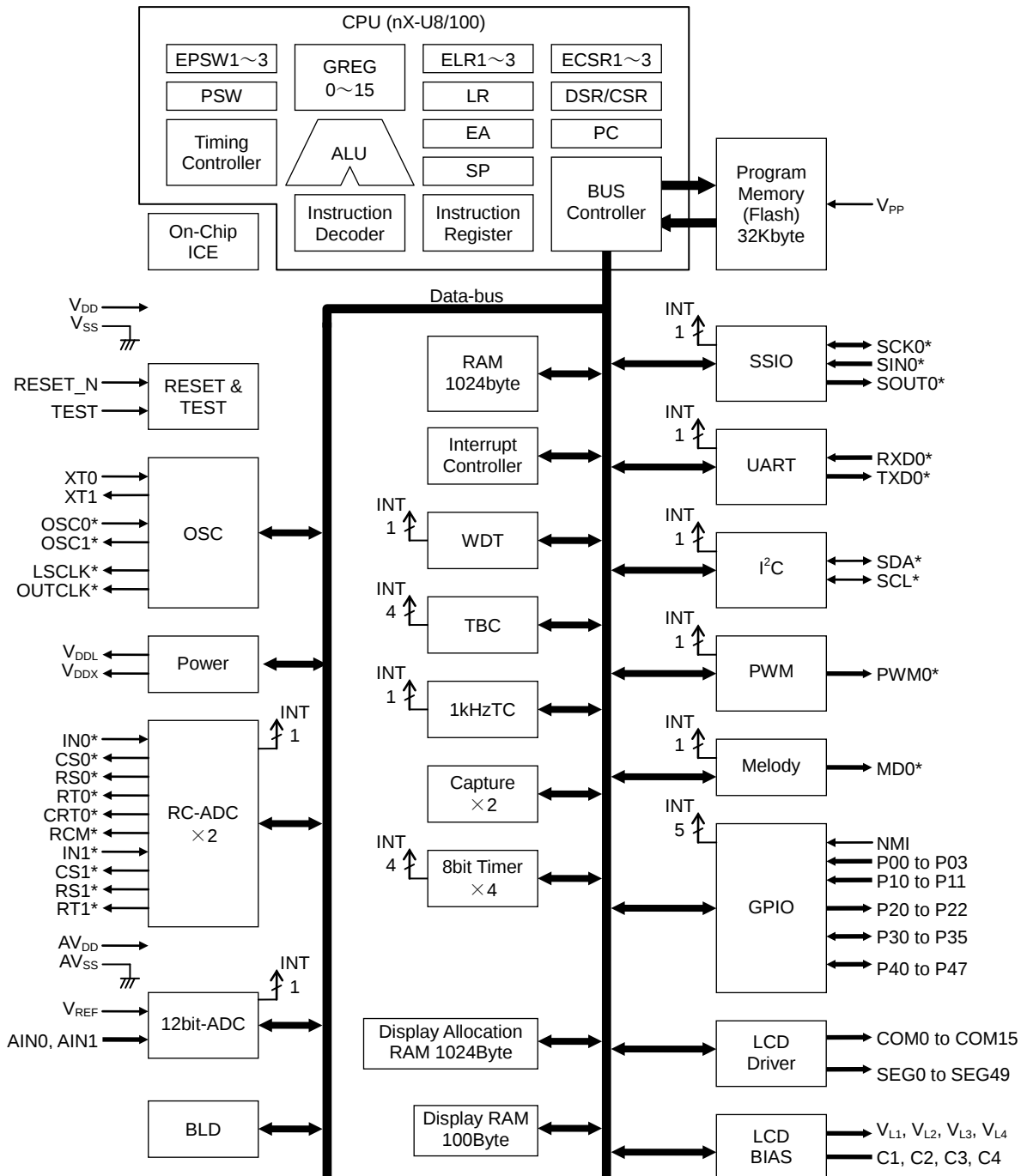
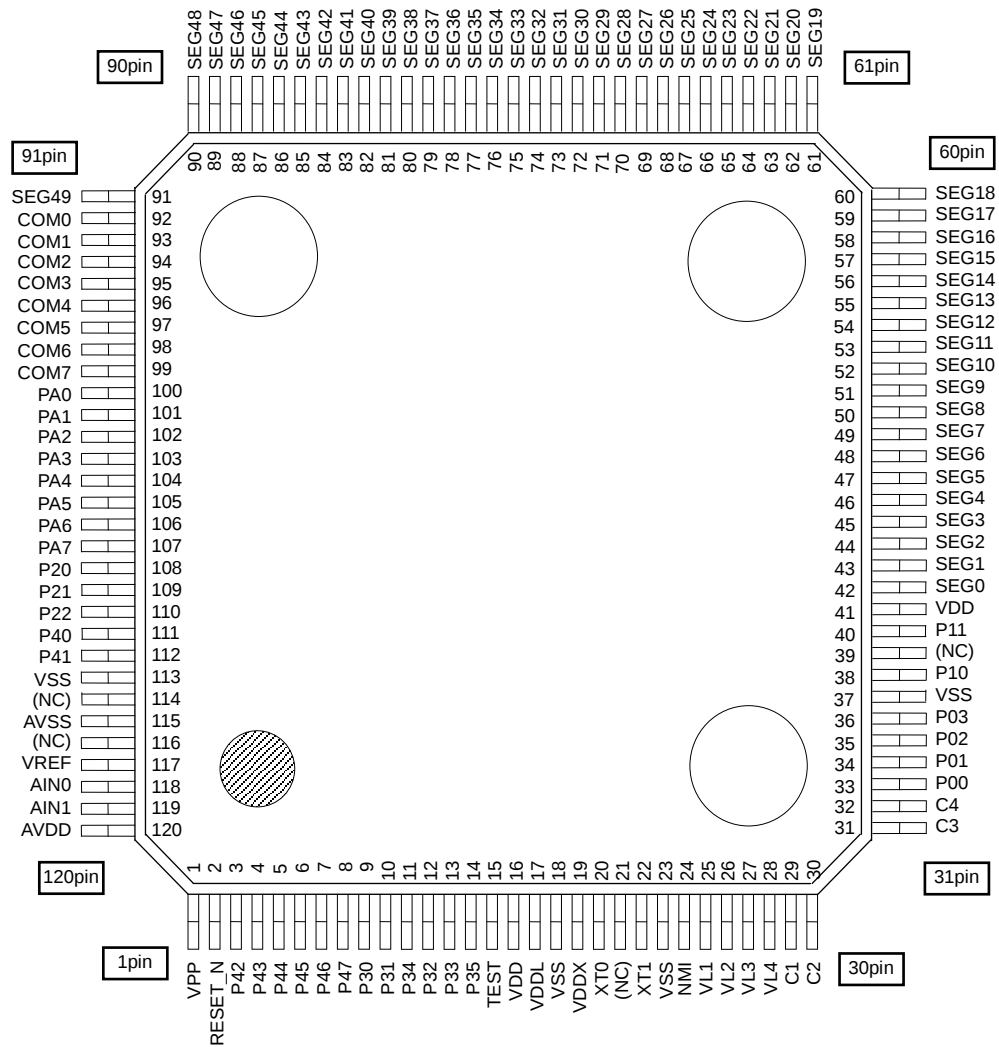


Figure 2 ML610Q422 Block Diagram

PIN CONFIGURATION

ML610Q421 TQFP120 Pin Layout

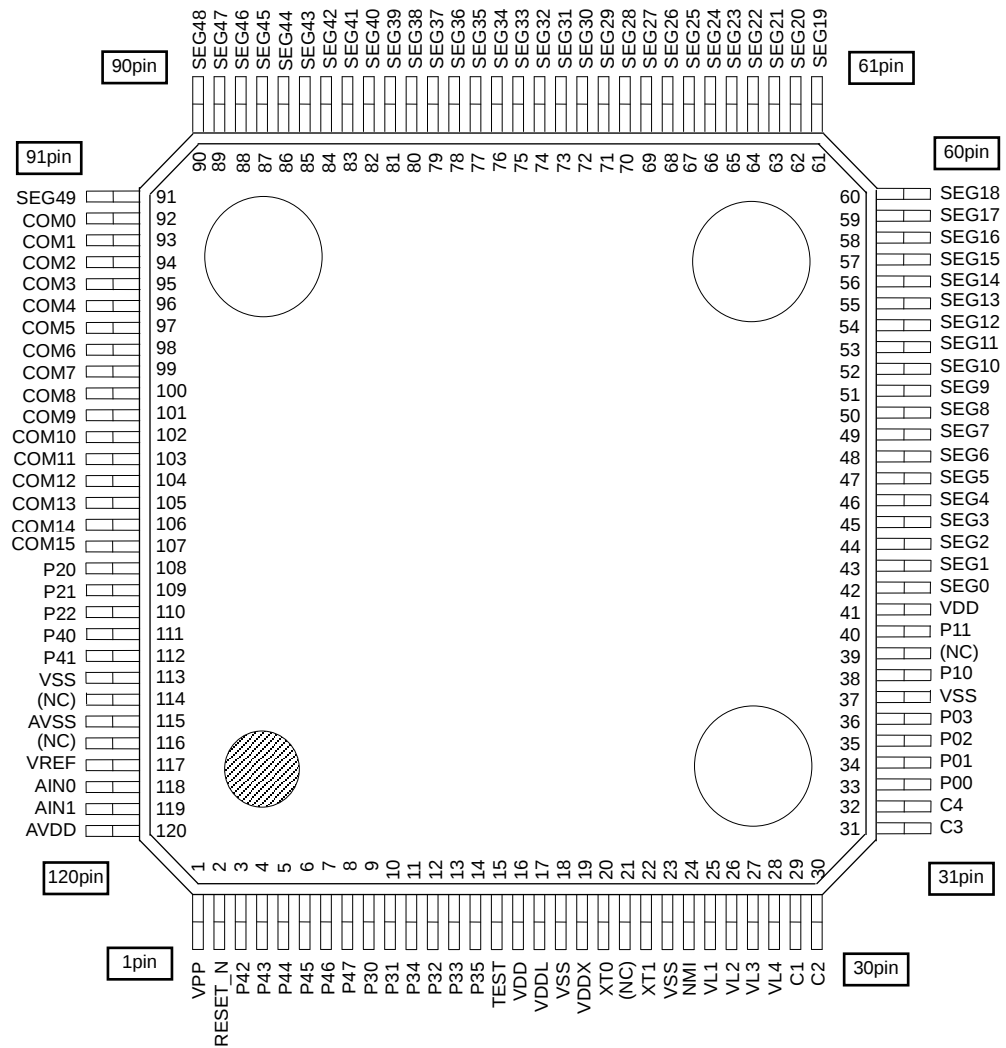


Note:

The assignment of the pads P30 to P35 are not in order.

Figure 3 ML610Q421 TQFP120 Pin Configuration

ML610Q422 TQFP120 Pin Layout

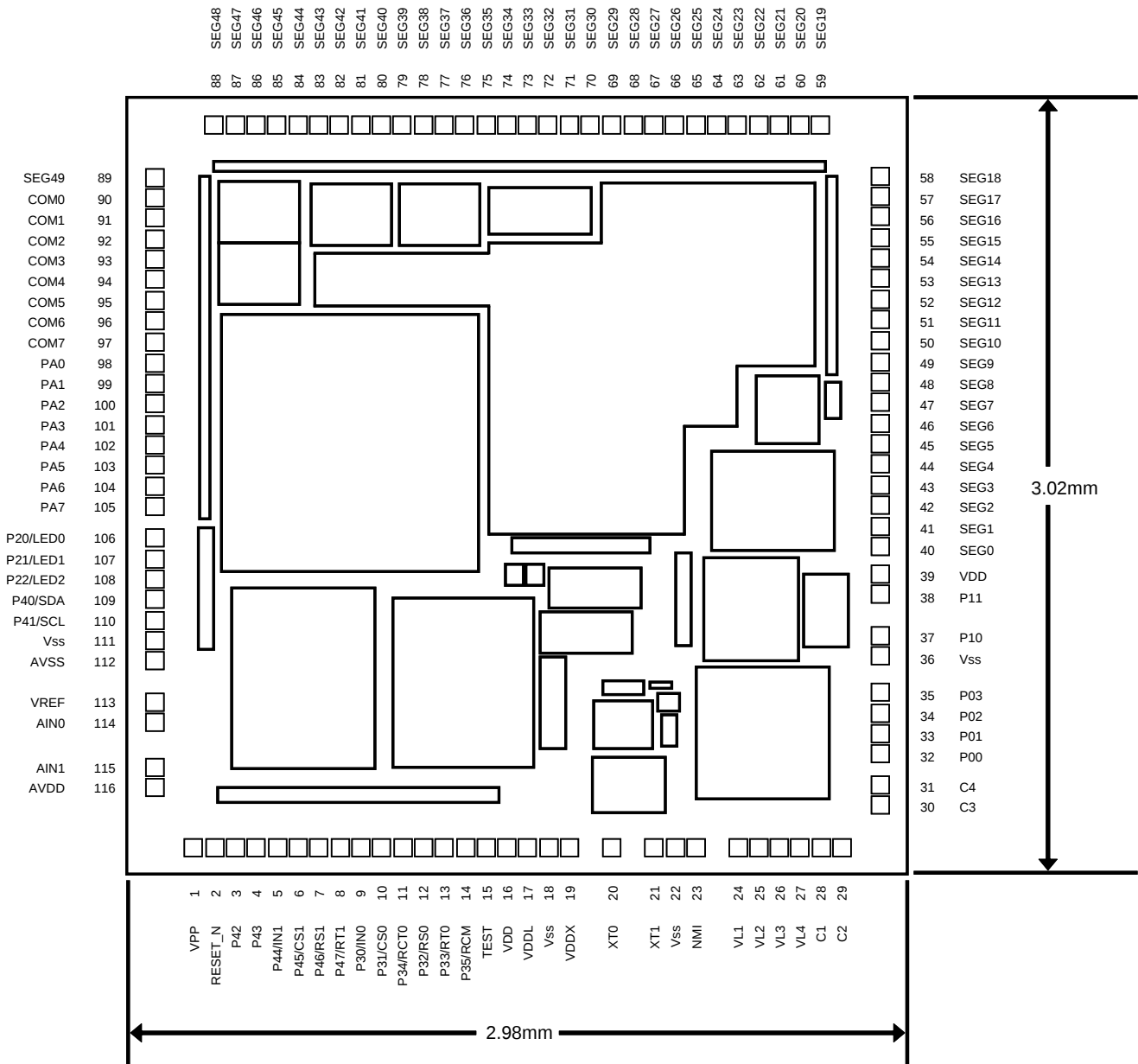


Note:

The assignment of the pads P30 to P35 are not in order.

Figure 4 ML610Q422 TQFP120 Pin Configuration

ML610Q421 Chip Pin Layout & Dimension



Note:

The assignment of the pads P30 to P35 are not in order.

Chip size:	2.98 mm × 3.02 mm
PAD count:	116 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V _{SS} level

Figure 5 ML610Q421 Chip Layout & Dimension

PAD COORDINATES

ML610Q421 Pad Coordinates

Table 1 ML610Q421 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)
1	VPP	-1240	-1404	51	SEG11	1384	640	101	PA3	-1384	240
2	RESET_N	-1160	-1404	52	SEG12	1384	720	102	PA4	-1384	160
3	P42	-1080	-1404	53	SEG13	1384	800	103	PA5	-1384	80
4	P43	-1000	-1404	54	SEG14	1384	880	104	PA6	-1384	0
5	P44	-920	-1404	55	SEG15	1384	960	105	PA7	-1384	-80
6	P45	-840	-1404	56	SEG16	1384	1040	106	P20	-1384	-200
7	P46	-760	-1404	57	SEG17	1384	1120	107	P21	-1384	-280
8	P47	-680	-1404	58	SEG18	1384	1200	108	P22	-1384	-360
9	P30	-600	-1404	59	SEG19	1160	1404	109	P40	-1384	-440
10	P31	-520	-1404	60	SEG20	1080	1404	110	P41	-1384	-520
11	P34	-440	-1404	61	SEG21	1000	1404	111	Vss	-1384	-600
12	P32	-360	-1404	62	SEG22	920	1404	112	AVss	-1384	-680
13	P33	-280	-1404	63	SEG23	840	1404	113	VREF	-1384	-840
14	P35	-200	-1404	64	SEG24	760	1404	114	AIN0	-1384	-920
15	TEST	-120	-1404	65	SEG25	680	1404	115	AIN1	-1384	-1092
16	VDD	-40	-1404	66	SEG26	600	1404	116	AVDD	-1384	-1172
17	VDDL	40	-1404	67	SEG27	520	1404				
18	Vss	120	-1404	68	SEG28	440	1404				
19	VDDX	200	-1404	69	SEG29	360	1404				
20	XT0	360	-1404	70	SEG30	280	1404				
21	XT1	520	-1404	71	SEG31	200	1404				
22	Vss	600	-1404	72	SEG32	120	1404				
23	NMI	680	-1404	73	SEG33	40	1404				
24	VL1	840	-1404	74	SEG34	-40	1404				
25	VL2	920	-1404	75	SEG35	-120	1404				
26	VL3	1000	-1404	76	SEG36	-200	1404				
27	VL4	1080	-1404	77	SEG37	-280	1404				
28	C1	1160	-1404	78	SEG38	-360	1404				
29	C2	1240	-1404	79	SEG39	-440	1404				
30	C3	1384	-1240	80	SEG40	-520	1404				
31	C4	1384	-1160	81	SEG41	-600	1404				
32	P00	1384	-1040	82	SEG42	-680	1404				
33	P01	1384	-960	83	SEG43	-760	1404				
34	P02	1384	-880	84	SEG44	-840	1404				
35	P03	1384	-800	85	SEG45	-920	1404				
36	Vss	1384	-660	86	SEG46	-1000	1404				
37	P10	1384	-580	87	SEG47	-1080	1404				
38	P11	1384	-420	88	SEG48	-1160	1404				
39	VDD	1384	-340	89	SEG49	-1384	1200				
40	SEG0	1384	-240	90	COM0	-1384	1120				
41	SEG1	1384	-160	91	COM1	-1384	1040				
42	SEG2	1384	-80	92	COM2	-1384	960				
43	SEG3	1384	0	93	COM3	-1384	880				
44	SEG4	1384	80	94	COM4	-1384	800				
45	SEG5	1384	160	95	COM5	-1384	720				
46	SEG6	1384	240	96	COM6	-1384	640				
47	SEG7	1384	320	97	COM7	-1384	560				
48	SEG8	1384	400	98	PA0	-1384	480				
49	SEG9	1384	480	99	PA1	-1384	400				
50	SEG10	1384	560	100	PA2	-1384	320				

PIN LIST

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
18,22, 36,111	18,22, 37,111	V _{SS}	—	Negative power supply pin	—	—	—	—	—	—
16,39	16,39	V _{DD}	—	Positive power supply pin	—	—	—	—	—	—
17	17	V _{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
19	19	V _{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
1	1	V _{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
112	112	AV _{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
116	116	AV _{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
24	24	V _{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
25	25	V _{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
26	26	V _{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
27	27	V _{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
28	28	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
29	29	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
30	30	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
31	31	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
15	15	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
2	2	RESET_N	I	Reset input pin	—	—	—	—	—	—
20	20	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
21	21	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
113	113	V _{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
114	114	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—
115	115	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—
23	23	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
32	32	P00/ EXI0/ CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
33	33	P01/ EXI1/ CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
34	34	P02/ EXI2/ RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
35	35	P03/ EXI3	I	Input port, External interrupt 3	—	—	—	—	—	—
37	37	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
38	38	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
106	106	P20/ LED0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
107	107	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
108	108	P22/LED2	O	Output port	MD0	O	Melody output	—	—	—
9	9	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
10	10	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
11	11	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
12	12	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
13	13	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
14	14	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
109	109	P40	I/O	Input/output port	SDA	I/O	I ² C data input/output	SIN0	I	SSIO data input
110	110	P41	I/O	Input/output port	SCL	I/O	I ² C clock input/output	SCK0	I/O	SSIO synchronous clock
3	3	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	I	SSIO data output
4	4	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
5	5	P44/ T02P0CK	I/O	Input/output port, Timer 0/Timer 2/ PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
6	6	P45/ T13P1CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
7	7	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
8	8	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
—	98	PA0	I/O	Input/output port	—	—	—	—	—	—
—	99	PA1	I/O	Input/output port	—	—	—	—	—	—
—	100	PA2	I/O	Input/output port	—	—	—	—	—	—
—	101	PA3	I/O	Input/output port	—	—	—	—	—	—
—	102	PA4	I/O	Input/output port	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
76	76	SEG36	O	LCD segment pin	—	—	—	—	—	—
77	77	SEG37	O	LCD segment pin	—	—	—	—	—	—
78	78	SEG38	O	LCD segment pin	—	—	—	—	—	—
79	79	SEG39	O	LCD segment pin	—	—	—	—	—	—
80	80	SEG40	O	LCD segment pin	—	—	—	—	—	—
81	81	SEG41	O	LCD segment pin	—	—	—	—	—	—
82	82	SEG42	O	LCD segment pin	—	—	—	—	—	—
83	83	SEG43	O	LCD segment pin	—	—	—	—	—	—
84	84	SEG44	O	LCD segment pin	—	—	—	—	—	—
85	85	SEG45	O	LCD segment pin	—	—	—	—	—	—
86	86	SEG46	O	LCD segment pin	—	—	—	—	—	—
87	87	SEG47	O	LCD segment pin	—	—	—	—	—	—
88	88	SEG48	O	LCD segment pin	—	—	—	—	—	—
89	89	SEG49	O	LCD segment pin	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V _{SS} as required.	—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock.	Secondary	—
OSC1	O	A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V _{SS} . This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port. These pins are for the ML610Q421, but are not provided in the ML610Q422.	Primary	Positive

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

Table 3 Termination of Unused Pins

Pin	Recommended pin termination
V _{PP}	Open
AV _{DD}	V _{SS}
AV _{SS}	V _{SS}
V _{REF}	V _{SS}
AIN0, AIN1	Open
V _{L1} , V _{L2} , V _{L3} , V _{L4}	Open
C1, C2, C3, C4	Open
RESET_N	Open
TEST	Open
NMI	Open
P00 to P03	V _{DD} or V _{SS}
P10 to P11	V _{DD}
P20 to P22	Open
P30 to P35	Open
P40 to P47	Open
PA0 to PA7	Open
COM0 to 15	Open
SEG0 to 49	Open

Note:

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 2	AV _{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 3	V _{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 4	V _{DDL}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 5	V _{DDX}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 6	V _{L1}	Ta = 25°C	−0.3 to +1.75	V
Power supply voltage 7	V _{L2}	Ta = 25°C	−0.3 to +3.5	V
Power supply voltage 8	V _{L3}	Ta = 25°C	−0.3 to +5.25	V
Power supply voltage 9	V _{L4}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V _{IN}	Ta = 25°C	−0.3 to V _{DD} +0.3	V
Output voltage	V _{OUT}	Ta = 25°C	−0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port3−A, Ta = 25°C	−12 to +11	mA
Output current 2	I _{OUT2}	Port2, Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	1.25	W
Storage temperature	T _{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	ML610Q421, ML610Q422	−20 to +70	°C
		ML610Q421P, ML610Q422P	−40 to +85	
Operating voltage	V _{DD}	—	1.1 to 3.6	V
	AV _{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f _{OP}	V _{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V _{DD} = 1.3 to 3.6V	30k to 650k	
		V _{DD} = 1.8 to 3.6V	30k to 4.2M	
Capacitor externally connected to V _{DDL} pin	C _{L0}	—	1.0±30%	μF
	C _{L1}	—	0.1±30%	
Capacitor externally connected to V _{DDX} pin	C _X	—	0.1±30%	μF
Capacitors externally connected to V _{L1, 2, 3, 4} pins	C _{a, b, c, d}	—	1.0±30%	μF
Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins	C _{12, C34}	—	1.0±30%	μF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f _{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R _L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor ^{*1}	C _{DL} /C _{GL}	C _L =6pF of crystal oscillation ^{*2}	—	0	—	pF
		C _L =9pF of crystal oscillation	—	6	—	
		C _L =12pF of crystal oscillation	—	12	—	
High-speed crystal/ceramic oscillation frequency	f _{XTH}	—	—	4.0M / 4.096M	—	Hz
High-speed crystal oscillation external capacitor	C _{DH}	—	—	24	—	pF
	C _{GH}	—	—	24	—	

^{*1}: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.

^{*2}: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	At write/erase	0 to +40	°C
Operating voltage	V _{DD}	At write/erase ^{*1}	2.75 to 3.6	V
	V _{DDL}	At write/erase ^{*1}	2.5 to 2.75	
	V _{PP}	At write/erase ^{*1}	7.7 to 8.3	
Write cycles	C _{EP}	—	80	cycles
Data retention	Y _{DR}	—	10	years

^{*1}: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and erasing Flash ROM.
V_{PP} pin has an internal pulldown resistor.

DC CHARACTERISTICS (2/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (2/5)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
V_{L1} voltage	V_{L1}	$V_{DD} = 3.0V$, $T_j = 25^\circ C$	CN4-0 = 00H	0.89	0.94	0.99	V	1
			CN4-0 = 01H	0.91	0.96	1.01		
			CN4-0 = 02H	0.93	0.98	1.03		
			CN4-0 = 03H	0.95	1.00	1.05		
			CN4-0 = 04H	0.97	1.02	1.07		
			CN4-0 = 05H	0.99	1.04	1.09		
			CN4-0 = 06H	1.01	1.06	1.11		
			CN4-0 = 07H	1.03	1.08	1.13		
			CN4-0 = 08H	1.05	1.10	1.15		
			CN4-0 = 09H	1.07	1.12	1.17		
			CN4-0 = 0AH	1.09	1.14	1.19		
			CN4-0 = 0BH	1.11	1.16	1.21		
			CN4-0 = 0CH	1.13	1.18	1.23		
			CN4-0 = 0DH	1.15	1.20	1.25		
			CN4-0 = 0EH	1.17	1.22	1.27		
			CN4-0 = 0FH	1.19	1.24	1.29		
			CN4-0 = 10H	1.21	1.26	1.31		
			CN4-0 = 11H	1.23	1.28	1.33		
			CN4-0 = 12H	1.25	1.30	1.35		
			CN4-0 = 13H	1.27	1.32	1.37		
			CN4-0 = 14H ^{*1}	1.29	1.34	1.39		
			CN4-0 = 15H ^{*1}	1.31	1.36	1.41		
			CN4-0 = 16H ^{*1}	1.33	1.38	1.43		
			CN4-0 = 17H ^{*1}	1.35	1.40	1.45		
			CN4-0 = 18H ^{*1}	1.37	1.42	1.47		
			CN4-0 = 19H ^{*1}	1.39	1.44	1.49		
			CN4-0 = 1AH ^{*1}	1.41	1.46	1.51		
			CN4-0 = 1BH ^{*1}	1.43	1.48	1.53		
			CN4-0 = 1CH ^{*1}	1.45	1.50	1.55		
			CN4-0 = 1DH ^{*1}	1.47	1.52	1.57		
			CN4-0 = 1EH ^{*1}	1.49	1.54	1.59		
			CN4-0 = 1FH ^{*1}	1.51	1.56	1.61		
V_{L1} temperature deviation	ΔV_{L1}	$V_{DD} = 3.0V$		—	-1.5	—	mV/°C	
V_{L1} voltage dependency	ΔV_{L1}	$V_{DD} = 1.3$ to $3.6V$		—	5	20	mV/V	
V_{L2} voltage ^{*2}	V_{L2}	$V_{DD} = 3.0V$, $T_j = 25^\circ C$, 500k Ω load ($V_{L4} - V_{SS}$)		Typ. -10%	$V_{L1} \times 2$	Typ. +4%	V	
V_{L3} voltage ^{*2}	V_{L3}	$V_{DD} = 3.0V$, $T_j = 25^\circ C$ 500k Ω load ($V_{L4} - V_{SS}$)	1/3 bias	Typ. -10%	$V_{L1} \times 2$	Typ. +4%		
			1/4 bias	Typ. -10%	$V_{L1} \times 3$	Typ. +4%		
V_{L4} voltage ^{*2}	V_{L4}		1/3 bias	Typ. -10%	$V_{L1} \times 3$	Typ. +5%		
			1/4 bias	Typ. -10%	$V_{L1} \times 4$	Typ. +5%		
LCD bias voltage generation time	T_{BIAS}	—		—	—	600	ms	

^{*1}: When using 1/4 bias, the V_{L1} voltage is set to typ. 1.32 V (same voltage as in CN4-0 = 13H).

^{*2}: Boost clock is 2kHz(initial) for the bias generation. C12=C34=1uF.

DC CHARACTERISTICS (3/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
BLD threshold voltage	V_{BLD}	$V_{DD} = 1.35$ to $3.6V$	LD2-0 = 0H	Typ. -2%	1.35	Typ. +2%	V	1
			LD2-0 = 1H		1.4			
			LD2-0 = 2H		1.45			
			LD2-0 = 3H		1.5			
			LD2-0 = 4H		1.6			
			LD2-0 = 5H		1.7			
			LD2-0 = 6H		1.8			
			LD2-0 = 7H		1.9			
			LD2-0 = 8H		2.0			
			LD2-0 = 9H		2.1			
			LD2-0 = 0AH		2.2			
			LD2-0 = 0BH		2.3			
			LD2-0 = 0CH		2.4			
			LD2-0 = 0DH		2.5			
			LD2-0 = 0EH		2.7			
			LD2-0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	$V_{DD} = 1.35$ to $3.6V$		—	0	—	%/ $^\circ C$	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	$T_a = 25^\circ C$	—	0.15	0.50	μA	1
			$T_a = -20$ to $+70^\circ C$	—	—	2.50		
			$T_a = -40$ to $+85^\circ C$	—	—	5.00		
Supply current 2	IDD2	CPU: In HALT state (LTBC, WDT: Operating ^{*3*5}). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	$T_a = 25^\circ C$	—	0.5	1.3	μA	
			$T_a = -20$ to $+70^\circ C$	—	—	3.5		
			$T_a = -40$ to $+85^\circ C$	—	—	6.0		
Supply current 3	IDD3	CPU: In 32.768kHz operating state. ^{*1*3} High-speed oscillation: Stopped. LCD/BIAS circuits: Operating. ^{*2}	$T_a = 25^\circ C$	—	5	7	μA	
			$T_a = -20$ to $+70^\circ C$	—	—	12		
			$T_a = -40$ to $+85^\circ C$	—	—	16		
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating. ^{*2}	$T_a = 25^\circ C$	—	70	85	μA	
			$T_a = -20$ to $+70^\circ C$	—	—	100		
			$T_a = -40$ to $+85^\circ C$	—	—	120		
Supply current 5	IDD5	CPU: In 4.096MHz operating state. ^{*2*3} PLL: In oscillating state. LCD/BIAS circuits: Operating. ^{*2} $V_{DD} = 1.8$ to $3.6V$	$T_a = 25^\circ C$	—	0.8	1.0	mA	
			$T_a = -20$ to $+70^\circ C$	—	—	1.2		
			$T_a = -40$ to $+85^\circ C$	—	—	1.2		
Supply current 6	IDD6	CPU: In 4.096MHz operating state. ^{*2} PLL: In oscillating state. ^{*3*4} A/D: In operating state. LCD/BIAS circuits: Operating. ^{*2} $V_{DD} = AV_{DD} = 3.0V$	$T_a = 25^\circ C$	—	1.5	1.6	mA	
			$T_a = -20$ to $+70^\circ C$	—	—	2.5		
			$T_a = -40$ to $+85^\circ C$	—	—	2.5		

^{*1} : When the CPU operating rate is 100% (No HALT state).

^{*2} : All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

^{*3} : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance $C_{GL}/C_{DL} = 0pF$.

^{*4} : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).

^{*5} : Significant bits of BLKCON0~BLKCON4 registers are all "1".

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (4/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input current 1 (RESET_N)	IIH1	$V_{IH1} = V_{DD}$		0	—	1	μA 4
	IIL1	$V_{IL1} = V_{SS}$	$V_{DD} = 1.8$ to $3.6V$	-600	-300	-20	
			$V_{DD} = 1.3$ to $3.6V$	-600	-300	-10	
			$V_{DD} = 1.1$ to $3.6V$	-600	-300	-2	
Input current 1 (TEST)	IIH1	$V_{IH1} = V_{DD}$	$V_{DD} = 1.8$ to $3.6V$	20	300	600	
			$V_{DD} = 1.3$ to $3.6V$	10	300	600	
			$V_{DD} = 1.1$ to $3.6V$	2	300	600	
	IIL1	$V_{IL1} = V_{SS}$		-1	—	—	
Input current 2 (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7) ^{*1}	IIH2	$V_{IH2} = V_{DD}$ (when pulled-down)	$V_{DD} = 1.8$ to $3.6V$	2	30	200	
			$V_{DD} = 1.3$ to $3.6V$	0.2	30	200	
			$V_{DD} = 1.1$ to $3.6V$	0.01	30	200	
	IIL2	$V_{IL2} = V_{SS}$ (when pulled-up)	$V_{DD} = 1.8$ to $3.6V$	-200	-30	-2	
			$V_{DD} = 1.3$ to $3.6V$	-200	-30	-0.2	
			$V_{DD} = 1.1$ to $3.6V$	-200	-30	-0.01	
	IIH2Z	$V_{IH2} = V_{DD}$ (in high-impedance state)		—	—	1	
	IIL2Z	$V_{IL2} = V_{SS}$ (in high-impedance state)		-1	—	—	

^{*1}: ML610Q421 only

DC CHARACTERISTICS (5/5)

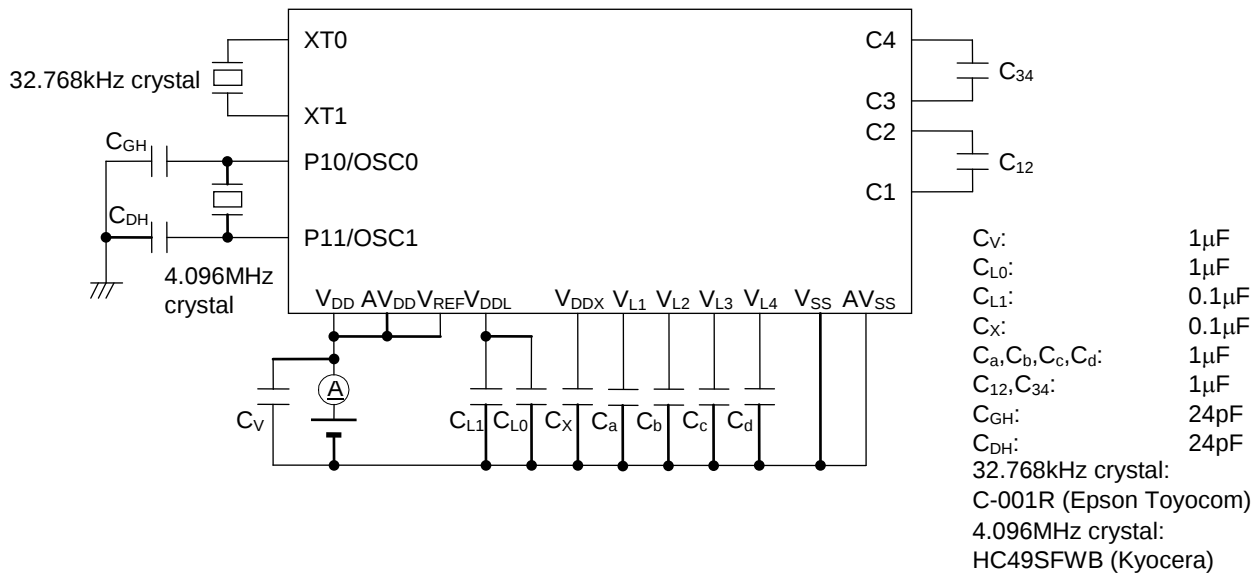
($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (5/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7) ^{*1}	VIH1	$V_{DD} = 1.3$ to $3.6V$	0.7 $\times V_{DD}$	—	V_{DD}	V	5
		$V_{DD} = 1.1$ to $3.6V$	0.7 $\times V_{DD}$	—	V_{DD}		
	VIL1	$V_{DD} = 1.3$ to $3.6V$	0	—	0.3 $\times V_{DD}$		
		$V_{DD} = 1.1$ to $3.6V$	0	—	0.2 $\times V_{DD}$		
Input voltage 2 (P30, P44)	VIH2	—	0.7 $\times V_{DD}$	—	V_{DD}	pF	—
	VIL2	—	0	—	0.3 $\times V_{DD}$		
Input pin capacitance (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7) ^{*1}	CIN	$f = 10kHz$ $V_{rms} = 50mV$ $T_a = 25^\circ C$	—	—	5	pF	—

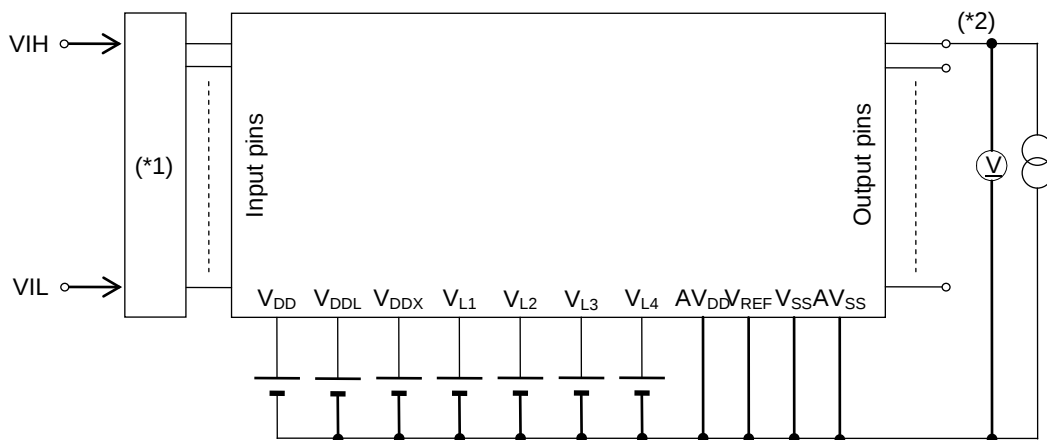
^{*1}: ML610Q421 only

MEASURING CIRCUITS

MEASURING CIRCUIT 1



MEASURING CIRCUIT 2



(*1) Input logic circuit to determine the specified measuring conditions.

(*2) Measured at the specified output pins.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q421-01	Jul. 29, 2009	–	–	Final edition 1
FEDL610Q421-02	Dec. 3, 2010	–	–	Add to B version
FEDL610Q421-03	Feb. 9, 2015	All	All	Change header
		3,4	3,4	Delete B version
		4	4	Change from "Shipment" to " Product name – Supported Function "
		–	22	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		22	23	Change "RESET" to " Reset pulse width (P_{RST})" and " Power-on reset activation power rise time (T_{POR})".
		36	37	Change description in Note.

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