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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	4.2MHz
Connectivity	I ² C, SSP, UART/USART
Peripherals	LCD, Melody Driver, POR, PWM, WDT
Number of I/O	14
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 2x12b, 2x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q422p-nnntb0arl

- 1 kHz timer
 - 10 Hz/1 Hz interrupt function
- Capture
 - Time base capture × 2 channels (4096 Hz to 32 Hz)
- PWM
 - Resolution 16 bits × 1 channel
- Synchronous serial port
 - Master/slave selectable
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
- UART
 - TXD/RXD × 1 channel
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- I²C bus interface
 - Master function only
 - Fast mode (400 kbps@4MHz), standard mode (100 kbps@1MHz, 50kbps@500kHz)
- Melody driver
 - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
 - Tone length: 63 types
 - Tempo: 15 types
 - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)
- RC oscillation type A/D converter
 - 24-bit counter
 - Time division × 2 channels
- Successive approximation type A/D converter
 - 12-bit A/D converter
 - Input × 2 channels
- General-purpose ports
 - Non-maskable interrupt input port × 1 channel
 - Input-only port × 6 channels (including secondary functions)
 - Output-only port × 3 channels (including secondary functions)
 - Input/output port
 - ML610Q421: 22 channels (including secondary functions)
 - ML610Q422: 14 channels (including secondary functions)

●Product name – Supported Function

The line-up of the ML610Q421 and the ML610Q422 is below.

- Chip (Die) -	ROM type	Operating temperature	Product availability
ML610Q421-xxxWA	Flash ROM	-20°C to +70°C	Yes
ML610Q422-xxxWA	Flash ROM	-20°C to +70°C	Yes
ML610Q421P-xxxWA	Flash ROM	-40°C to +85°C	Yes
ML610Q422P-xxxWA	Flash ROM	-40°C to +85°C	Yes

-120-pin plastic TQFP -	ROM type	Operating temperature	Product availability
ML610Q421-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q422-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q421P-xxxTB	Flash ROM	-40°C to +85°C	Yes
ML610Q422P-xxxTB	Flash ROM	-40°C to +85°C	Yes

xxx: ROM code number (xxx of the blank product is NNN)

Q: Flash ROM version

P: Wide range temperature version (P version)

WA: Chip (Die),

TB: TQFP

BLOCK DIAGRAM**ML610Q421 Block Diagram**

Figure 1 show the block diagram of the ML610Q421.

"*" indicates the secondary function of each port.

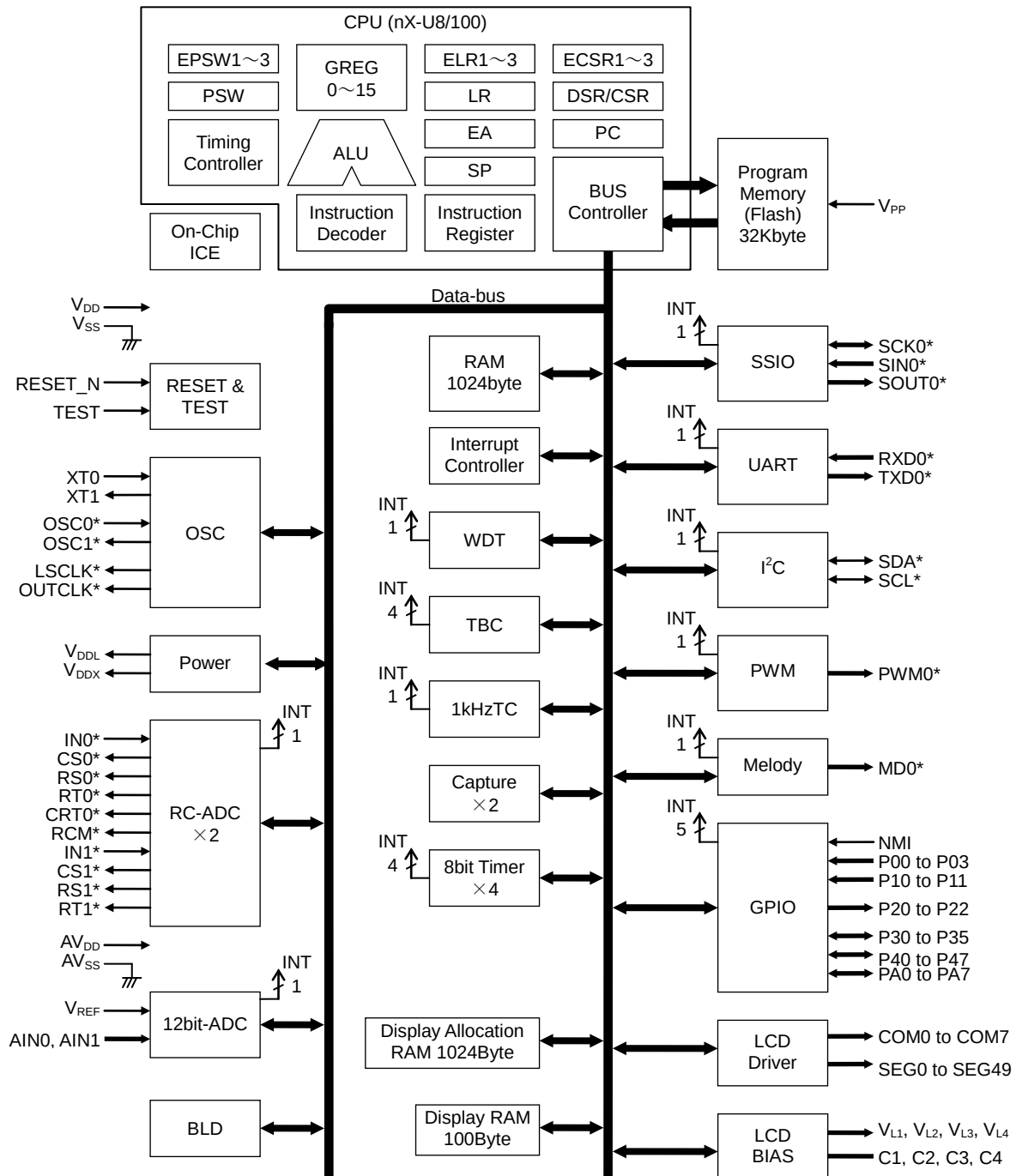


Figure 1 ML610Q421 Block Diagram

ML610Q422 Block Diagram

Figure 2 show the block diagram of the ML610Q422.

"*" indicates the secondary function of each port.

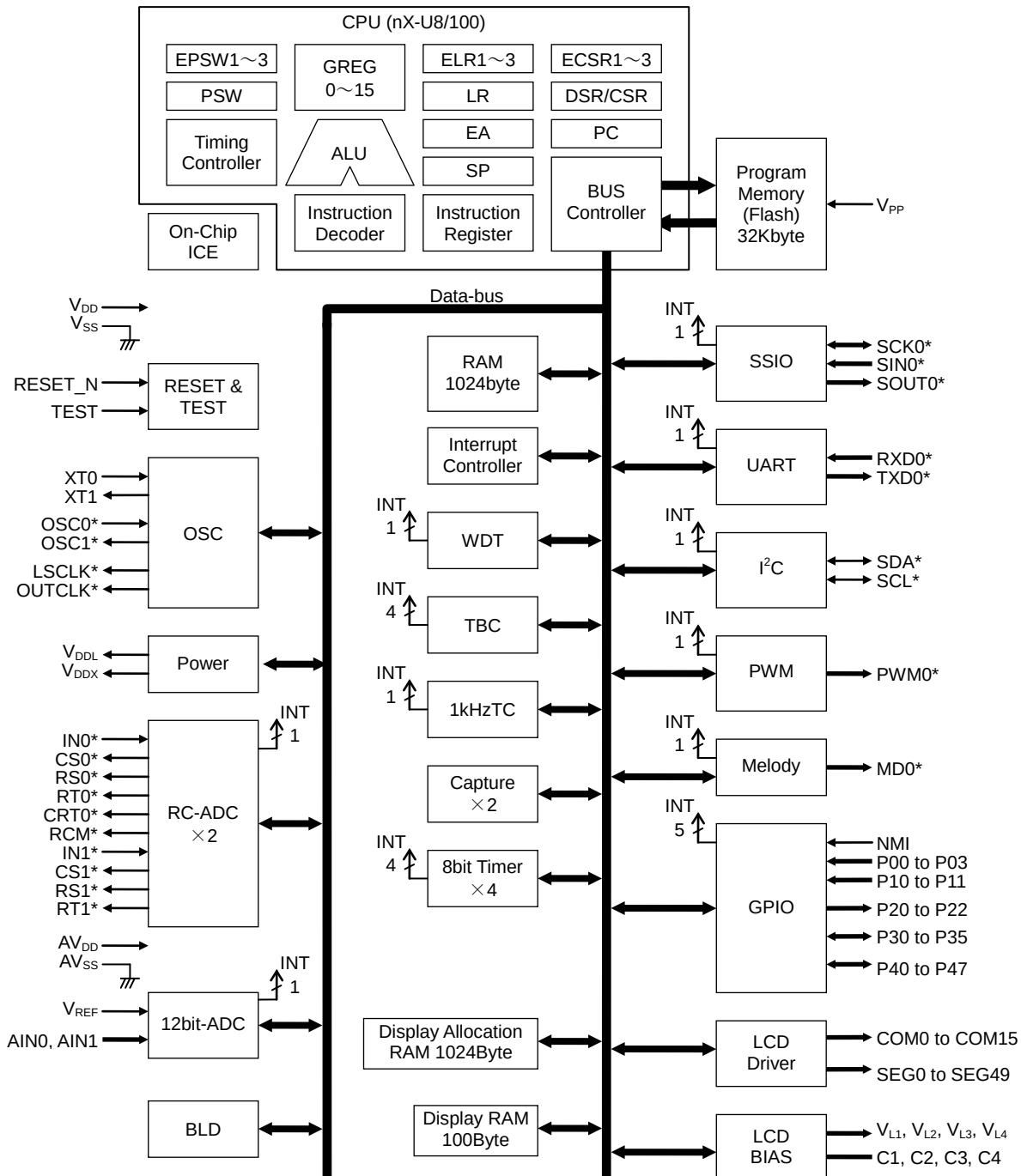
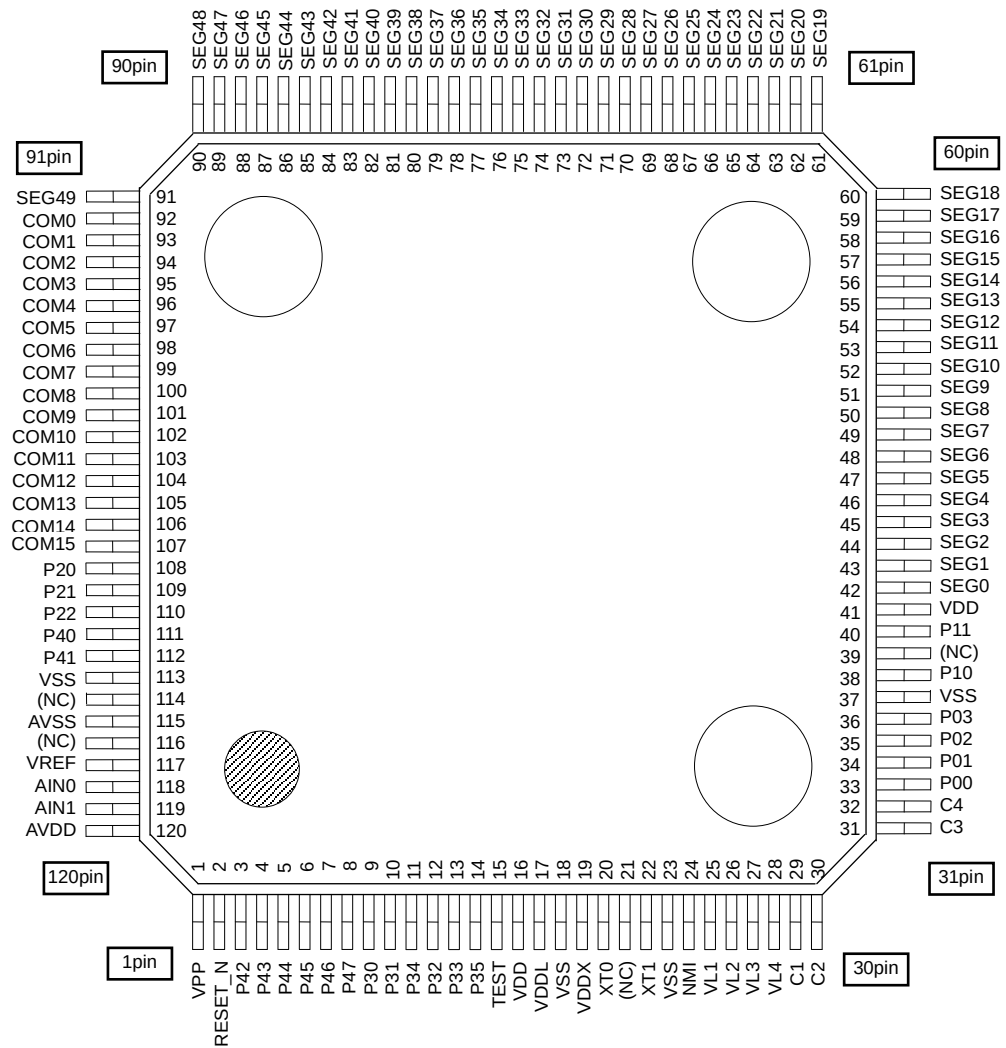


Figure 2 ML610Q422 Block Diagram

ML610Q422 TQFP120 Pin Layout



Note:

The assignment of the pads P30 to P35 are not in order.

Figure 4 ML610Q422 TQFP120 Pin Configuration

ML610Q422 Pad Coordinates

Table 2 ML610Q422 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)
1	VPP	-1240	-1404	51	SEG11	1384	640	101	COM11	-1384	240
2	RESET_N	-1160	-1404	52	SEG12	1384	720	102	COM12	-1384	160
3	P42	-1080	-1404	53	SEG13	1384	800	103	COM13	-1384	80
4	P43	-1000	-1404	54	SEG14	1384	880	104	COM14	-1384	0
5	P44	-920	-1404	55	SEG15	1384	960	105	COM15	-1384	-80
6	P45	-840	-1404	56	SEG16	1384	1040	106	P20	-1384	-200
7	P46	-760	-1404	57	SEG17	1384	1120	107	P21	-1384	-280
8	P47	-680	-1404	58	SEG18	1384	1200	108	P22	-1384	-360
9	P30	-600	-1404	59	SEG19	1160	1404	109	P40	-1384	-440
10	P31	-520	-1404	60	SEG20	1080	1404	110	P41	-1384	-520
11	P34	-440	-1404	61	SEG21	1000	1404	111	Vss	-1384	-600
12	P32	-360	-1404	62	SEG22	920	1404	112	AVss	-1384	-680
13	P33	-280	-1404	63	SEG23	840	1404	113	VREF	-1384	-840
14	P35	-200	-1404	64	SEG24	760	1404	114	AIN0	-1384	-920
15	TEST	-120	-1404	65	SEG25	680	1404	115	AIN1	-1384	-1092
16	VDD	-40	-1404	66	SEG26	600	1404	116	AVDD	-1384	-1172
17	VDDL	40	-1404	67	SEG27	520	1404				
18	Vss	120	-1404	68	SEG28	440	1404				
19	VDDX	200	-1404	69	SEG29	360	1404				
20	XT0	360	-1404	70	SEG30	280	1404				
21	XT1	520	-1404	71	SEG31	200	1404				
22	Vss	600	-1404	72	SEG32	120	1404				
23	NMI	680	-1404	73	SEG33	40	1404				
24	VL1	840	-1404	74	SEG34	-40	1404				
25	VL2	920	-1404	75	SEG35	-120	1404				
26	VL3	1000	-1404	76	SEG36	-200	1404				
27	VL4	1080	-1404	77	SEG37	-280	1404				
28	C1	1160	-1404	78	SEG38	-360	1404				
29	C2	1240	-1404	79	SEG39	-440	1404				
30	C3	1384	-1240	80	SEG40	-520	1404				
31	C4	1384	-1160	81	SEG41	-600	1404				
32	P00	1384	-1040	82	SEG42	-680	1404				
33	P01	1384	-960	83	SEG43	-760	1404				
34	P02	1384	-880	84	SEG44	-840	1404				
35	P03	1384	-800	85	SEG45	-920	1404				
36	Vss	1384	-660	86	SEG46	-1000	1404				
37	P10	1384	-580	87	SEG47	-1080	1404				
38	P11	1384	-420	88	SEG48	-1160	1404				
39	VDD	1384	-340	89	SEG49	-1384	1200				
40	SEG0	1384	-240	90	COM0	-1384	1120				
41	SEG1	1384	-160	91	COM1	-1384	1040				
42	SEG2	1384	-80	92	COM2	-1384	960				
43	SEG3	1384	0	93	COM3	-1384	880				
44	SEG4	1384	80	94	COM4	-1384	800				
45	SEG5	1384	160	95	COM5	-1384	720				
46	SEG6	1384	240	96	COM6	-1384	640				
47	SEG7	1384	320	97	COM7	-1384	560				
48	SEG8	1384	400	98	COM8	-1384	480				
49	SEG9	1384	480	99	COM9	-1384	400				
50	SEG10	1384	560	100	COM10	-1384	320				

PIN LIST

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
18,22, 36,111	18,22, 37,111	V _{SS}	—	Negative power supply pin	—	—	—	—	—	—
16,39	16,39	V _{DD}	—	Positive power supply pin	—	—	—	—	—	—
17	17	V _{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
19	19	V _{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
1	1	V _{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
112	112	AV _{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
116	116	AV _{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
24	24	V _{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
25	25	V _{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
26	26	V _{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
27	27	V _{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
28	28	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
29	29	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
30	30	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
31	31	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
15	15	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
2	2	RESET_N	I	Reset input pin	—	—	—	—	—	—
20	20	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
21	21	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
113	113	V _{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q422	Q421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
76	76	SEG36	O	LCD segment pin	—	—	—	—	—	—
77	77	SEG37	O	LCD segment pin	—	—	—	—	—	—
78	78	SEG38	O	LCD segment pin	—	—	—	—	—	—
79	79	SEG39	O	LCD segment pin	—	—	—	—	—	—
80	80	SEG40	O	LCD segment pin	—	—	—	—	—	—
81	81	SEG41	O	LCD segment pin	—	—	—	—	—	—
82	82	SEG42	O	LCD segment pin	—	—	—	—	—	—
83	83	SEG43	O	LCD segment pin	—	—	—	—	—	—
84	84	SEG44	O	LCD segment pin	—	—	—	—	—	—
85	85	SEG45	O	LCD segment pin	—	—	—	—	—	—
86	86	SEG46	O	LCD segment pin	—	—	—	—	—	—
87	87	SEG47	O	LCD segment pin	—	—	—	—	—	—
88	88	SEG48	O	LCD segment pin	—	—	—	—	—	—
89	89	SEG49	O	LCD segment pin	—	—	—	—	—	—

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
I²C bus interface				
SDA	I/O	I ² C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I ² C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/ negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software.	Primary	Positive/ negative
CAP1	I	These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/ negative
LED drive				
LED0-2	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
CRT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
Successive approximation type A/D converter				
AV _{SS}	—	Negative power supply pin for successive approximation type A/D converter.	—	—
AV _{DD}	—	Positive power supply pin for successive approximation type A/D converter.	—	—
V _{REF}	—	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0	I	Channel 0 analog input for successive approximation type A/D converter.	—	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter.	—	—
LCD drive signal				
COM0-7	O	Common output pins.	—	—
COM8-15	O	Common output pins. These pins are for the ML610Q422, but are not provided in the ML610Q421.	—	—
SEG0-49	O	Segment output pin.	—	—
LCD driver power supply				
V _{L1}	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, Cc, and Cd (see measuring circuit 1) are connected between V _{SS} and V _{L1} , V _{L2} , V _{L3} , and V _{L4} , respectively.	—	—
V _{L2}	—		—	—
V _{L3}	—		—	—
V _{L4}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 and C34 (see measuring circuit 1) are connected between C1 and C2 and between C3 and C4, respectively.	—	—
C2	—		—	—
C3	—		—	—
C4	—		—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V _{SS}	—	Negative power supply pin.	—	—
V _{DD}	—	Positive power supply pin.	—	—
V _{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V _{SS} .	—	—
V _{DDX}	—	Plus-side power supply pin (internally generated) for low-speed oscillation. Capacitor Cx (see measuring circuit 1) is connected between this pin and V _{SS} .	—	—
V _{PP}	—	Power supply pin for programming Flash ROM. A pull-up resistor is internally connected.	—	—

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 2	AV _{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 3	V _{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 4	V _{DDL}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 5	V _{DDX}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 6	V _{L1}	Ta = 25°C	−0.3 to +1.75	V
Power supply voltage 7	V _{L2}	Ta = 25°C	−0.3 to +3.5	V
Power supply voltage 8	V _{L3}	Ta = 25°C	−0.3 to +5.25	V
Power supply voltage 9	V _{L4}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V _{IN}	Ta = 25°C	−0.3 to V _{DD} +0.3	V
Output voltage	V _{OUT}	Ta = 25°C	−0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port3−A, Ta = 25°C	−12 to +11	mA
Output current 2	I _{OUT2}	Port2, Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	1.25	W
Storage temperature	T _{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	ML610Q421, ML610Q422	−20 to +70	°C
		ML610Q421P, ML610Q422P	−40 to +85	
Operating voltage	V _{DD}	—	1.1 to 3.6	V
	AV _{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f _{OP}	V _{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V _{DD} = 1.3 to 3.6V	30k to 650k	
		V _{DD} = 1.8 to 3.6V	30k to 4.2M	
Capacitor externally connected to V _{DDL} pin	C _{L0}	—	1.0±30%	μF
	C _{L1}	—	0.1±30%	
Capacitor externally connected to V _{DDX} pin	C _X	—	0.1±30%	μF
Capacitors externally connected to V _{L1} , 2, 3, 4 pins	C _{a, b, c, d}	—	1.0±30%	μF
Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins	C ₁₂ , C ₃₄	—	1.0±30%	μF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f _{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R _L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor ^{*1}	C _{DL} /C _{GL}	C _L =6pF of crystal oscillation ^{*2}	—	0	—	pF
		C _L =9pF of crystal oscillation	—	6	—	
		C _L =12pF of crystal oscillation	—	12	—	
High-speed crystal/ceramic oscillation frequency	f _{XTH}	—	—	4.0M / 4.096M	—	Hz
High-speed crystal oscillation external capacitor	C _{DH}	—	—	24	—	pF
	C _{GH}	—	—	24	—	

^{*1}: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.

^{*2}: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	At write/erase	0 to +40	°C
Operating voltage	V _{DD}	At write/erase ^{*1}	2.75 to 3.6	V
	V _{DDL}	At write/erase ^{*1}	2.5 to 2.75	
	V _{PP}	At write/erase ^{*1}	7.7 to 8.3	
Write cycles	C _{EP}	—	80	cycles
Data retention	Y _{DR}	—	10	years

^{*1}: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and erasing Flash ROM.
V_{PP} pin has an internal pulldown resistor.

DC CHARACTERISTICS (3/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
BLD threshold voltage	V_{BLD}	$V_{DD} = 1.35$ to $3.6V$	LD2-0 = 0H	Typ. -2%	1.35	Typ. +2%	V	1
			LD2-0 = 1H		1.4			
			LD2-0 = 2H		1.45			
			LD2-0 = 3H		1.5			
			LD2-0 = 4H		1.6			
			LD2-0 = 5H		1.7			
			LD2-0 = 6H		1.8			
			LD2-0 = 7H		1.9			
			LD2-0 = 8H		2.0			
			LD2-0 = 9H		2.1			
			LD2-0 = 0AH		2.2			
			LD2-0 = 0BH		2.3			
			LD2-0 = 0CH		2.4			
			LD2-0 = 0DH		2.5			
			LD2-0 = 0EH		2.7			
			LD2-0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	$V_{DD} = 1.35$ to $3.6V$		—	0	—	%/ $^\circ C$	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	$T_a = 25^\circ C$	—	0.15	0.50	μA	1
			$T_a = -20$ to $+70^\circ C$	—	—	2.50		
			$T_a = -40$ to $+85^\circ C$	—	—	5.00		
Supply current 2	IDD2	CPU: In HALT state (LTBC, WDT: Operating ^{*3*5}). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	$T_a = 25^\circ C$	—	0.5	1.3	μA	
			$T_a = -20$ to $+70^\circ C$	—	—	3.5		
			$T_a = -40$ to $+85^\circ C$	—	—	6.0		
Supply current 3	IDD3	CPU: In 32.768kHz operating state. ^{*1*3} High-speed oscillation: Stopped. LCD/BIAS circuits: Operating. ^{*2}	$T_a = 25^\circ C$	—	5	7	μA	
			$T_a = -20$ to $+70^\circ C$	—	—	12		
			$T_a = -40$ to $+85^\circ C$	—	—	16		
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating. ^{*2}	$T_a = 25^\circ C$	—	70	85	μA	
			$T_a = -20$ to $+70^\circ C$	—	—	100		
			$T_a = -40$ to $+85^\circ C$	—	—	120		
Supply current 5	IDD5	CPU: In 4.096MHz operating state. ^{*2*3} PLL: In oscillating state. LCD/BIAS circuits: Operating. ^{*2} $V_{DD} = 1.8$ to $3.6V$	$T_a = 25^\circ C$	—	0.8	1.0	mA	
			$T_a = -20$ to $+70^\circ C$	—	—	1.2		
			$T_a = -40$ to $+85^\circ C$	—	—	1.2		
Supply current 6	IDD6	CPU: In 4.096MHz operating state. ^{*2} PLL: In oscillating state. ^{*3*4} A/D: In operating state. LCD/BIAS circuits: Operating. ^{*2} $V_{DD} = AV_{DD} = 3.0V$	$T_a = 25^\circ C$	—	1.5	1.6	mA	
			$T_a = -20$ to $+70^\circ C$	—	—	2.5		
			$T_a = -40$ to $+85^\circ C$	—	—	2.5		

^{*1} : When the CPU operating rate is 100% (No HALT state).

^{*2} : All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

^{*3} : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance $C_{GL}/C_{DL} = 0pF$.

^{*4} : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).

^{*5} : Significant bits of BLKCON0~BLKCON4 registers are all "1".

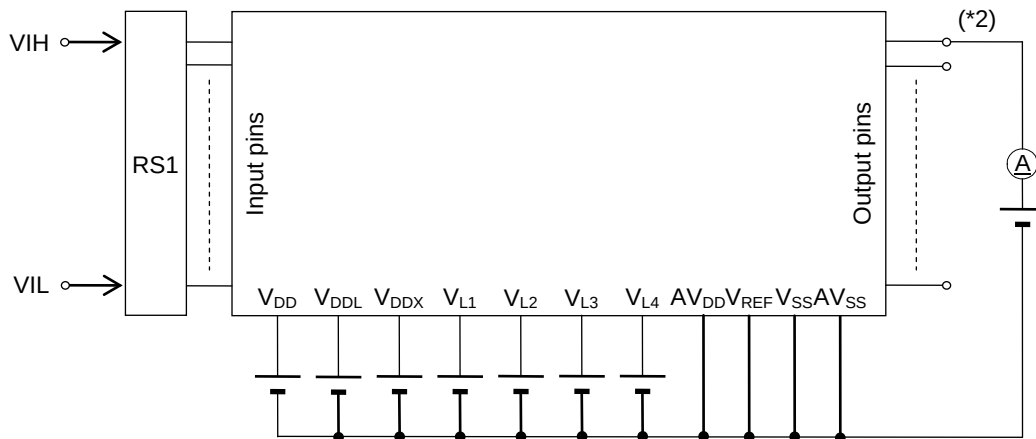
DC CHARACTERISTICS (4/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified) (4/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20–P22/2 nd function is selected) (P30–P36) (P40–P47) (PA0–PA7) ^{*1}	VOH1	IOH1 = $-0.5mA$, $V_{DD} = 1.8$ to $3.6V$	$V_{DD} - 0.5$	—	—	V	2
		IOH1 = $-0.1mA$, $V_{DD} = 1.3$ to $3.6V$	$V_{DD} - 0.3$	—	—		
		IOH1 = $-0.03mA$, $V_{DD} = 1.1$ to $3.6V$	$V_{DD} - 0.3$	—	—		
	VOL1	IOL1 = $+0.5mA$, $V_{DD} = 1.8$ to $3.6V$	—	—	0.5		
		IOL1 = $+0.1mA$, $V_{DD} = 1.3$ to $3.6V$	—	—	0.5		
		IOL1 = $+0.03mA$, $V_{DD} = 1.1$ to $3.6V$	—	—	0.3		
Output voltage 2 (P20–P22/2 nd function is Not selected)	VOH2	IOH1 = $-0.5mA$, $V_{DD} = 1.8$ to $3.6V$	$V_{DD} - 0.5$	—	—		
		IOH1 = $-0.1mA$, $V_{DD} = 1.3$ to $3.6V$	$V_{DD} - 0.3$	—	—		
		IOH1 = $-0.03mA$, $V_{DD} = 1.1$ to $3.6V$	$V_{DD} - 0.3$	—	—		
	VOL2	IOL2 = $+5mA$, $V_{DD} = 1.8$ to $3.6V$	—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = $+3mA$, $V_{DD} = 2.0$ to $3.6V$ (when I ² C mode is selected)	—	—	0.4		
Output voltage 4 (COM0–15) (SEG0–49)	VOH4	IOH4 = $-0.2mA$, $V_{L1} = 1.2V$	$V_{L4} - 0.2$	—	—		
	VOMH4	IOMH4 = $+0.2mA$, $V_{L1} = 1.2V$	—	—	$V_{L3} + 0.2$		
	VOMH4S	IOMH4S = $-0.2mA$, $V_{L1} = 1.2V$	$V_{L3} - 0.2$	—	—		
	VOM4	IOM4 = $+0.2mA$, $V_{L1} = 1.2V$	—	—	$V_{L2} + 0.2$		
	VOM4S	IOM4S = $-0.2mA$, $V_{L1} = 1.2V$	$V_{L2} - 0.2$	—	—		
	VOML4	IOML4 = $+0.2mA$, $V_{L1} = 1.2V$	—	—	$V_{L1} + 0.2$		
	VOML4S	IOML4S = $-0.2mA$, $V_{L1} = 1.2V$	$V_{L1} - 0.2$	—	—		
	VOL4	IOL4 = $+0.2mA$, $V_{L1} = 1.2V$	—	—	0.2		
Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA7) ^{*1}	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	-1	—	—		

^{*1}: ML610Q421 only

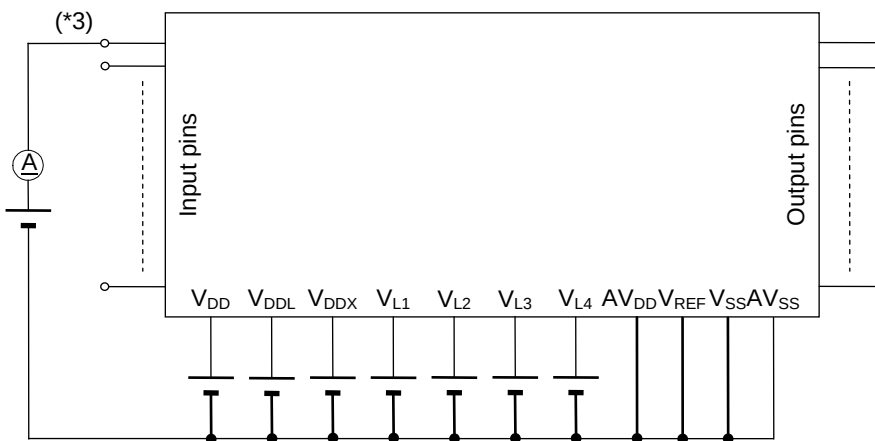
MEASURING CIRCUIT 3



*1: Input logic circuit to determine the specified measuring conditions.

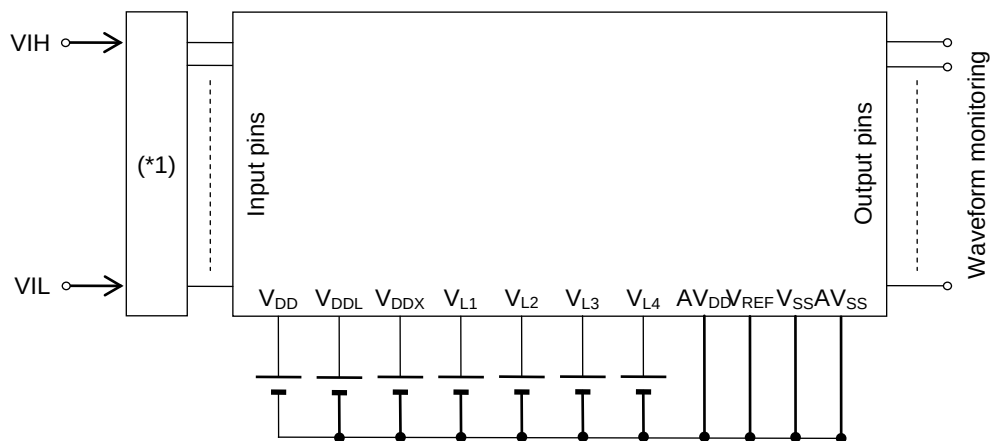
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

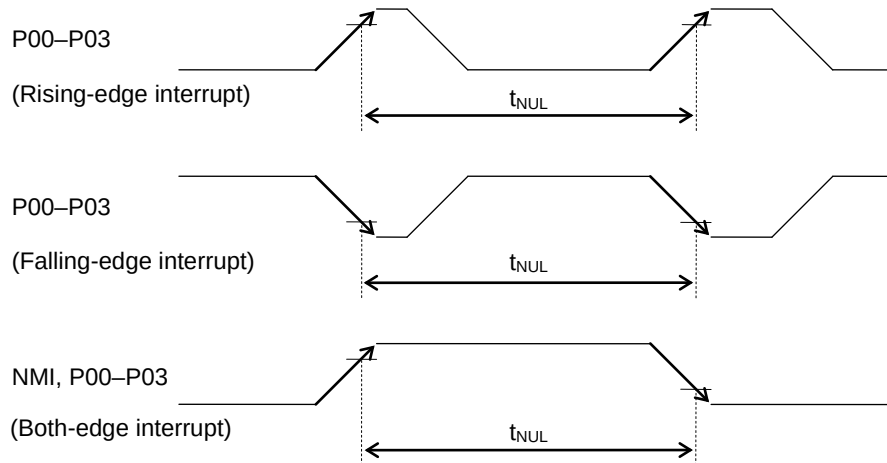


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

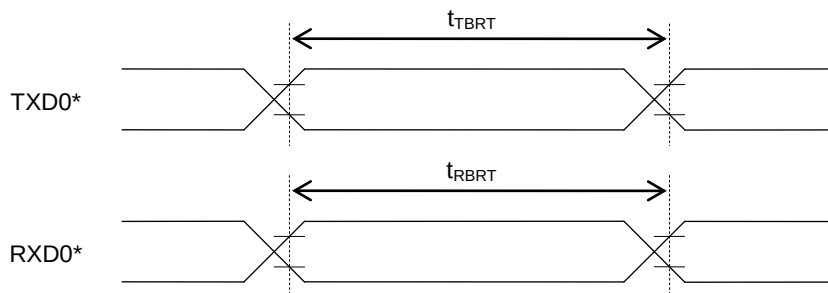
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled ($MIE = 1$), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

**AC CHARACTERISTICS (UART)**

($V_{DD} = 1.3$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT^{*1}	—	s
Receive baud rate	t_{RBRT}	—	BRT^{*1} –3%	BRT^{*1}	BRT^{*1} +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the UART0 baud rate register (UA0BRTL,H) and the UART0 mode register 0 (UA0MOD0).



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

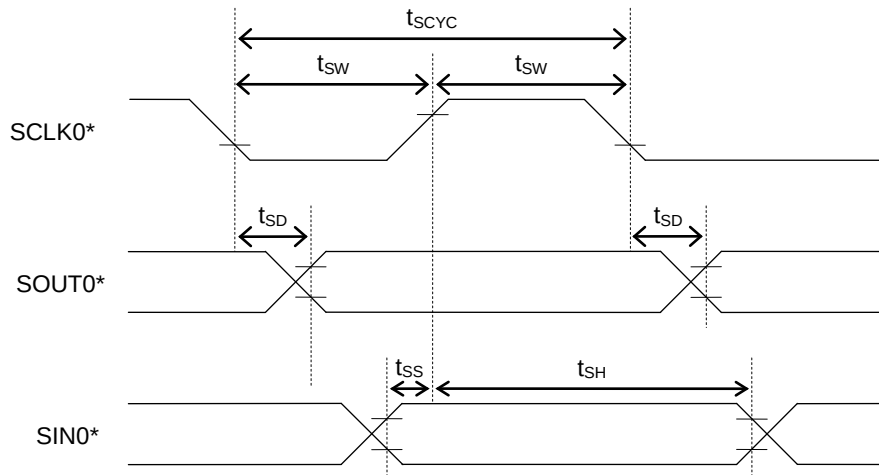
($V_{DD} = 1.3$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When RC oscillation is active* ² ($V_{DD} = 1.3$ to $3.6V$)	10	—	—	μs
		When high-speed oscillation is active* ³ ($V_{DD} = 1.8$ to $3.6V$)	1	—	—	μs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK* ¹	—	s
SCLK input pulse width (slave mode)	t_{SW}	When RC oscillation is active* ² ($V_{DD} = 1.3$ to $3.6V$)	4	—	—	μs
		When high-speed oscillation is active* ³ ($V_{DD} = 1.8$ to $3.6V$)	0.4	—	—	μs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK* ¹ $\times 0.4$	SCLK* ¹ $\times 0.5$	SCLK* ¹ $\times 0.6$	s
SOUT output delay time (slave mode)	t_{SD}	When RC oscillation is active* ² ($V_{DD} = 1.3$ to $3.6V$)	—	—	500	ns
		When high-speed oscillation is active* ³ ($V_{DD} = 1.8$ to $3.6V$)	—	—	240	
SOUT output delay time (master mode)	t_{SD}	When RC oscillation is active* ² ($V_{DD} = 1.3$ to $3.6V$)	—	—	500	ns
		When high-speed oscillation is active* ³ ($V_{DD} = 1.8$ to $3.6V$)	—	—	240	
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	When RC oscillation is active* ² ($V_{DD} = 1.3$ to $3.6V$)	500	—	—	ns
		When high-speed oscillation is active* ³ ($V_{DD} = 1.8$ to $3.6V$)	240	—	—	
SIN input hold time	t_{SH}	When RC oscillation is active* ² ($V_{DD} = 1.3$ to $3.6V$)	300	—	—	ns
		When high-speed oscillation is active* ³ ($V_{DD} = 1.8$ to $3.6V$)	80	—	—	

*¹: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)

*²: When RC oscillation is selected with OSCM1–0 of the frequency control register (FCON0)

*³: When Crystal/ceramic oscillation, built-in PLL oscillation, or external clock input is selected with OSCM1–0 of the frequency control register (FCON0)



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I²C Bus Interface: Standard Mode 100kHz)

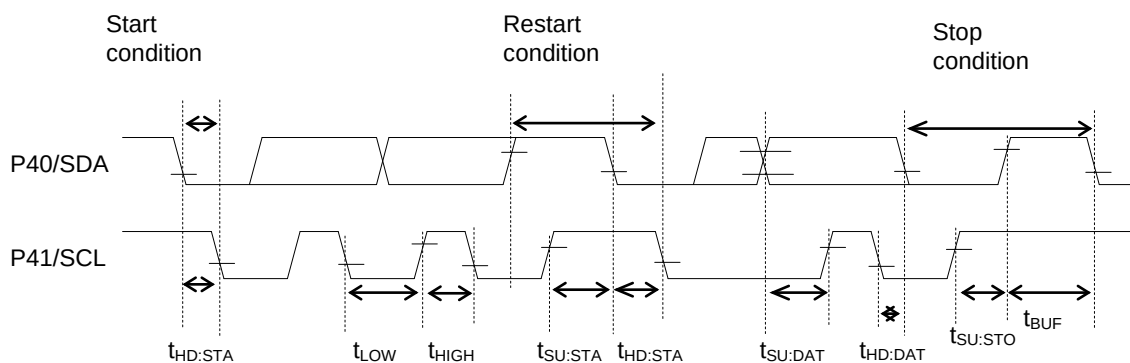
($V_{DD} = 1.8$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	μs
SCL "L" level time	t_{LOW}	—	4.7	—	—	μs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	μs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	μs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	μs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	μs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	μs
Bus-free time	t_{BUF}	—	4.7	—	—	μs

AC CHARACTERISTICS (I²C Bus Interface: Fast Mode 400kHz)

($V_{DD} = 1.8$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	μs
SCL "L" level time	t_{LOW}	—	1.3	—	—	μs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	μs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	μs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	μs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	μs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	μs
Bus-free time	t_{BUF}	—	1.3	—	—	μs

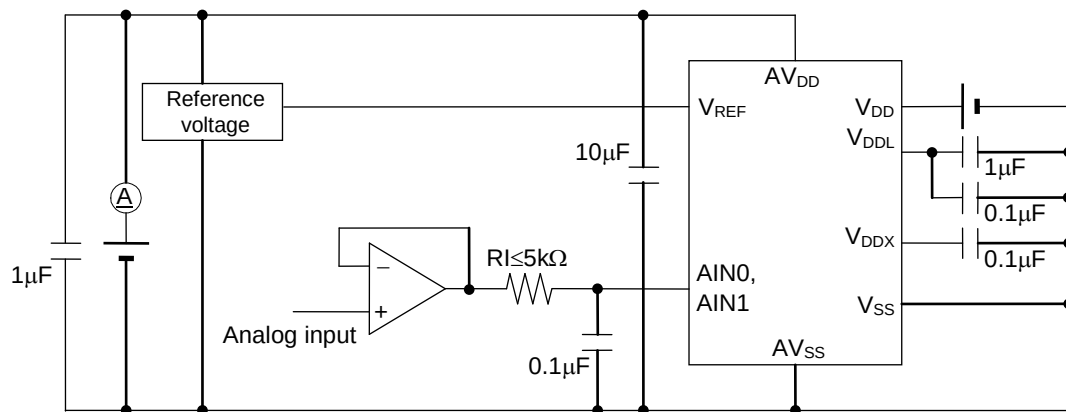


Electrical Characteristics of Successive Approximation Type A/D Converter

($V_{DD} = 1.8$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	$2.7V \leq V_{REF} \leq 3.6V$	-4	—	+4	LSB
		$2.2V \leq V_{REF} \leq 2.7V$	-6	—	+6	
Differential non-linearity error	DNL	$2.7V \leq V_{REF} \leq 3.6V$	-3	—	+3	
		$2.2V \leq V_{REF} \leq 2.7V$	-5	—	+5	
Zero-scale error	V_{OFF}	—	-6	—	+6	
Full-scale error	FSE	—	-6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	SACK = 0 (HSCLK = 375kHz to 625kHz)	—	25	—	ϕ/CH
		SACK = 1 (HSCLK = 1.5MHz to 4.2MHz)	—	112	—	

ϕ : Period of high-speed clock (HSCLK)



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q421-01	Jul. 29, 2009	–	–	Final edition 1
FEDL610Q421-02	Dec. 3, 2010	–	–	Add to B version
FEDL610Q421-03	Feb. 9, 2015	All	All	Change header
		3,4	3,4	Delete B version
		4	4	Change from "Shipment" to " Product name – Supported Function "
		–	22	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		22	23	Change "RESET" to " Reset pulse width (P_{RST})" and " Power-on reset activation power rise time (T_{POR})".
		36	37	Change description in Note.