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Details

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Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	87
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08dz128cll

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Number < Lowest Priorit			ority> Higl	hest		
100	64	48	Pe Pin/In	ort terrupt	Alt 1	Alt 2
26	17	13	PTE2			SS1
27	18	14	PTE3			SPSCK1
28	19	15	PTE4		SCL1 ²	MOSI1
29	20	16	PTE5		SDA1 ²	MISO1
30	21		PTG2			
31	22		PTG3			
32	_	_	PTL6			
33	_		PTL7			
34	23	17	PTF0			TxD2 ³
35	24	18	PTF1			RxD2 ³
36	25	19	PTF2		TPM1CLK	SCL1 ²
37	26	20	PTF3		TPM2CLK	SDA1 ²
38	—					V _{DD}
39	_	_				V _{SS}
40	27		PTG4			
41	28		PTG5			
42	_		PTG6			SCL2
43	_		PTG7			SDA2
44	29	21	PTE6		TxD2 ³	TXCAN
45	30	22	PTE7		RxD2 ³	RxCAN
46	_	_	PTL0			
47	—		PTL1			
48	—		PTL2			
49	31	23	PTD0	PID0		TPM2CH0
50	32	24	PTD1	PID1		TPM2CH1

Table 2-1. Pin Availability by Package Pin-Count (continued)



Chapter 3 Modes of Operation



Chapter 4 Memory

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x00 75	PTKDD	PTKDD7	PTKDD6	PTKDD5	PTKDD4	PTKDD3	PTKDD2	PTKDD1	PTKDD0
0x00 76	PTLD	PTLD7	PTLD6	PTLD5	PTLD4	PTLD3	PTLD2	PTLD1	PTLD0
0x00 77	PTLDD	PTLDD7	PTLDD6	PTLDD5	PTLDD4	PTLDD3	PTLDD2	PTLDD1	PTLDD0
0x00 78	PPAGE	0	0	0	0	0	XA16	XA15	XA14
0x00 79	LAP2	0	0	0	0	0	0	0	LA16
0x00 7A	LAP1	LA15	LA14	LA13	LA12	LA11	LA10	LA9	LA8
0x00 7B	LAP0	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0
0x00 7C	LWP	D7	D6	D5	D4	D3	D2	D1	D0
0x00 7D	LBP	D7	D6	D5	D4	D3	D2	D1	D0
0x00 7E	LB	D7	D6	D5	D4	D3	D2	D1	D0
0x00 7F	LAPAB	D7	D6	D5	D4	D3	D2	D1	D0

Table 4-2. Direct-Page Register Summary (Sheet 4 of 4)

High-page registers, shown in Table 4-3, are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at 0x1800.

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x1800	SRS	POR	PIN	COP	ILOP	ILAD	LOC	LVD	0
0x1801	SBDFR	0	0	0	0	0	0	0	BDFR
0x1802	SOPT1	CO	PT	STOPE	SCI2PS	IIC1PS	0	0	0
0x1803	SOPT2	COPCLKS	COPW	0	ADHTS	0		MCSEL	
0x1804 — 0x1805	Reserved	_	_	_	_	_	_	_	_
0x1806	SDIDH	_	—	_		ID11	ID10	ID9	ID8
0x1807	SDIDL	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0x1808	Reserved	—			—	—	—	—	_
0x1809	SPMSC1	LVWF	LVWACK	LVWIE	LVDRE	LVDSE	LVDE	0	BGBE
0x180A	SPMSC2	0	0	LVDV	LVWV	PPDF	PPDACK	—	PPDC
0x180B– 0x180F	Reserved	_	_	_	_	_	_	_	_
0x1810	DBGCAH	Bit 15	14	13	12	11	10	9	Bit 8
0x1811	DBGCAL	Bit 7	6	5	4	3	2	1	Bit 0
0x1812	DBGCBH	Bit 15	14	13	12	11	10	9	Bit 8
0x1813	DBGCBL	Bit 7	6	5	4	3	2	1	Bit 0
0x1814	DBGCCH	Bit 15	14	13	12	11	10	9	Bit 8
0x1815	DBGCCL	Bit 7	6	5	4	3	2	1	Bit 0
0x1816	DBGFH	Bit 15	14	13	12	11	10	9	Bit 8
0x1817	DBGFL	Bit 7	6	5	4	3	2	1	Bit 0
0x1818	DBGCAX	RWAEN	RWA	PAGSEL	0	0	0	0	Bit 16
0x1819	DBGCBX	RWBEN	RWB	PAGSEL	0	0	0	0	Bit 16

Table 4-3. High-Page Register Summary (Sheet 1 of 5)



Chapter 5 Resets, Interrupts, and General System Control

5.1 Introduction

This section discusses basic reset and interrupt mechanisms and their various sources in the MC9S08DZ128 Series. Some interrupt sources from peripheral modules are discussed in greater detail within other sections of this data sheet. This section gathers basic information about all reset and interrupt sources in one place for easy reference. A few reset and interrupt sources, including the computer operating properly (COP) watchdog, are not part of on-chip peripheral systems with their own chapters.

5.2 Features

Reset and interrupt features include:

- Multiple sources of reset for flexible system configuration and reliable operation
- Reset status register (SRS) to indicate source of most recent reset
- Separate interrupt vector for each module (reduces polling overhead); see Table 5-1

5.3 MCU Reset

Resetting the MCU provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector (0xFFFE:0xFFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose high-impedance inputs with pull-up devices disabled. The I bit in the condition code register (CCR) is set to block maskable interrupts so the user program has a chance to initialize the stack pointer (SP) and system control settings. (See the CPU chapter for information on the Interrupt (I) bit.) SP is forced to 0x00FF at reset.

The MC9S08DZ128 Series has eight sources for reset:

- Power-on reset (POR)
- External pin reset (PIN)
- Computer operating properly (COP) timer
- Illegal opcode detect (ILOP)
- Illegal address detect (ILAD)
- Low-voltage detect (LVD)
- Loss of clock (LOC)
- Background debug forced reset (BDFR)

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status register (SRS). Whenever the MCU enters reset, the reset pin is driven low for 34



6.5.2 Port B Registers

Port B is controlled by the registers listed below.

6.5.2.1 Port B Data Register (PTBD)



Figure 6-11. Port B Data Register (PTBD)

Table 6-9. PTBD Register Field Descriptions

Field	Description
7:0 PTBD[7:0]	Port B Data Register Bits — For port B pins that are inputs, reads return the logic level on the pin. For port B pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port B pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTBD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups/pull-downs disabled.

6.5.2.2 Port B Data Direction Register (PTBDD)

	7	6	5	4	3	2	1	0
R	דחחדח	DTDDC			07002			
w	PIDUUI	PIBDDo	PIBDDS	PIBDD4	PIBDD3	PIBDD2	ועעשויי	PIBDDU
Reset:	0	0	0	0	0	0	0	0

Figure 6-12. Port B Data Direction Register (PTBDD)

Table 6-10. PTBDD Register Field Descriptions

Field	Description
7:0 PTBDD[7:0]	Data Direction for Port B Bits — These read/write bits control the direction of port B pins and what is read for PTBD reads.
	 Input (output driver disabled) and reads return the pin value. Output driver enabled for port B bit n and PTBD reads return the contents of PTBDn.



Chapter 6 Parallel Input/Output Control

6.5.8.3 Port H Pull Enable Register (PTHPE)



Figure 6-49. Internal Pull Enable for Port H Register (PTHPE)

Table 6-47. PTHPE Register Field Descriptions

Field	Description
7:0	Internal Pull Enable for Port H Bits — Each of these control bits determines if the internal pull-up device is
PTHPE[7:0]	enabled for the associated PTH pin. For port H pins that are configured as outputs, these bits have no effect and
	the internal pull devices are disabled.
	0 Internal pull-up device disabled for port H bit n.
	1 Internal pull-up device enabled for port H bit n.

NOTE

Pull-down devices only apply when using pin interrupt functions, when corresponding edge select and pin select functions are configured.

6.5.8.4 Port H Slew Rate Enable Register (PTHSE)



Figure 6-50. Slew Rate Enable for Port H Register (PTHSE)

Table 6-48. PTHSE Register Field Descriptions

Field	Description
7:0 PTHSE[7:0]	 Output Slew Rate Enable for Port H Bits — Each of these control bits determines if the output slew rate control is enabled for the associated PTH pin. For port H pins that are configured as inputs, these bits have no effect. Output slew rate control disabled for port H bit n. Output slew rate control enabled for port H bit n.

Note: Slew rate reset default values may differ between engineering samples and final production parts. Always initialize slew rate control to the desired value to ensure correct operation.







8.5.4 Calibrating the Internal Reference Clock (IRC)

The IRC is calibrated by writing to the MCGTRM register first, then using the FTRIM bit to "fine tune" the frequency. We will refer to this total 9-bit value as the trim value, ranging from 0x000 to 0x1FF, where the FTRIM bit is the LSB.

The trim value after reset is the factory trim value unless the device resets into any BDM mode in which case it is 0x800. Writing a larger value will decrease the frequency and smaller values will increase the frequency. The trim value is linear with the period, except that slight variations in wafer fab processing produce slight non-linearities between trim value and period. These non-linearities are why an iterative

NP

Chapter 9 5-V Analog Comparator (S08ACMPV3)



Figure 9-1. MC9S08DZ128 Block Diagram with ACMP Highlighted



Chapter 10 Analog-to-Digital Converter (S08ADC12V1)



Figure 10-2. ADC Block Diagram

10.2 External Signal Description

The ADC module supports up to 28 separate analog inputs. It also requires four supply/reference/ground connections.

Name	Function
AD27–AD0	Analog Channel inputs
V _{REFH}	High reference voltage
V _{REFL}	Low reference voltage
V _{DDAD}	Analog power supply
V _{SSAD}	Analog ground

Table 10-2. Signal Properties



Chapter 11 Inter-Integrated Circuit (S08IICV2)



Figure 11-1. MC9S08DZ128 Block Diagram with IIC Highlighted



11.3.3 IIC Control Register (IICxC1)



Figure 11-5. IIC Control Register (IICxC1)

Field	Description
7 IICEN	 IIC Enable. The IICEN bit determines whether the IIC module is enabled. 0 IIC is not enabled 1 IIC is enabled
6 IICIE	 IIC Interrupt Enable. The IICIE bit determines whether an IIC interrupt is requested. 0 IIC interrupt request not enabled 1 IIC interrupt request enabled
5 MST	 Master Mode Select. The MST bit changes from a 0 to a 1 when a start signal is generated on the bus and master mode is selected. When this bit changes from a 1 to a 0 a stop signal is generated and the mode of operation changes from master to slave. 0 Slave mode 1 Master mode
4 TX	Transmit Mode Select. The TX bit selects the direction of master and slave transfers. In master mode, this bit should be set according to the type of transfer required. Therefore, for address cycles, this bit is always high. When addressed as a slave, this bit should be set by software according to the SRW bit in the status register. 0 Receive 1 Transmit
3 ТХАК	 Transmit Acknowledge Enable. This bit specifies the value driven onto the SDA during data acknowledge cycles for master and slave receivers. 0 An acknowledge signal is sent out to the bus after receiving one data byte 1 No acknowledge signal response is sent
2 RSTA	Repeat start. Writing a 1 to this bit generates a repeated start condition provided it is the current master. This bit is always read as cleared. Attempting a repeat at the wrong time results in loss of arbitration.



Chapter 11 Inter-Integrated Circuit (S08IICV2)

the transition from master to slave mode does not generate a stop condition. Meanwhile, a status bit is set by hardware to indicate loss of arbitration.

11.4.1.7 Clock Synchronization

Because wire-AND logic is performed on the SCL line, a high-to-low transition on the SCL line affects all the devices connected on the bus. The devices start counting their low period and after a device's clock has gone low, it holds the SCL line low until the clock high state is reached. However, the change of low to high in this device clock may not change the state of the SCL line if another device clock is still within its low period. Therefore, synchronized clock SCL is held low by the device with the longest low period. Devices with shorter low periods enter a high wait state during this time (see Figure 11-10). When all devices concerned have counted off their low period, the synchronized clock SCL line is released and pulled high. There is then no difference between the device clocks and the state of the SCL line and all the devices start counting their high periods. The first device to complete its high period pulls the SCL line low again.



11.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such a case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

11.4.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it. If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

Chapter 12 Freescale's Controller Area Network (S08MSCANV1)



12.1.1 Features

The basic features of the MSCAN are as follows:

- Implementation of the CAN protocol Version 2.0A/B
 - Standard and extended data frames
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbps^1
 - Support for remote frames
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization using a "local priority" concept
- Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, or four 16-bit filters, or eight 8-bit filters
- Programmable wakeup functionality with integrated low-pass filter
- Programmable loopback mode supports self-test operation
- Programmable listen-only mode for monitoring of CAN bus
- Programmable bus-off recovery functionality
- Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
- Programmable MSCAN clock source either bus clock or oscillator clock
- Internal timer for time-stamping of received and transmitted messages
- Three low-power modes: sleep, power down, and MSCAN enable
- Global initialization of configuration registers

12.1.2 Modes of Operation

The following modes of operation are specific to the MSCAN. See Section 12.5, "Functional Description," for details.

- Listen-Only Mode
- MSCAN Sleep Mode
- MSCAN Initialization Mode
- MSCAN Power Down Mode
- Loopback Self Test Mode

^{1.} Depending on the actual bit timing and the clock jitter of the PLL.



Chapter 12 Freescale's Controller Area Network (S08MSCANV1)

12.1.3 Block Diagram



Figure 12-2. MSCAN Block Diagram

12.2 External Signal Description

The MSCAN uses two external pins:

12.2.1 RXCAN — CAN Receiver Input Pin

RXCAN is the MSCAN receiver input pin.

12.2.2 TXCAN — CAN Transmitter Output Pin

TXCAN is the MSCAN transmitter output pin. The TXCAN output pin represents the logic level on the CAN bus:

0 = Dominant state 1 = Recessive state

12.2.3 CAN System

A typical CAN system with MSCAN is shown in Figure 12-3. Each CAN node is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective nodes.



12.3.14 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.



Figure 12-18. MSCAN Transmit Error Counter (CANTXERR)

Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)

Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

12.3.15 MSCAN Identifier Acceptance Registers (CANIDAR0-7)

On reception, each message is written into the background receive buffer. The CPU is only signalled to read the message if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the MSCAN are applied on the IDR0–IDR3 registers (see Section 12.4.1, "Identifier Registers (IDR0–IDR3)") of incoming messages in a bit by bit manner (see Section 12.5.3, "Identifier Acceptance Filter").

For extended identifiers, all four acceptance and mask registers are applied. For standard identifiers, only the first two (CANIDAR0/1, CANIDMR0/1) are applied.

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 12-19. MSCAN Identifier Acceptance Registers (First Bank) — CANIDAR0–CANIDAR3

Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)



	Data Byte			
DLC3	DLC2	DLC1	DLC0	Count
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

Table 12-33. Data Length Codes

12.4.5 Transmit Buffer Priority Register (TBPR)

This register defines the local priority of the associated message transmit buffer. The local priority is used for the internal prioritization process of the MSCAN and is defined to be highest for the smallest binary number. The MSCAN implements the following internal prioritization mechanisms:

- All transmission buffers with a cleared TXEx flag participate in the prioritization immediately before the SOF (start of frame) is sent.
- The transmission buffer with the lowest local priority field wins the prioritization.

In cases of more than one buffer having the same lowest priority, the message buffer with the lower index number wins.

	7	6	5	4	3	2	1	0
R W	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
Reset:	0	0	0	0	0	0	0	0

Figure 12-35. Transmit Buffer Priority Register (TBPR)

Read: Anytime when TXEx flag is set (see Section 12.3.6, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.10, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

Write: Anytime when TXEx flag is set (see Section 12.3.6, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.10, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

12.4.6 Time Stamp Register (TSRH–TSRL)

If the TIME bit is enabled, the MSCAN will write a time stamp to the respective registers in the active transmit or receive buffer as soon as a message has been acknowledged on the CAN bus (see



Chapter 12 Freescale's Controller Area Network (S08MSCANV1)



Field	Description
4 MSTR	Master/Slave Mode Select 0 SPI module configured as a slave SPI device 1 SPI module configured as a master SPI device
3 CPOL	 Clock Polarity — This bit effectively places an inverter in series with the clock signal from a master SPI or to a slave SPI device. Refer to Section 13.5.1, "SPI Clock Formats" for more details. 0 Active-high SPI clock (idles low) 1 Active-low SPI clock (idles high)
2 CPHA	 Clock Phase — This bit selects one of two clock formats for different kinds of synchronous serial peripheral devices. Refer to Section 13.5.1, "SPI Clock Formats" for more details. 0 First edge on SPSCK occurs at the middle of the first cycle of an 8-cycle data transfer 1 First edge on SPSCK occurs at the start of the first cycle of an 8-cycle data transfer
1 SSOE	Slave Select Output Enable — This bit is used in combination with the mode fault enable (MODFEN) bit in SPCR2 and the master/slave (MSTR) control bit to determine the function of the SS pin as shown in Table 13-2.
0 LSBFE	 LSB First (Shifter Direction) 0 SPI serial data transfers start with most significant bit 1 SPI serial data transfers start with least significant bit

Table 13-2. SS Pin Function

MODFEN	SSOE	Master Mode	Slave Mode
0	0	General-purpose I/O (not SPI)	Slave select input
0	1	General-purpose I/O (not SPI) Slave select input	
1	0	SS input for mode fault	Slave select input
1	1	Automatic SS output	Slave select input

NOTE

Ensure that the SPI should not be disabled (SPE=0) at the same time as a bit change to the CPHA bit. These changes should be performed as separate operations or unexpected behavior may occur.

13.4.2 SPI Control Register 2 (SPIxC2)

This read/write register is used to control optional features of the SPI system. Bits 7, 6, 5, and 2 are not implemented and always read 0.







Chapter 18 Debug Module (S08DBGV3) (128K)

18.4.4.3.7 A And Not B (Full Mode)

In the A And Not B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A And Not B trigger mode, if the match condition for A and Not B happen on the same bus cycle, both the AF and BF flags in the DBGS register are set. If a match condition on only A or only Not B occur no flags are set.

For Breakpoint tagging operation with an end-trigger type trace, only matches from Comparator A will be used to determine if the Breakpoint conditions are met and Comparator B matches will be ignored.

18.4.4.3.8 Inside Range, $A \leq address \leq B$

In the Inside Range trigger mode, if the match condition for A and B happen on the same bus cycle, both the AF and BF flags in the DBGS register are set. If a match condition on only A or only B occur no flags are set.

18.4.4.3.9 Outside Range, address < A or address > B

In the Outside Range trigger mode, if the match condition for A or B is met, the corresponding flag in the DBGS register is set.

The four control bits BEGIN and TRGSEL in DBGT, and BRKEN and TAG in DBGC, determine the basic type of debug run as shown in Table 1.21. Some of the 16 possible combinations are not used (refer to the notes at the end of the table).

BEGIN	TRGSEL	BRKEN	TAG	Type of Debug Run
0	0	0	x ⁽¹⁾	Fill FIFO until trigger address (No CPU breakpoint - keep running)
0	0	1	0	Fill FIFO until trigger address, then force CPU breakpoint
0	0	1	1	Do not use ⁽²⁾
0	1	0	x ⁽¹⁾	Fill FIFO until trigger opcode about to execute (No CPU breakpoint - keep running)
0	1	1	0	Do not use ⁽³⁾
0	1	1	1	Fill FIFO until trigger opcode about to execute (trigger causes CPU breakpoint)
1	0	0	x ⁽¹⁾	Start FIFO at trigger address (No CPU breakpoint - keep running)
1	0	1	0	Start FIFO at trigger address, force CPU breakpoint when FIFO full
1	0	1	1	Do not use ⁽⁴⁾
1	1	0	x ⁽¹⁾	Start FIFO at trigger opcode (No CPU breakpoint - keep running)
1	1	1	0	Start FIFO at trigger opcode, force CPU breakpoint when FIFO full
1	1	1	1	Do not use ⁽⁴⁾

Table 18-21. Basic Types of Debug Runs

Num	С	Parameter	Symbol	V _{DD} (V)	Typ ¹	Max ²	Unit
8	Р	Adder to stop3 for oscillator enabled ⁷	ସ୍ଥ	5	5	8	ıιΔ
	Р	(EREFSTEN =1)	DDOSC	3	5	8	μΑ

	Table A-7.	Supply Current	Characteristics	(continued)
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¹ Typical are measured at 25°C. See Figure A-8 through Figure A-10 for typical curves across voltage/temperature.

- ² Max values in this column apply for the full operating temperature range of the device unless otherwise noted.
- ³ All modules except ADC active, ICS configured for FBE, and does not include any dc loads on port pins
- ⁴ All modules except ADC active, ICS configured for FEI, and does not include any dc loads on port pins
- ⁵ Stop currents are tested in production for 25°C on all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and approved.
- ⁶ Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.
- ⁷ Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal and low power mode (HGO = 0).



Figure A-5. Typical Run I_{DD} vs. Bus Frequency ($V_{DD} = 5V$)