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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	87
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08dz128mll

debug interface) and verifying that FLASH is blank. To avoid returning to secure mode after the next reset, program the security bits (SEC) to the unsecured state (1:0).

4.4 Memory Management Unit

The memory management unit (MMU) allows the program and data space for the HCS08 Family of Microcontrollers to be extended beyond the 64K CPU addressable memory map. The extended memory when used for data can also be accessed linearly using a linear address pointer and data access registers.

4.4.1 Features

Key features of the MMU module are:

- Memory Management Unit extends the HCS08 memory space
 - up to 128K for program and data space
- Extended program space using paging scheme
 - PPAGE register used for page selection
 - fixed 16K byte memory window
 - architecture supports eight 16K pages
- Extended data space using linear address pointer
 - 17-bit linear address pointer
 - linear address pointer and data register provided in direct page allows access of complete FLASH memory map using direct page instructions
 - optional auto increment of pointer when data accessed
 - supports a 2s complement addition/subtraction to address pointer without using any math instructions or memory resources
 - supports word accesses to any address specified by the linear address pointer when using LDHX, STHX instructions

4.4.2 Memory Expansion

The HCS08 Core architecture limits the CPU addressable space available to 64K bytes. The Program Page (PPAGE) allows for integrating up to 128K of FLASH into the system by selecting one of the 16K byte blocks to be accessed through the Paging Window located at 0x8000-0xBFFF. The MMU module also provides a linear address pointer that allows extension of data access up to 128K.

4.4.2.1 Program Space

The PPAGE register holds the page select value for the Paging Window. The value in PPAGE can be manipulated by using normal read and write instructions as well as the CALL and RTC instructions. The user should not change PPAGE directly when running from paged memory, only CALL and RTC should be used.

6.5.6.5 Port F Drive Strength Selection Register (PTFDS)

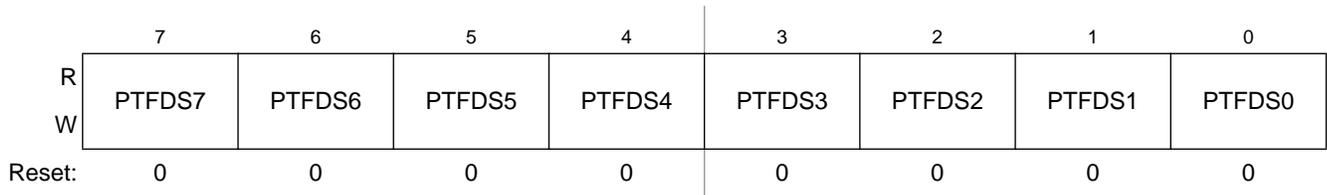


Figure 6-41. Drive Strength Selection for Port F Register (PTFDS)

Table 6-39. PTFDS Register Field Descriptions

Field	Description
7:0 PTFDS[7:0]	<p>Output Drive Strength Selection for Port F Bits — Each of these control bits selects between low and high output drive for the associated PTF pin. For port F pins that are configured as inputs, these bits have no effect.</p> <p>0 Low output drive strength selected for port F bit n.</p> <p>1 High output drive strength selected for port F bit n.</p>

6.5.9 Port J Registers

Port J is controlled by the registers listed below.

6.5.9.1 Port J Data Register (PTJD)

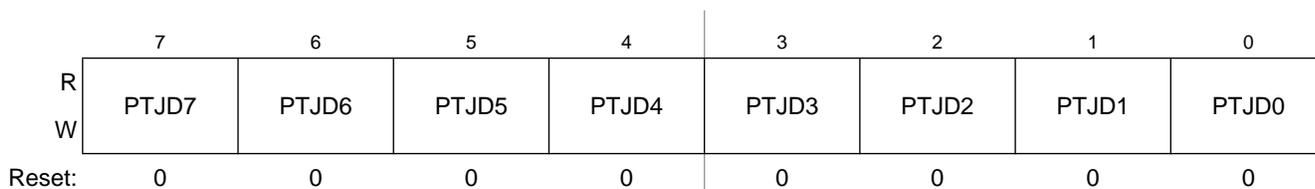


Figure 6-52. Port J Data Register (PTJD)

Table 6-50. PTJD Register Field Descriptions

Field	Description
7:0 PTJD[7:0]	Port J Data Register Bits — For port J pins that are inputs, reads return the logic level on the pin. For port J pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port J pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTJD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups disabled.

6.5.9.2 Port J Data Direction Register (PTJDD)

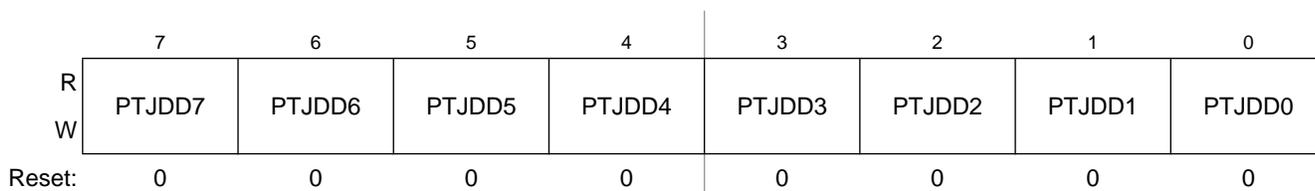


Figure 6-53. Port J Data Direction Register (PTJDD)

Table 6-51. PTJDD Register Field Descriptions

Field	Description
7:0 PTJDD[7:0]	Data Direction for Port J Bits — These read/write bits control the direction of port J pins and what is read for PTJD reads. 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port J bit n and PTJD reads return the contents of PTJDn.

7.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08, memory, status and control registers, and input/output (I/O) ports share a single 64-Kbyte CPU address space. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

NOTE

For more information about extended addressing modes, see the Memory Management Unit section in the Memory chapter.

MCU derivatives with more than 64-Kbytes of memory also include a memory management unit (MMU) to support extended memory space. A PPAGE register is used to manage 16-Kbyte pages of memory which can be accessed by the CPU through a 16-Kbyte window from 0x8000 through 0xBFFF. The CPU includes two special instructions (CALL and RTC). CALL operates like the JSR instruction except that CALL saves the current PPAGE value on the stack and provides a new PPAGE value for the destination. RTC works like the RTS instruction except RTC restores the old PPAGE value in addition to the PC during the return from the called routine. The MMU also includes a linear address pointer register and data access registers so that the extended memory space operates as if it was a single linear block of memory. For additional information about the MMU, refer to the Memory chapter of this data sheet.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

7.3.1 Inherent Addressing Mode (INH)

In this addressing mode, operands needed to complete the instruction (if any) are located within CPU registers so the CPU does not need to access memory to get any operands.

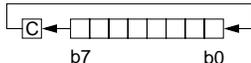
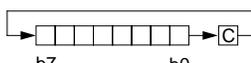
7.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed 8-bit offset value is located in the memory location immediately following the opcode. During execution, if the branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address.

7.3.3 Immediate Addressing Mode (IMM)

In immediate addressing mode, the operand needed to complete the instruction is included in the object code immediately following the instruction opcode in memory. In the case of a 16-bit immediate operand,

Table 7-2. Instruction Set Summary (Sheet 6 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR	
						V I 1 H	I N Z C
MOV <i>opr8a,opr8a</i> MOV <i>opr8a,X+</i> MOV <i>#opr8i,opr8a</i> MOV <i>,X+,opr8a</i>	Move $(M)_{\text{destination}} \leftarrow (M)_{\text{source}}$ In IX+/DIR and DIR/IX+ Modes, $H:X \leftarrow (H:X) + \$0001$	DIR/DIR DIR/IX+ IMM/DIR IX+/DIR	4E dd dd 5E dd 6E ii dd 7E dd	5 5 4 5	rfwpp rfwpp pwpp rfwpp	0 1 1 -	- \uparrow \downarrow \uparrow -
MUL	Unsigned multiply $X:A \leftarrow (X) \times (A)$	INH	42	5	ffffp	- 1 1 0	- - - - 0
NEG <i>opr8a</i> NEGA NEGX NEG <i>opr8,X</i> NEG <i>,X</i> NEG <i>opr8,SP</i>	Negate Two's Complement $M \leftarrow -(M) = \$00 - (M)$ $A \leftarrow -(A) = \$00 - (A)$ $X \leftarrow -(X) = \$00 - (X)$ $M \leftarrow -(M) = \$00 - (M)$ $M \leftarrow -(M) = \$00 - (M)$ $M \leftarrow -(M) = \$00 - (M)$	DIR INH INH IX1 IX SP1	30 dd 40 50 60 ff 70 9E 60 ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	\uparrow 1 1 -	- \uparrow \downarrow \uparrow \downarrow
NOP	No Operation — Uses 1 Bus Cycle	INH	9D	1	p	- 1 1 -	- - - - -
NSA	Nibble Swap Accumulator $A \leftarrow (A[3:0]:A[7:4])$	INH	62	1	p	- 1 1 -	- - - - -
ORA <i>#opr8i</i> ORA <i>opr8a</i> ORA <i>opr16a</i> ORA <i>opr16,X</i> ORA <i>opr8,X</i> ORA <i>,X</i> ORA <i>opr16,SP</i> ORA <i>opr8,SP</i>	Inclusive OR Accumulator and Memory $A \leftarrow (A) (M)$	IMM DIR EXT IX2 IX1 IX SP2 SP1	AA ii BA dd CA hh ll DA ee ff EA ff FA 9E DA ee ff 9E EA ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	0 1 1 -	- \uparrow \downarrow \uparrow -
PSHA	Push Accumulator onto Stack Push (A); $SP \leftarrow (SP) - \$0001$	INH	87	2	sp	- 1 1 -	- - - - -
PSHH	Push H (Index Register High) onto Stack Push (H); $SP \leftarrow (SP) - \$0001$	INH	8B	2	sp	- 1 1 -	- - - - -
PSHX	Push X (Index Register Low) onto Stack Push (X); $SP \leftarrow (SP) - \$0001$	INH	89	2	sp	- 1 1 -	- - - - -
PULA	Pull Accumulator from Stack $SP \leftarrow (SP + \$0001)$; Pull (A)	INH	86	3	ufp	- 1 1 -	- - - - -
PULH	Pull H (Index Register High) from Stack $SP \leftarrow (SP + \$0001)$; Pull (H)	INH	8A	3	ufp	- 1 1 -	- - - - -
PULX	Pull X (Index Register Low) from Stack $SP \leftarrow (SP + \$0001)$; Pull (X)	INH	88	3	ufp	- 1 1 -	- - - - -
ROL <i>opr8a</i> ROLA ROLX ROL <i>opr8,X</i> ROL <i>,X</i> ROL <i>opr8,SP</i>	Rotate Left through Carry 	DIR INH INH IX1 IX SP1	39 dd 49 59 69 ff 79 9E 69 ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	\uparrow 1 1 -	- \uparrow \downarrow \uparrow \downarrow
ROR <i>opr8a</i> RORA RORX ROR <i>opr8,X</i> ROR <i>,X</i> ROR <i>opr8,SP</i>	Rotate Right through Carry 	DIR INH INH IX1 IX SP1	36 dd 46 56 66 ff 76 9E 66 ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	\uparrow 1 1 -	- \uparrow \downarrow \uparrow \downarrow

8.3.6 MCG Test and Control Register (MCGT)

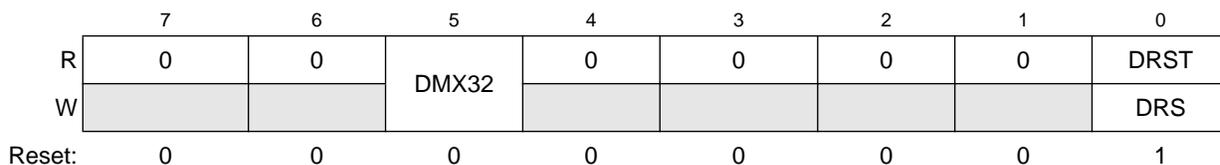


Figure 8-8. MCG Test and Control Register (MCGT)

Table 8-8. MCG Test and Control Register Field Descriptions

Field	Description
7:6	Reserved for test, user code should not write 1's to these bits.
5 DMX32	DCO Maximum frequency with 32.768 kHz reference — The DMX32 bit controls whether or not the DCO frequency range is narrowed to its maximum frequency with a 32.768 kHz reference. See Table 8-9. 0 DCO has default range of 25%. 1 DCO is fined tuned for maximum frequency with 32.768 kHz reference.
4:1	Reserved for test, user code should not write 1's to these bits.
0 DRST DRS	DCO Range Status — The DRST read bit indicates the current frequency range for the FLL output, DCOOUT. See Table 8-9. The DRST bit does not update immediately after a write to the DRS field due to internal synchronization between clock domains. The DRST bit is not valid in BLPI, BLPE, PBE or PEE mode and it reads zero regardless of the DCO range selected by the DRS bit. DCO Range Select — The DRS bit selects the frequency range for the FLL output, DCOOUT. Writes to the DRS bit while either the LP or PLLS bit is set are ignored. 0 Low range. 1 Mid range.

Table 8-9. DCO frequency range¹

DRS	DMX32	Reference range	FLL factor	DCO range
0	0	31.25 - 39.0625 kHz	512	16 - 20 MHz
	1	32.768 kHz	608	19.92 MHz
1	0	31.25 - 39.0625 kHz	1024	32 - 40 MHz
	1	32.768 kHz	1216	39.85 MHz

¹ The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

- If ERCLKEN was set in step 1 or the MCG is in FEE, FBE, PEE, PBE, or BLPE mode, and EREFS was also set in step 1, wait here for the OSCINIT bit to become set indicating that the external clock source has finished its initialization cycles and stabilized. Typical crystal startup times are given in Appendix A, “Electrical Characteristics”.
 - If in FEE mode, check to make sure the IREFST bit is cleared and the LOCK bit is set before moving on.
 - If in FBE mode, check to make sure the IREFST bit is cleared, the LOCK bit is set, and the CLKST bits have changed to %10 indicating the external reference clock has been appropriately selected. Although the FLL is bypassed in FBE mode, it is still on and will lock in FBE mode.
5. Write to the MCGT register to determine the DCO output (MCGOUT) frequency range.
 - By default, with DMX32 (bit 5) cleared to 0, the FLL multiplier for the DCO output is 1024. For greater flexibility, if a mid-range FLL multiplier of 512 is desired instead, clear the DRS bit (bit 0) to 0 for a DCO output frequency of 16.78 MHz.
 - When using a 32.768 kHz external reference, if the maximum mid-range DCO frequency that can be achieved with a 32.768 kHz reference is desired, clear the DRS bit (bit 0) to 0 and set the DMX32 bit (bit 5) to 1. The resulting DCO output (MCGOUT) frequency with the new multiplier of 608 will be 19.92 MHz.
 - When using a 32.768 kHz external reference, if the maximum high-range DCO frequency that can be achieved with a 32.768 kHz reference is desired, set the DRS bit (bit 0) to 1 and set the DMX32 bit (bit 5) to 1. The resulting DCO output (MCGOUT) frequency with the new multiplier of 1216 will be 39.85 MHz.
 6. Wait for the LOCK bit in MCGSC to become set, indicating that the FLL has locked to the new multiplier value designated by the DRS and DMX32 bits.

NOTE

Setting DIV32 (bit 4) in MCGC3 is strongly recommended for FLL external modes when using a high frequency range (RANGE = 1) external reference clock. The DIV32 bit is ignored in all other modes.

To change from FEI clock mode to FBI clock mode, follow this procedure:

1. Change the CLKS bits in MCGC1 to %01 so that the internal reference clock is selected as the system clock source.
2. Wait for the CLKST bits in the MCGSC register to change to %01, indicating that the internal reference clock has been appropriately selected.

8.5.2 Using a 32.768 kHz Reference

In FEE and FBE modes, if using a 32.768 kHz external reference, at the default FLL multiplication factor of 1024, the DCO output (MCGOUT) frequency is 33.55 MHz at high-range. If DRS is cleared to 0, the multiplication factor is halved to 512, and the resulting DCO output frequency is 16.78 Mhz at mid-range.

Setting the DMX32 bit in MCGT to 1 increases the FLL multiplication factor to allow the 32.768 kHz reference to achieve its maximum DCO output frequency. When the DRS bit is set, the 32.768 kHz

reference can achieve a high-range maximum DCO output of 39.85 MHz with a multiplier of 1216. When the DRS bit is clear, the 32.768 kHz reference can achieve a mid-range maximum DCO output of 19.92 MHz with a multiplier of 608.

In FBI and FEI modes, setting the DMX32 bit is not recommended. If the internal reference is trimmed to a frequency above 32.768 kHz, the greater FLL multiplication factor could potentially push the microcontroller system clock out of specification and damage the part.

8.5.3 MCG Mode Switching

When switching between operational modes of the MCG, certain configuration bits must be changed in order to properly move from one mode to another. Each time any of these bits are changed (PLLS, IREFS, CLKS, or EREFS), the corresponding bits in the MCGSC register (PLLST, IREFST, CLKST, or OSCINIT) must be checked before moving on in the application software.

Additionally, care must be taken to ensure that the reference clock divider (RDIV) is set properly for the mode being switched to. For instance, in PEE mode, if using a 4 MHz crystal, RDIV must be set to %001 (divide-by-2) or %010 (divide -by-4) in order to divide the external reference down to the required frequency between 1 and 2 MHz.

If switching to FBE or FEE mode, first setting the DIV32 bit will ensure a proper reference frequency is sent to the FLL clock at all times.

In FBE, FEE, FBI, and FEI modes, at any time, the application can switch the FLL multiplication factor between 1024 and 512 with the DRS bit in MCGT. Writes to DRS will be ignored if LP=1 or PLLS=1.

The RDIV and IREFS bits should always be set properly before changing the PLLS bit so that the FLL or PLL clock has an appropriate reference clock frequency to switch to. The table below shows MCGOUT frequency calculations using RDIV, BDIV, and VDIV settings for each clock mode. The bus frequency is equal to MCGOUT divided by 2.

Table 8-10. MCGOUT Frequency Calculation Options

Clock Mode	f_{MCGOUT}^1	Note
FEI (FLL engaged internal)	$(f_{int} * F) / B$	Typical $f_{MCGOUT} = 16$ MHz immediately after reset.
FEE (FLL engaged external)	$(f_{ext} / R * F) / B$	f_{ext} / R must be in the range of 31.25 kHz to 39.0625 kHz
FBE (FLL bypassed external)	f_{ext} / B	f_{ext} / R must be in the range of 31.25 kHz to 39.0625 kHz
FBI (FLL bypassed internal)	f_{int} / B	Typical $f_{int} = 32$ kHz
PEE (PLL engaged external)	$[(f_{ext} / R) * M] / B$	f_{ext} / R must be in the range of 1 MHz to 2 MHz
PBE (PLL bypassed external)	f_{ext} / B	f_{ext} / R must be in the range of 1 MHz to 2 MHz
BLPI (Bypassed low power internal)	f_{int} / B	
BLPE (Bypassed low power external)	f_{ext} / B	

- IREFS (bit 2) set to 1 to select the internal reference clock as the reference clock source
 - RDIV (bits 5-3) remain unchanged because the reference divider does not affect the internal reference.
 - b) Loop until IREFST (bit 4) in MCGSC is 1, indicating the internal reference clock has been selected as the reference clock source
 - c) Loop until CLKST (bits 3 and 2) in MCGSC are %01, indicating that the internal reference clock is selected to feed MCGOUT
4. Lastly, FBI transitions into BLPI mode.
- a) MCGC2 = 0x08 (%00001000)
 - LP (bit 3) in MCGSC is 1
 - RANGE, HGO, EREFS, ERCLKEN, and EREFSTEN bits are ignored when the IREFS bit (bit2) in MCGC is set. They can remain set, or be cleared at this point.

Chapter 10

Analog-to-Digital Converter (S08ADC12V1)

10.1 Introduction

The 12-bit analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.

NOTE

MC9S08DZ128 Series devices operate at a higher voltage range (2.7 V to 5.5 V) and do not include stop1 mode. Please ignore references to stop1.

The ADC channel assignments, alternate clock function, and hardware trigger function are configured as described in [Section 10.1.1, “Channel Assignments.”](#)

10.1.1 Channel Assignments

NOTE

The ADC channel assignments for the MC9S08DZ128 Series devices are shown in [Table 10-1](#). Reserved channels convert to an unknown value.

This chapter shows bits for all S08ADC12V1 channels. MC9S08DZ128 Series MCUs do not use all of these channels. All bits corresponding to channels that are not available on a device are reserved.

10.1.2 Analog Power and Ground Signal Names

References to V_{DDAD} and V_{SSAD} in this chapter correspond to signals V_{DDA} and V_{SSA} , respectively.

used to control the pins associated with channels 0–7 of the ADC module.

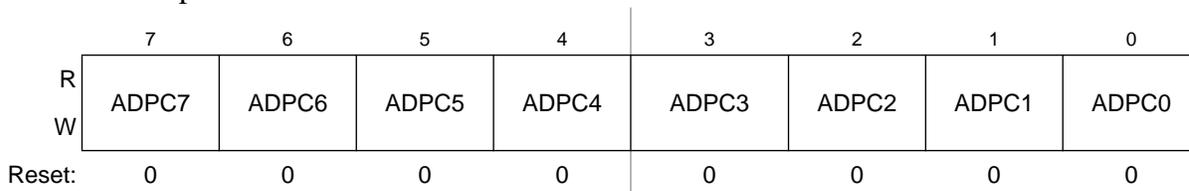


Figure 10-10. Pin Control 1 Register (APCTL1)

Table 10-10. APCTL1 Register Field Descriptions

Field	Description
7 ADPC7	ADC Pin Control 7. ADPC7 controls the pin associated with channel AD7. 0 AD7 pin I/O control enabled 1 AD7 pin I/O control disabled
6 ADPC6	ADC Pin Control 6. ADPC6 controls the pin associated with channel AD6. 0 AD6 pin I/O control enabled 1 AD6 pin I/O control disabled
5 ADPC5	ADC Pin Control 5. ADPC5 controls the pin associated with channel AD5. 0 AD5 pin I/O control enabled 1 AD5 pin I/O control disabled
4 ADPC4	ADC Pin Control 4. ADPC4 controls the pin associated with channel AD4. 0 AD4 pin I/O control enabled 1 AD4 pin I/O control disabled
3 ADPC3	ADC Pin Control 3. ADPC3 controls the pin associated with channel AD3. 0 AD3 pin I/O control enabled 1 AD3 pin I/O control disabled
2 ADPC2	ADC Pin Control 2. ADPC2 controls the pin associated with channel AD2. 0 AD2 pin I/O control enabled 1 AD2 pin I/O control disabled
1 ADPC1	ADC Pin Control 1. ADPC1 controls the pin associated with channel AD1. 0 AD1 pin I/O control enabled 1 AD1 pin I/O control disabled
0 ADPC0	ADC Pin Control 0. ADPC0 controls the pin associated with channel AD0. 0 AD0 pin I/O control enabled 1 AD0 pin I/O control disabled

10.3.9 Pin Control 2 Register (APCTL2)

APCTL2 controls channels 8–15 of the ADC module.

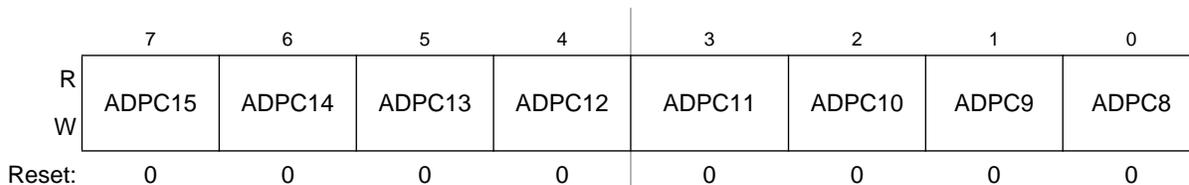


Figure 10-11. Pin Control 2 Register (APCTL2)

11.4.2 10-bit Address

For 10-bit addressing, 0x11110 is used for the first 5 bits of the first address byte. Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing.

11.4.2.1 Master-Transmitter Addresses a Slave-Receiver

The transfer direction is not changed (see Table 11-10). When a 10-bit address follows a start condition, each slave compares the first seven bits of the first byte of the slave address (11110XX) with its own address and tests whether the eighth bit (R/\overline{W} direction bit) is 0. More than one device can find a match and generate an acknowledge (A1). Then, each slave that finds a match compares the eight bits of the second byte of the slave address with its own address. Only one slave finds a match and generates an acknowledge (A2). The matching slave remains addressed by the master until it receives a stop condition (P) or a repeated start condition (Sr) followed by a different slave address.

S	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 0	A1	Slave Address 2nd byte AD[8:1]	A2	Data	A	...	Data	A/A	P
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Table 11-10. Master-Transmitter Addresses Slave-Receiver with a 10-bit Address

After the master-transmitter has sent the first byte of the 10-bit address, the slave-receiver sees an IIC interrupt. Software must ensure the contents of IICD are ignored and not treated as valid data for this interrupt.

11.4.2.2 Master-Receiver Addresses a Slave-Transmitter

The transfer direction is changed after the second R/\overline{W} bit (see Table 11-11). Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a slave-receiver. After the repeated start condition (Sr), a matching slave remembers that it was addressed before. This slave then checks whether the first seven bits of the first byte of the slave address following Sr are the same as they were after the start condition (S) and tests whether the eighth (R/\overline{W}) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a stop condition (P) or a repeated start condition (Sr) followed by a different slave address.

After a repeated start condition (Sr), all other slave devices also compare the first seven bits of the first byte of the slave address with their own addresses and test the eighth (R/\overline{W}) bit. However, none of them are addressed because $R/\overline{W} = 1$ (for 10-bit devices) or the 11110XX slave address (for 7-bit devices) does not match.

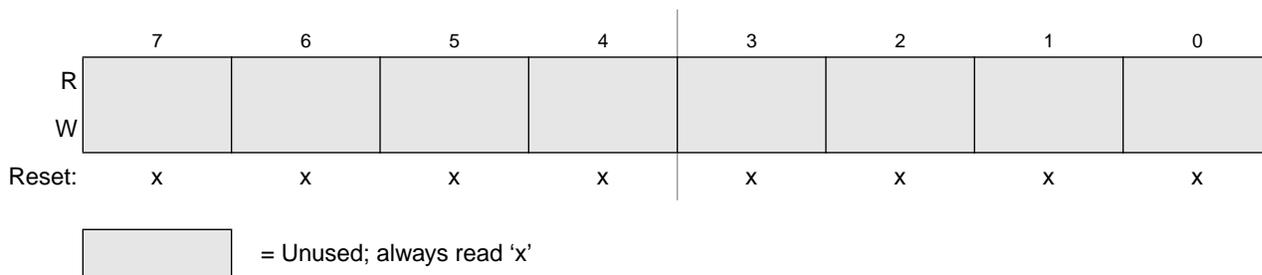
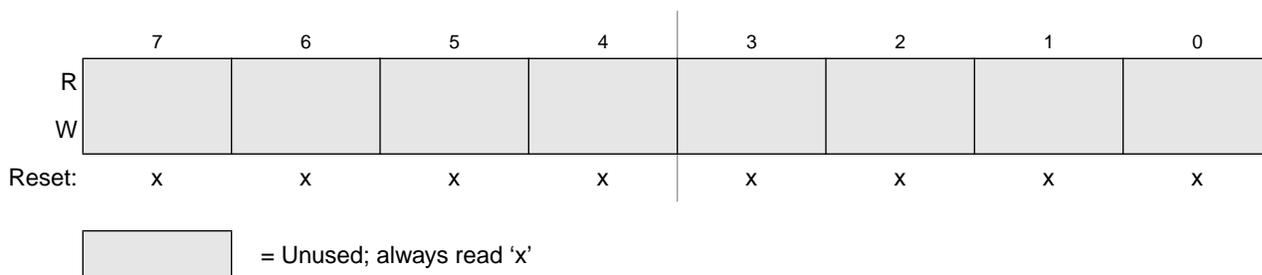
S	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 0	A1	Slave Address 2nd byte AD[8:1]	A2	Sr	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 1	A3	Data	A	...	Data	A	P
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Table 11-11. Master-Receiver Addresses a Slave-Transmitter with a 10-bit Address

After the master-receiver has sent the first byte of the 10-bit address, the slave-transmitter sees an IIC interrupt. Software must ensure the contents of IICD are ignored and not treated as valid data for this interrupt.

Table 12-30. IDR1 Register Field Descriptions

Field	Description
7:5 ID[2:0]	Standard Format Identifier — The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 12-29 .
4 RTR	Remote Transmission Request — This flag reflects the status of the Remote Transmission Request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent. 0 Data frame 1 Remote frame
3 IDE	ID Extended — This flag indicates whether the extended or standard identifier format is applied in this buffer. In the case of a receive buffer, the flag is set as received and indicates to the CPU how to process the buffer identifier registers. In the case of a transmit buffer, the flag indicates to the MSCAN what type of identifier to send. 0 Standard format (11 bit) 1 Extended format (29 bit)


Figure 12-31. Identifier Register 2 — Standard Mapping

Figure 12-32. Identifier Register 3 — Standard Mapping

12.4.3 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

14.1.4 Block Diagram

Figure 14-2 shows the transmitter portion of the SCI.

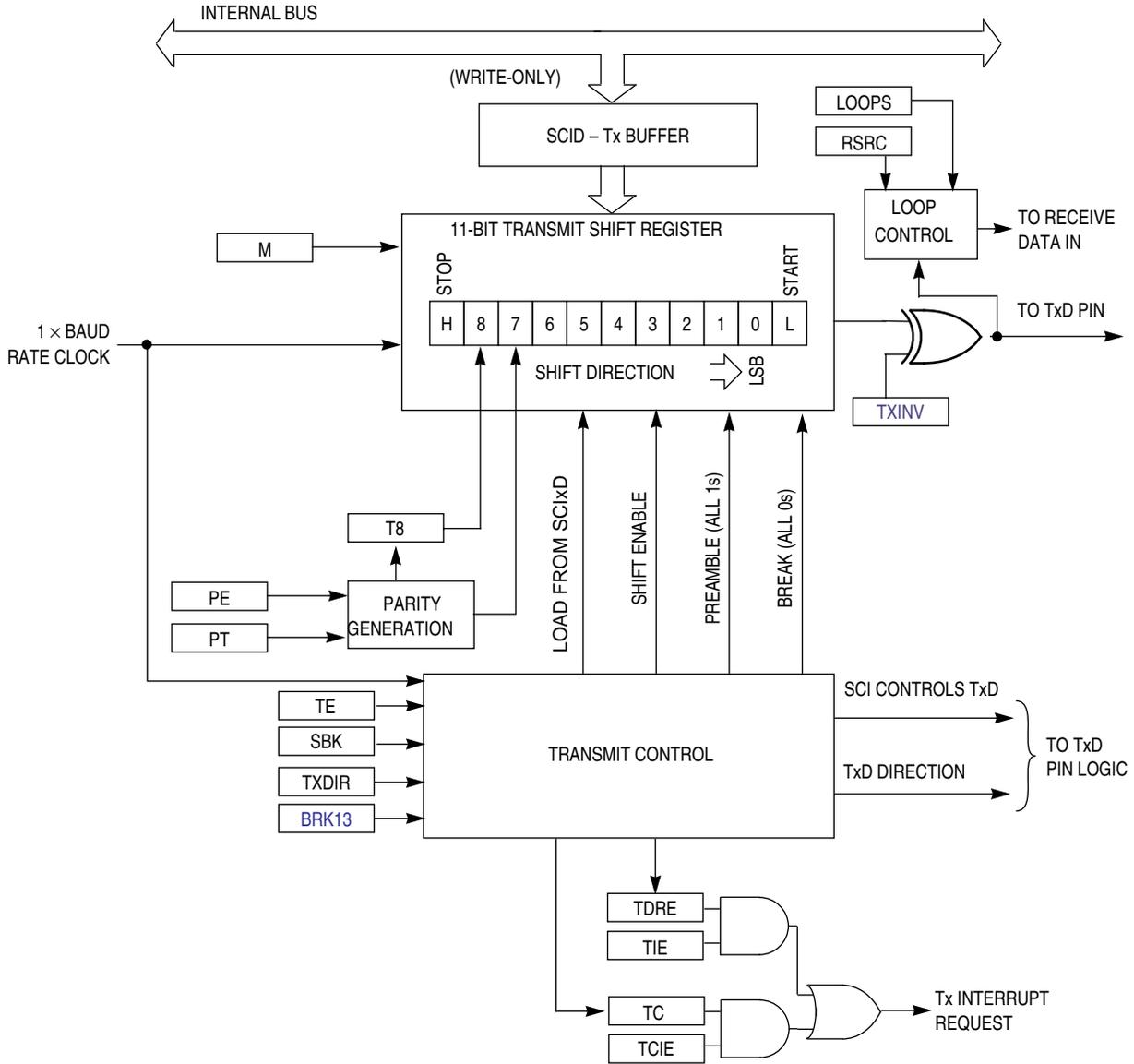


Figure 14-2. SCI Transmitter Block Diagram

Table 14-8. SCIxC3 Field Descriptions (continued)

Field	Description
4 TXINV ¹	Transmit Data Inversion — Setting this bit reverses the polarity of the transmitted data output. 0 Transmit data not inverted 1 Transmit data inverted
3 ORIE	Overrun Interrupt Enable — This bit enables the overrun flag (OR) to generate hardware interrupt requests. 0 OR interrupts disabled (use polling). 1 Hardware interrupt requested when OR = 1.
2 NEIE	Noise Error Interrupt Enable — This bit enables the noise flag (NF) to generate hardware interrupt requests. 0 NF interrupts disabled (use polling). 1 Hardware interrupt requested when NF = 1.
1 FEIE	Framing Error Interrupt Enable — This bit enables the framing error flag (FE) to generate hardware interrupt requests. 0 FE interrupts disabled (use polling). 1 Hardware interrupt requested when FE = 1.
0 PEIE	Parity Error Interrupt Enable — This bit enables the parity error flag (PF) to generate hardware interrupt requests. 0 PF interrupts disabled (use polling). 1 Hardware interrupt requested when PF = 1.

¹ Setting TXINV inverts the TxD output for all cases: data bits, start and stop bits, break, and idle.

14.2.7 SCI Data Register (SCIXD)

This register is actually two separate registers. Reads return the contents of the read-only receive data buffer and writes go to the write-only transmit data buffer. Reads and writes of this register are also involved in the automatic flag clearing mechanisms for the SCI status flags.

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 14-11. SCI Data Register (SCIXD)

14.3 Functional Description

The SCI allows full-duplex, asynchronous, NRZ serial communication among the MCU and remote devices, including other MCUs. The SCI comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. During normal operation, the MCU monitors the status of the SCI, writes the data to be transmitted, and processes received data. The following describes each of the blocks of the SCI.

14.3.1 Baud Rate Generation

As shown in [Figure 14-12](#), the clock source for the SCI baud rate generator is the bus-rate clock.

17.1.2 Features

Features of the BDC module include:

- Single pin for mode selection and background communications
- BDC registers are not located in the memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC
- Oscillator runs in stop mode, if BDC enabled
- COP watchdog disabled while in active background mode

17.2 Background Debug Controller (BDC)

All MCUs in the HCS08 Family contain a single-wire background debug interface that supports in-circuit programming of on-chip nonvolatile memory and sophisticated non-intrusive debug capabilities. Unlike debug interfaces on earlier 8-bit MCUs, this system does not interfere with normal application resources. It does not use any user memory or locations in the memory map and does not share any on-chip peripherals.

BDC commands are divided into two groups:

- Active background mode commands require that the target MCU is in active background mode (the user program is not running). Active background mode commands allow the CPU registers to be read or written, and allow the user to trace one user instruction at a time, or GO to the user program from active background mode.
- Non-intrusive commands can be executed at any time even while the user's program is running. Non-intrusive commands allow a user to read or write MCU memory locations or access status and control registers within the background debug controller.

Typically, a relatively simple interface pod is used to translate commands from a host computer into commands for the custom serial interface to the single-wire background debug system. Depending on the development tool vendor, this interface pod may use a standard RS-232 serial port, a parallel printer port, or some other type of communications such as a universal serial bus (USB) to communicate between the host PC and the pod. The pod typically connects to the target system with ground, the BKGD pin, $\overline{\text{RESET}}$, and sometimes V_{DD} . An open-drain connection to reset allows the host to force a target system reset, which is useful to regain control of a lost target system or to control startup of a target system before the on-chip nonvolatile memory has been programmed. Sometimes V_{DD} can be used to allow the pod to use power from the target system to avoid the need for a separate power supply. However, if the pod is powered separately, it can be connected to a running target system without forcing a target system reset or otherwise disturbing the running application program.

Table A-6. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ ¹	Max	Unit	
14	D	RAM retention voltage	V_{RAM}		—	0.6	1.0	V	
15	D	POR re-arm voltage ⁸	V_{POR}		0.9	1.4	2.0	V	
16	D	POR re-arm time ⁹	t_{POR}		10	—	—	μ s	
17	P	Low-voltage detection threshold — high range	V_{LVD1}		V_{DD} falling	3.9	4.0	4.1	V
					V_{DD} rising	4.0	4.1	4.2	
18	P	Low-voltage detection threshold — low range	V_{LVD0}		V_{DD} falling	2.48	2.56	2.64	V
					V_{DD} rising	2.54	2.62	2.70	
19	P	Low-voltage warning threshold — high range 1	V_{LVW3}		V_{DD} falling	4.5	4.6	4.7	V
					V_{DD} rising	4.6	4.7	4.8	
20	P	Low-voltage warning threshold — high range 0	V_{LVW2}		V_{DD} falling	4.2	4.3	4.4	V
					V_{DD} rising	4.3	4.4	4.5	
21	P	Low-voltage warning threshold low range 1	V_{LVW1}		V_{DD} falling	2.84	2.92	3.00	V
					V_{DD} rising	2.90	2.98	3.06	
22	P	Low-voltage warning threshold — low range 0	V_{LVW0}		V_{DD} falling	2.66	2.74	2.82	V
					V_{DD} rising	2.72	2.80	2.88	
23	T	Low-voltage inhibit reset/recover hysteresis	V_{Ivihys}	5 V	—	100	—	mV	
				3 V	—	60	—		
24	P	Bandgap Voltage Reference ¹⁰	V_{BG}		1.19	1.20	1.21	V	

¹ Typical values are measured at 25°C. Characterized, not tested.

² When a pin interrupt is configured to detect rising edges, pulldown resistors are used in place of pullup resistors.

³ The specified resistor value is the actual value internal to the device. The pullup value may measure higher when measured externally on the pin.

⁴ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁵ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

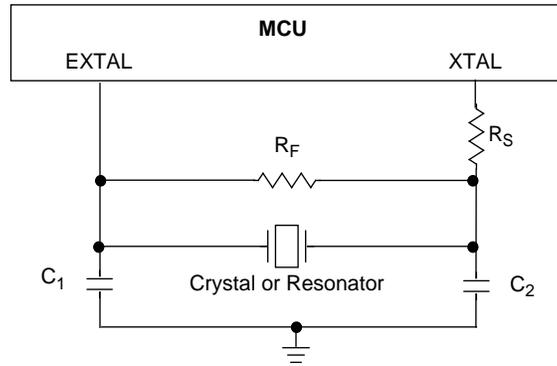
⁶ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁷ The PTE1_{pin} does not have a clamp diode to V_{DD} . Do not drive this pin above V_{DD} .

⁸ Maximum is highest voltage that POR will occur.

⁹ Simulated, not tested

¹⁰ Factory trimmed at $V_{DD} = 5.0$ V, Temp = 25°C



A.11 MCG Specifications

Table A-12. MCG Frequency Specifications (Temperature Range = -40 to 125°C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit	
1	P	Internal reference frequency - factory trimmed at VDD=5.0V and temperature=25C	f_{int_ft}	—	31.25	—	kHz	
2	P	Internal reference frequency - untrimmed ¹	f_{int_ut}	25	36	41.66	kHz	
3	P	Internal reference frequency - user trimmed	f_{int_t}	31.25	—	39.0625	kHz	
4	D	Internal reference startup time	t_{irefst}	—	55	100	us	
5	—	DCO output frequency range - untrimmed ¹	f_{dco_ut}	Low range (DRS=0, DMX32=0) $f_{dco_ut} = 512X f_{int_ut}$	12.8	18.43	21.33	MHz
	—			Mid range (DRS=1, DMX32=0) $f_{dco_ut} = 1024 X f_{int_ut}$	25.6	36.86	42.66	
6	P	DCO output frequency range - trimmed ²	f_{dco_t}	Low range (DRS=0, DMX32=0) $f_{dco_ut} = 512X f_{int_ut}$	16	—	20	MHz
	P			Mid range (DRS=1, DMX32=0) $f_{dco_ut} = 1024 X f_{int_ut}$	32	—	40	
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco_res_t}$	—	± 0.1	± 0.2	% f_{dco}	
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco_res_t}$	—	± 0.2	± 0.4	% f_{dco}	
9	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	% f_{dco}	
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 - 70 °C	Δf_{dco_t}	—	± 0.5	± 1	% f_{dco}	
11	C	FLL acquisition time ³	$t_{fill_acquire}$	—	—	1	ms	
12	D	PLL acquisition time ⁴	$t_{pll_acquire}$	—	—	1	ms	
13	C	Long term Jitter of DCO output clock (averaged over 2mS interval) ⁵	C_{Jitter}	—	0.02	0.2	% f_{dco}	
14	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz	

Table A-12. MCG Frequency Specifications (Temperature Range = -40 to 125°C Ambient) (continued)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
15	D	PLL reference frequency range	$f_{\text{pll_ref}}$	1.0	—	2.0	MHz
16	T	RMS frequency variation of a single clock cycle measured 2 ms after reference edge. ⁶	$f_{\text{pll_cycjit_2ms}}$	—	0.590 ⁵	—	% f_{pll}
17	T	Maximum frequency variation averaged over 2 ms window.	$f_{\text{pll_maxjit_2ms}}$	—	0.001	—	% f_{pll}
18	T	RMS frequency variation of a single clock cycle measured 625 ns after reference edge. ⁷	$f_{\text{pll_cycjit_625ns}}$	—	0.566 ⁵	—	% f_{pll}
19	T	Maximum frequency variation averaged over 625 ns window.	$f_{\text{pll_maxjit_625ns}}$	—	0.113	—	% f_{pll}
20	D	Lock entry frequency tolerance ⁸	D_{lock}	± 1.49	—	± 2.98	%
21	D	Lock exit frequency tolerance ⁹	D_{unl}	± 4.47	—	± 5.97	%
22	D	Lock time - FLL	$t_{\text{fl_lock}}$	—	—	$t_{\text{fl_acquire}} + 1075(1/f_{\text{int_t}})$	s

¹ This applies when TRIM register at value (0x80) and FTRIM control bit at value (0x0). These values load when in BDM modes.

² The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

³ This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁴ This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

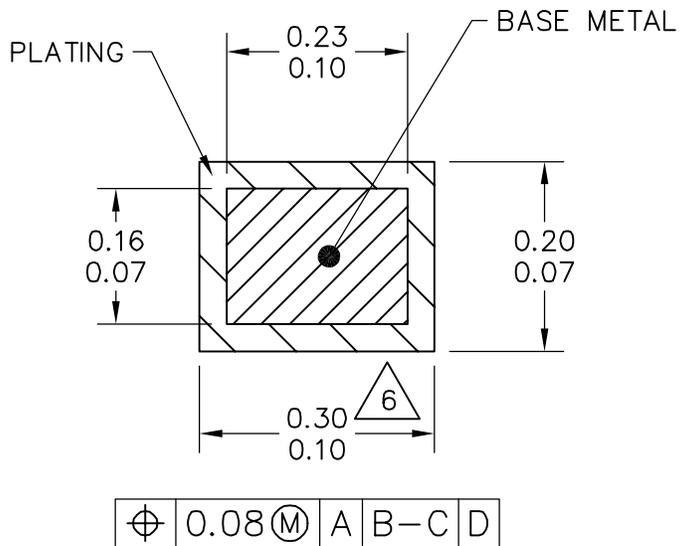
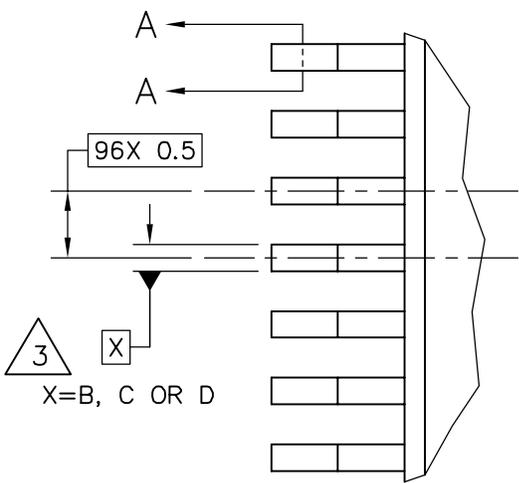
⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval. These jitter measurements are based upon a 40 MHz MCGOUT clock frequency.

⁶ In some specifications, this value is described as, "Long term accuracy of PLL output clock (averaged over 2 ms)" with symbol " $f_{\text{pll_jitter_2ms}}$." The parameter is unchanged, but the description has been changed for clarification purposes.

⁷ In some specifications, this value is described as "Jitter of PLL output clock measured over 625 ns" with symbol " $f_{\text{pll_jitter_625ns}}$." The parameter is unchanged, but the description has been changed for clarification purposes.

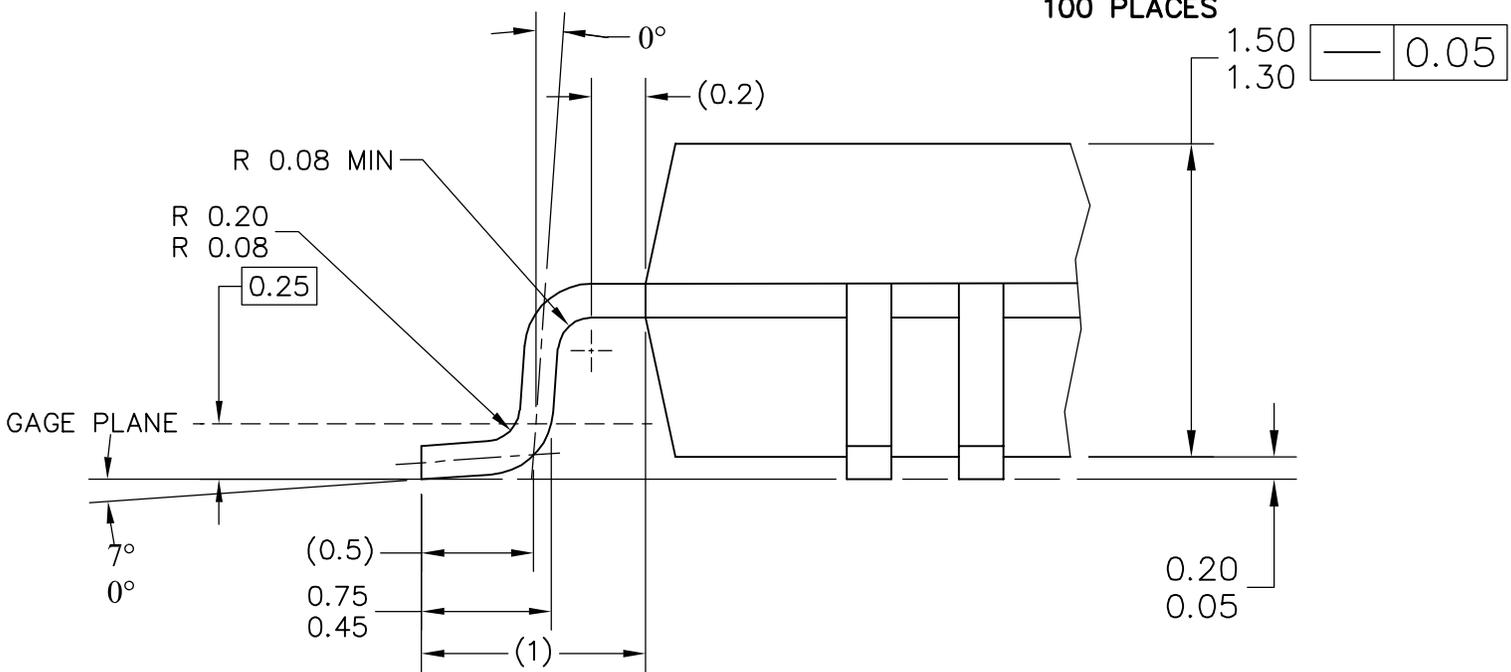
⁸ Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

⁹ Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.



SECTION A-A
 ROTATED 90° CW
 100 PLACES

VIEW A



VIEW B

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: H	
	CASE NUMBER: 983-02	25 MAY 2005	
	STANDARD: NON-JEDEC		