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Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	87
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08dz96mll

Semiconductor-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

6.5.1 Port A Registers

Port A is controlled by the registers listed below.

6.5.1.1 Port A Data Register (PTAD)

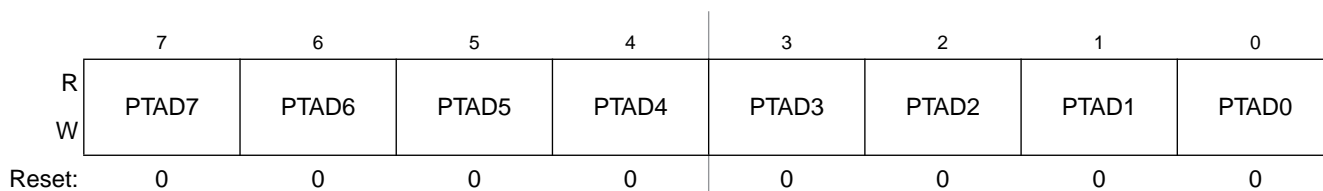


Figure 6-3. Port A Data Register (PTAD)

Table 6-1. PTAD Register Field Descriptions

Field	Description
7:0 PTAD[7:0]	<p>Port A Data Register Bits — For port A pins that are inputs, reads return the logic level on the pin. For port A pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port A pins that are configured as outputs, the logic level is driven out the corresponding MCU pin.</p> <p>Reset forces PTAD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups/pull-downs disabled.</p>

6.5.1.2 Port A Data Direction Register (PTADD)

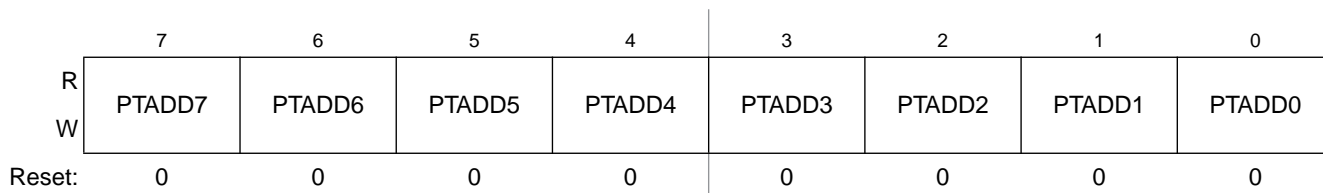


Figure 6-4. Port A Data Direction Register (PTADD)

Table 6-2. PTADD Register Field Descriptions

Field	Description
7:0 PTADD[7:0]	<p>Data Direction for Port A Bits — These read/write bits control the direction of port A pins and what is read for PTAD reads.</p> <p>0 Input (output driver disabled) and reads return the pin value.</p> <p>1 Output driver enabled for port A bit n and PTAD reads return the contents of PTADn.</p>

6.5.2.5 Port B Drive Strength Selection Register (PTBDS)

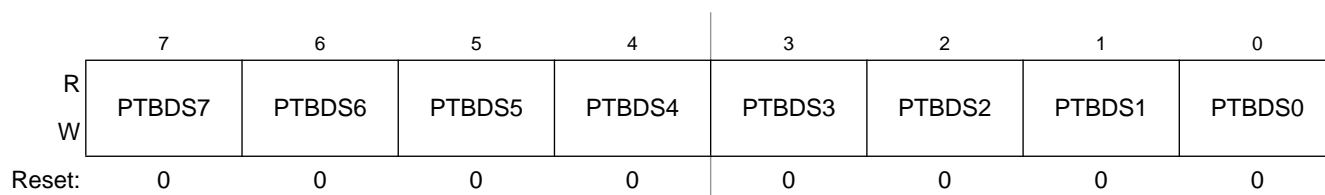


Figure 6-15. Drive Strength Selection for Port B Register (PTBDS)

Table 6-13. PTBDS Register Field Descriptions

Field	Description
7:0 PTBDS[7:0]	Output Drive Strength Selection for Port B Bits — Each of these control bits selects between low and high output drive for the associated PTB pin. For port B pins that are configured as inputs, these bits have no effect. 0 Low output drive strength selected for port B bit n. 1 High output drive strength selected for port B bit n.

6.5.2.6 Port B Interrupt Status and Control Register (PTBSC)

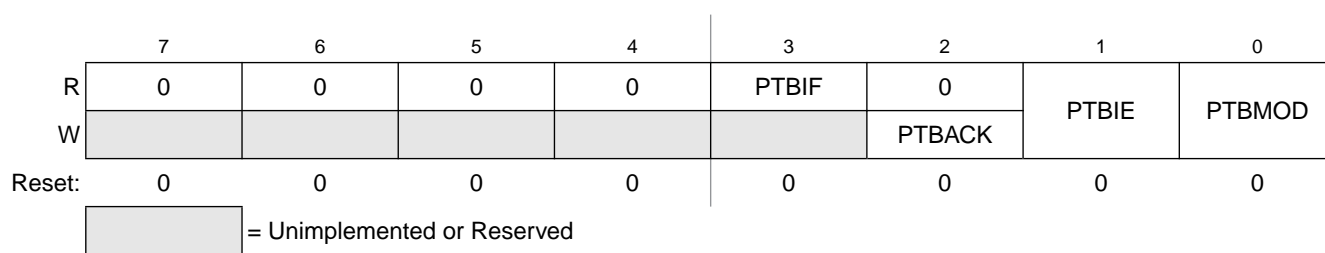


Figure 6-16. Port B Interrupt Status and Control Register (PTBSC)

Table 6-14. PTBSC Register Field Descriptions

Field	Description
3 PTBIF	Port B Interrupt Flag — PTBIF indicates when a Port B interrupt is detected. Writes have no effect on PTBIF. 0 No Port B interrupt detected. 1 Port B interrupt detected.
2 PTBACK	Port B Interrupt Acknowledge — Writing a 1 to PTBACK is part of the flag clearing mechanism. PTBACK always reads as 0.
1 PTBIE	Port B Interrupt Enable — PTBIE determines whether a port B interrupt is requested. 0 Port B interrupt request not enabled. 1 Port B interrupt request enabled.
0 PTBMOD	Port B Detection Mode — PTBMOD (along with the PTBES bits) controls the detection mode of the port B interrupt pins. 0 Port B pins detect edges only. 1 Port B pins detect both edges and levels.

6.5.10.3 Port K Pull Enable Register (PTKPE)

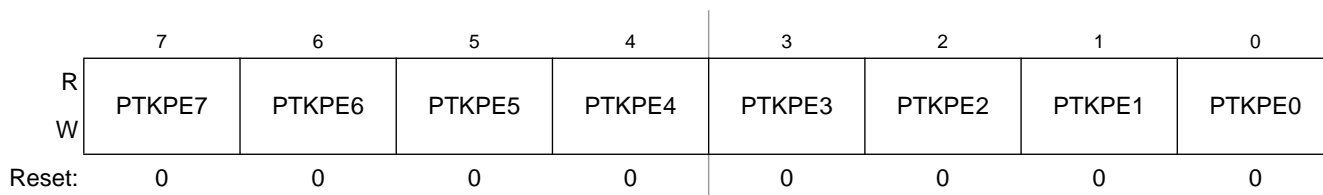


Figure 6-62. Internal Pull Enable for Port K Register (PTKPE)

Table 6-60. PTKPE Register Field Descriptions

Field	Description
7:0 PTKPE[7:0]	<p>Internal Pull Enable for Port K Bits — Each of these control bits determines if the internal pull-up device is enabled for the associated PTK pin. For port K pins that are configured as outputs, these bits have no effect and the internal pull devices are disabled.</p> <p>0 Internal pull-up device disabled for port K bit n. 1 Internal pull-up device enabled for port K bit n.</p>

NOTE

Pull-down devices only apply when using pin interrupt functions, when corresponding edge select and pin select functions are configured.

6.5.10.4 Port K Slew Rate Enable Register (PTKSE)

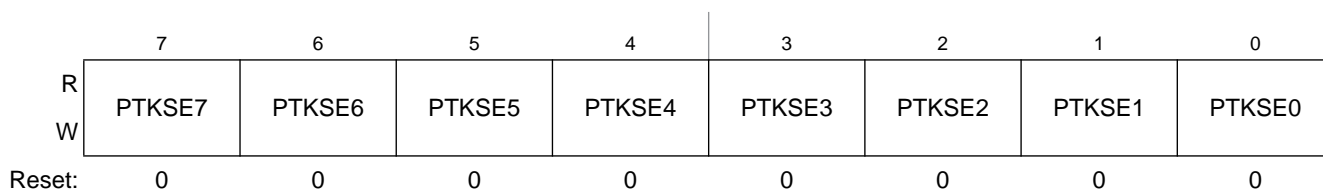


Figure 6-63. Slew Rate Enable for Port K Register (PTKSE)

Table 6-61. PTKSE Register Field Descriptions

Field	Description
7:0 PTKSE[7:0]	<p>Output Slew Rate Enable for Port K Bits — Each of these control bits determines if the output slew rate control is enabled for the associated PTK pin. For port K pins that are configured as inputs, these bits have no effect.</p> <p>0 Output slew rate control disabled for port K bit n. 1 Output slew rate control enabled for port K bit n.</p>

Note: Slew rate reset default values may differ between engineering samples and final production parts. Always initialize slew rate control to the desired value to ensure correct operation.

Table 7-2. Instruction Set Summary (Sheet 8 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR	
						V 1 1 H	I N Z C
SUB #opr8i SUB opr8a SUB opr16a SUB oprx16,X SUB oprx8,X SUB ,X SUB oprx16,SP SUB oprx8,SP	Subtract $A \leftarrow (A) - (M)$	IMM DIR EXT IX2 IX1 IX SP2 SP1	A0 ii B0 dd C0 hh ll D0 ee ff E0 ff F0 9E D0 ee ff 9E E0 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	\uparrow 1 1 -	- \uparrow \uparrow \uparrow
SWI	Software Interrupt $PC \leftarrow (PC) + \$0001$ Push (PCL); $SP \leftarrow (SP) - \$0001$ Push (PCH); $SP \leftarrow (SP) - \$0001$ Push (X); $SP \leftarrow (SP) - \$0001$ Push (A); $SP \leftarrow (SP) - \$0001$ Push (CCR); $SP \leftarrow (SP) - \$0001$ $I \leftarrow 1$; PCH \leftarrow Interrupt Vector High Byte PCL \leftarrow Interrupt Vector Low Byte	INH	83	11	sssssvvfppp	- 1 1 -	1 - - -
TAP	Transfer Accumulator to CCR $CCR \leftarrow (A)$	INH	84	1	p	\uparrow 1 1 \uparrow	\uparrow \uparrow \uparrow \uparrow
TAX	Transfer Accumulator to X (Index Register Low) $X \leftarrow (A)$	INH	97	1	p	- 1 1 -	- - - -
TPA	Transfer CCR to Accumulator $A \leftarrow (CCR)$	INH	85	1	p	- 1 1 -	- - - -
TST opr8a TSTA TSTX TST oprx8,X TST ,X TST oprx8,SP	Test for Negative or Zero (M) - \$00 (A) - \$00 (X) - \$00 (M) - \$00 (M) - \$00 (M) - \$00	DIR INH INH IX1 IX SP1	3D dd 4D 5D 6D ff 7D 9E 6D ff	4 1 1 4 3 5	rfpp p p rfpp rfp prfpp	0 1 1 -	- \uparrow \uparrow -
TSX	Transfer SP to Index Reg. $H:X \leftarrow (SP) + \$0001$	INH	95	2	fp	- 1 1 -	- - - -
TXA	Transfer X (Index Reg. Low) to Accumulator $A \leftarrow (X)$	INH	9F	1	p	- 1 1 -	- - - -

reference can achieve a high-range maximum DCO output of 39.85 MHz with a multiplier of 1216. When the DRS bit is clear, the 32.768 kHz reference can achieve a mid-range maximum DCO output of 19.92 MHz with a multiplier of 608.

In FBI and FEI modes, setting the DMX32 bit is not recommended. If the internal reference is trimmed to a frequency above 32.768 kHz, the greater FLL multiplication factor could potentially push the microcontroller system clock out of specification and damage the part.

8.5.3 MCG Mode Switching

When switching between operational modes of the MCG, certain configuration bits must be changed in order to properly move from one mode to another. Each time any of these bits are changed (PLLS, IREFS, CLKS, or EREFS), the corresponding bits in the MCGSC register (PLLST, IREFST, CLKST, or OSCINIT) must be checked before moving on in the application software.

Additionally, care must be taken to ensure that the reference clock divider (RDIV) is set properly for the mode being switched to. For instance, in PEE mode, if using a 4 MHz crystal, RDIV must be set to %001 (divide-by-2) or %010 (divide -by-4) in order to divide the external reference down to the required frequency between 1 and 2 MHz.

If switching to FBE or FEE mode, first setting the DIV32 bit will ensure a proper reference frequency is sent to the FLL clock at all times.

In FBE, FEE, FBI, and FEI modes, at any time, the application can switch the FLL multiplication factor between 1024 and 512 with the DRS bit in MCGT. Writes to DRS will be ignored if LP=1 or PLLS=1.

The RDIV and IREFS bits should always be set properly before changing the PLLS bit so that the FLL or PLL clock has an appropriate reference clock frequency to switch to. The table below shows MCGOUT frequency calculations using RDIV, BDIV, and VDIV settings for each clock mode. The bus frequency is equal to MCGOUT divided by 2.

Table 8-10. MCGOUT Frequency Calculation Options

Clock Mode	f_{MCGOUT}^1	Note
FEI (FLL engaged internal)	$(f_{int} * F) / B$	Typical $f_{MCGOUT} = 16$ MHz immediately after reset.
FEE (FLL engaged external)	$(f_{ext} / R * F) / B$	f_{ext} / R must be in the range of 31.25 kHz to 39.0625 kHz
FBE (FLL bypassed external)	f_{ext} / B	f_{ext} / R must be in the range of 31.25 kHz to 39.0625 kHz
FBI (FLL bypassed internal)	f_{int} / B	Typical $f_{int} = 32$ kHz
PEE (PLL engaged external)	$[(f_{ext} / R) * M] / B$	f_{ext} / R must be in the range of 1 MHz to 2 MHz
PBE (PLL bypassed external)	f_{ext} / B	f_{ext} / R must be in the range of 1 MHz to 2 MHz
BLPI (Bypassed low power internal)	f_{int} / B	
BLPE (Bypassed low power external)	f_{ext} / B	

9.2 External Signal Description

The ACMP has two analog input pins, ACMPx+ and ACMPx- and one digital output pin ACMPxO. Each of these pins can accept an input voltage that varies across the full operating voltage range of the MCU. As shown in [Figure 9-2](#), the ACMPx- pin is connected to the inverting input of the comparator, and the ACMPx+ pin is connected to the comparator non-inverting input if ACBGS is a 0. As shown in [Figure 9-2](#), the ACMPxO pin can be enabled to drive an external pin.

The signal properties of ACMP are shown in [Table 9-1](#).

Table 9-1. Signal Properties

Signal	Function	I/O
ACMPx-	Inverting analog input to the ACMP. (Minus input)	I
ACMPx+	Non-inverting analog input to the ACMP. (Positive input)	I
ACMPxO	Digital output of the ACMP.	O

9.3 Memory Map

9.3.1 Register Descriptions

The ACMP includes one register:

- An 8-bit status and control register

Refer to the direct-page register summary in the memory section of this data sheet for the absolute address assignments for all ACMP registers. This section refers to registers and control bits only by their names .

Some MCUs may have more than one ACMP, so register names include placeholder characters to identify which ACMP is being referenced.

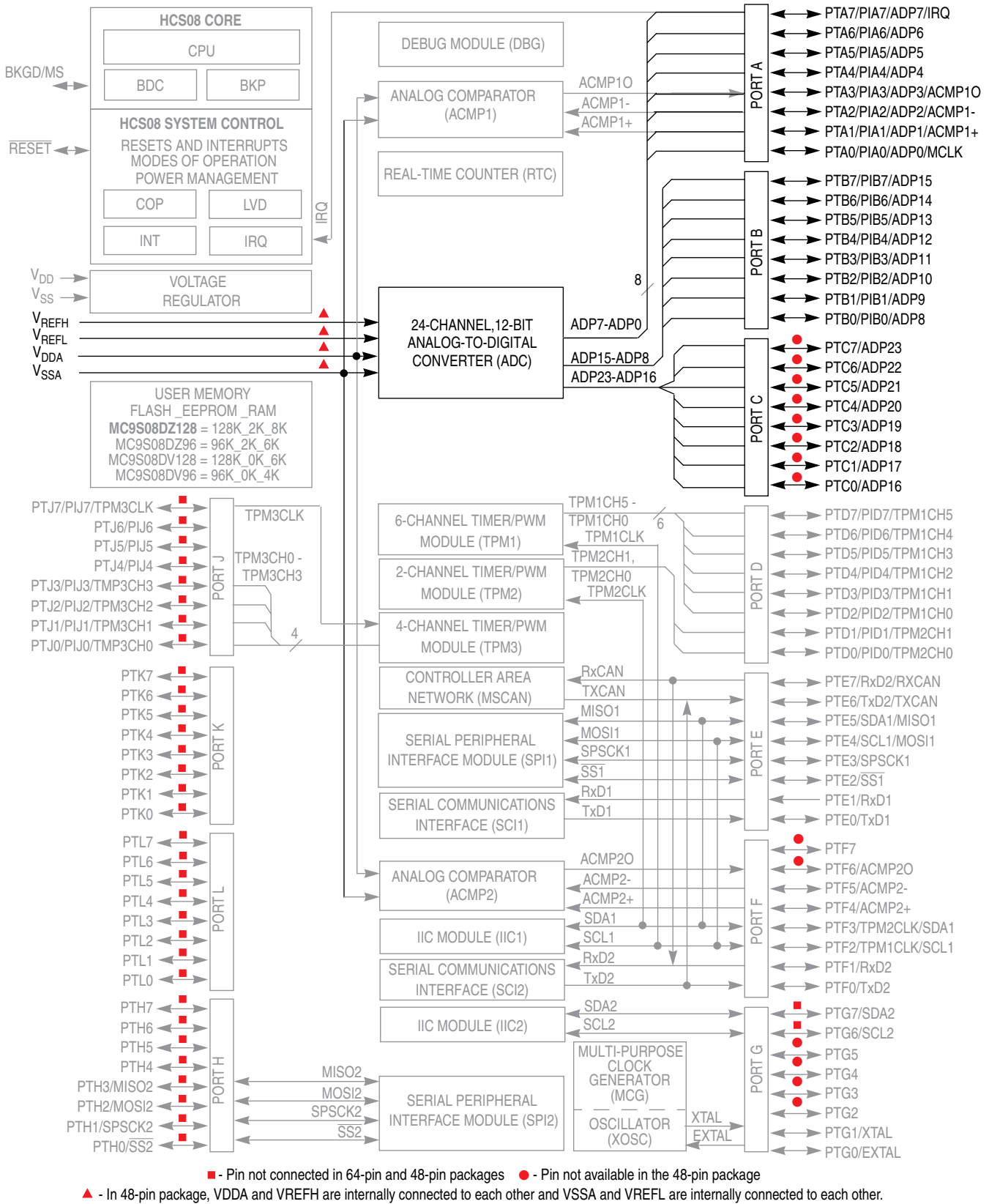


Figure 10-1. MC9S08DZ128 Block Diagram with ADC Highlighted

In 10-bit mode, the ADCCVH register holds the upper two bits of the 10-bit compare value (ADCV[9:8]). These bits are compared to the upper two bits of the result following a conversion in 10-bit mode when the compare function is enabled.

In 8-bit mode, ADCCVH is not used during compare.

10.3.6 Compare Value Low Register (ADCCVL)

This register holds the lower 8 bits of the 12-bit or 10-bit compare value or all 8 bits of the 8-bit compare value. When the compare function is enabled, bits ADCV[7:0] are compared to the lower 8 bits of the result following a conversion in 12-bit, 10-bit or 8-bit mode.

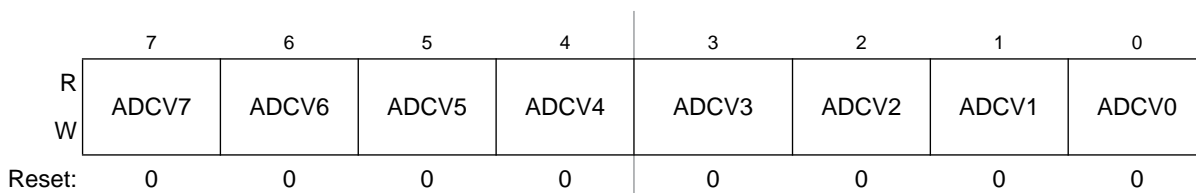


Figure 10-8. Compare Value Low Register(ADCCVL)

10.3.7 Configuration Register (ADCCFG)

ADCCFG selects the mode of operation, clock source, clock divide, and configures for low power and long sample time.

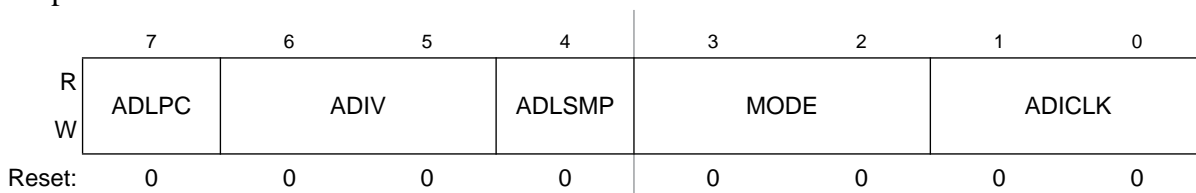


Figure 10-9. Configuration Register (ADCCFG)

Table 10-6. ADCCFG Register Field Descriptions

Field	Description
7 ADLPC	Low-Power Configuration. ADLPC controls the speed and power configuration of the successive approximation converter. This optimizes power consumption when higher sample rates are not required. 0 High speed configuration 1 Low power configuration:The power is reduced at the expense of maximum clock speed.
6:5 ADIV	Clock Divide Select. ADIV selects the divide ratio used by the ADC to generate the internal clock ADCK. Table 10-7 shows the available clock configurations.
4 ADLSMP	Long Sample Time Configuration. ADLSMP selects between long and short sample time. This adjusts the sample period to allow higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption when continuous conversions are enabled if high conversion rates are not required. 0 Short sample time 1 Long sample time

Table 10-12. APCTL3 Register Field Descriptions

Field	Description
7 ADPC23	ADC Pin Control 23. ADPC23 controls the pin associated with channel AD23. 0 AD23 pin I/O control enabled 1 AD23 pin I/O control disabled
6 ADPC22	ADC Pin Control 22. ADPC22 controls the pin associated with channel AD22. 0 AD22 pin I/O control enabled 1 AD22 pin I/O control disabled
5 ADPC21	ADC Pin Control 21. ADPC21 controls the pin associated with channel AD21. 0 AD21 pin I/O control enabled 1 AD21 pin I/O control disabled
4 ADPC20	ADC Pin Control 20. ADPC20 controls the pin associated with channel AD20. 0 AD20 pin I/O control enabled 1 AD20 pin I/O control disabled
3 ADPC19	ADC Pin Control 19. ADPC19 controls the pin associated with channel AD19. 0 AD19 pin I/O control enabled 1 AD19 pin I/O control disabled
2 ADPC18	ADC Pin Control 18. ADPC18 controls the pin associated with channel AD18. 0 AD18 pin I/O control enabled 1 AD18 pin I/O control disabled
1 ADPC17	ADC Pin Control 17. ADPC17 controls the pin associated with channel AD17. 0 AD17 pin I/O control enabled 1 AD17 pin I/O control disabled
0 ADPC16	ADC Pin Control 16. ADPC16 controls the pin associated with channel AD16. 0 AD16 pin I/O control enabled 1 AD16 pin I/O control disabled

10.4 Functional Description

The ADC module is disabled during reset or when the ADCH bits are all high. The module is idle when a conversion has completed and another conversion has not been initiated. When idle, the module is in its lowest power state.

The ADC can perform an analog-to-digital conversion on any of the software selectable channels. In 12-bit and 10-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 12-bit digital result. In 8-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 9-bit digital result.

When the conversion is completed, the result is placed in the data registers (ADCRH and ADCRL). In 10-bit mode, the result is rounded to 10 bits and placed in the data registers (ADCRH and ADCRL). In 8-bit mode, the result is rounded to 8 bits and placed in ADCRL. The conversion complete flag (COCO) is then set and an interrupt is generated if the conversion complete interrupt has been enabled (AIEN = 1).

The ADC module has the capability of automatically comparing the result of a conversion with the contents of its compare registers. The compare function is enabled by setting the ACFE bit and operates with any of the conversion modes and configurations.

When a conversion is aborted, the contents of the data registers, ADCRH and ADCRL, are not altered. However, they continue to be the values transferred after the completion of the last successful conversion. If the conversion was aborted by a reset, ADCRH and ADCRL return to their reset states.

10.4.4.4 Power Control

The ADC module remains in its idle state until a conversion is initiated. If ADACK is selected as the conversion clock source, the ADACK clock generator is also enabled.

Power consumption when active can be reduced by setting ADLPC. This results in a lower maximum value for f_{ADCK} (see the electrical specifications).

10.4.4.5 Sample Time and Total Conversion Time

The total conversion time depends on the sample time (as determined by ADLSMP), the MCU bus frequency, the conversion mode (8-bit, 10-bit or 12-bit), and the frequency of the conversion clock (f_{ADCK}). After the module becomes active, sampling of the input begins. ADLSMP selects between short (3.5 ADCK cycles) and long (23.5 ADCK cycles) sample times. When sampling is complete, the converter is isolated from the input channel and a successive approximation algorithm is performed to determine the digital value of the analog signal. The result of the conversion is transferred to ADCRH and ADCRL upon completion of the conversion algorithm.

If the bus frequency is less than the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when short sample is enabled (ADLSMP=0). If the bus frequency is less than 1/11th of the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when long sample is enabled (ADLSMP=1).

The maximum total conversion time for different conditions is summarized in [Table 10-13](#).

Table 10-13. Total Conversion Time vs. Control Conditions

Conversion Type	ADICLK	ADLSMP	Max Total Conversion Time
Single or first continuous 8-bit	0x, 10	0	20 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	0x, 10	0	23 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	0x, 10	1	40 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	0x, 10	1	43 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	11	0	5 μ s + 20 ADCK + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	11	0	5 μ s + 23 ADCK + 5 bus clock cycles
Single or first continuous 8-bit	11	1	5 μ s + 40 ADCK + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	11	1	5 μ s + 43 ADCK + 5 bus clock cycles
Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}$	xx	0	17 ADCK cycles
Subsequent continuous 10-bit or 12-bit; $f_{BUS} \geq f_{ADCK}$	xx	0	20 ADCK cycles
Subsequent continuous 8-bit; $f_{BUS} \geq f_{ADCK}/11$	xx	1	37 ADCK cycles

Table 12-1. CANCTL0 Register Field Descriptions (continued)

Field	Description
1 SLPRQ ⁵	<p>Sleep Mode Request — This bit requests the MSCAN to enter sleep mode, which is an internal power saving mode (see Section 12.5.5.4, “MSCAN Sleep Mode”). The sleep mode request is serviced when the CAN bus is idle, i.e., the module is not receiving a message and all transmit buffers are empty. The module indicates entry to sleep mode by setting SLPK = 1 (see Section 12.3.2, “MSCAN Control Register 1 (CANCTL1)”). SLPRQ cannot be set while the WUPIF flag is set (see Section 12.3.4.1, “MSCAN Receiver Flag Register (CANRFLG)”). Sleep mode will be active until SLPRQ is cleared by the CPU or, depending on the setting of WUPE, the MSCAN detects activity on the CAN bus and clears SLPRQ itself.</p> <p>0 Running — The MSCAN functions normally</p> <p>1 Sleep mode request — The MSCAN enters sleep mode when CAN bus idle</p>
0 INITRQ ^{6,7}	<p>Initialization Mode Request — When this bit is set by the CPU, the MSCAN skips to initialization mode (see Section 12.5.5.5, “MSCAN Initialization Mode”). Any ongoing transmission or reception is aborted and synchronization to the CAN bus is lost. The module indicates entry to initialization mode by setting INITAK = 1 (Section 12.3.2, “MSCAN Control Register 1 (CANCTL1)”).</p> <p>The following registers enter their hard reset state and restore their default values: CANCTL0⁸, CANRFLG⁹, CANRIER¹⁰, CANTFLG, CANTIER, CANTARQ, CANTAACK, and CANTBSEL.</p> <p>The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0-7, and CANIDMR0-7 can only be written by the CPU when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1). The values of the error counters are not affected by initialization mode.</p> <p>When this bit is cleared by the CPU, the MSCAN restarts and then tries to synchronize to the CAN bus. If the MSCAN is not in bus-off state, it synchronizes after 11 consecutive recessive bits on the CAN bus; if the MSCAN is in bus-off state, it continues to wait for 128 occurrences of 11 consecutive recessive bits.</p> <p>Writing to other bits in CANCTL0, CANRFLG, CANRIER, CANTFLG, or CANTIER must be done only after initialization mode is exited, which is INITRQ = 0 and INITAK = 0.</p> <p>0 Normal operation</p> <p>1 MSCAN in initialization mode</p>

¹ The MSCAN must be in normal mode for this bit to become set.

² See the Bosch CAN 2.0A/B specification for a detailed definition of transmitter and receiver states.

³ In order to protect from accidentally violating the CAN protocol, the TXCAN pin is immediately forced to a recessive state when the CPU enters wait (CSWAI = 1) or stop mode (see Section 12.5.5.2, “Operation in Wait Mode” and Section 12.5.5.3, “Operation in Stop Mode”).

⁴ The CPU has to make sure that the WUPE bit and the WUPIE wake-up interrupt enable bit (see Section 12.3.5, “MSCAN Receiver Interrupt Enable Register (CANRIER)”) is enabled, if the recovery mechanism from stop or wait is required.

⁵ The CPU cannot clear SLPRQ before the MSCAN has entered sleep mode (SLPRQ = 1 and SLPK = 1).

⁶ The CPU cannot clear INITRQ before the MSCAN has entered initialization mode (INITRQ = 1 and INITAK = 1).

⁷ In order to protect from accidentally violating the CAN protocol, the TXCAN pin is immediately forced to a recessive state when the initialization mode is requested by the CPU. Thus, the recommended procedure is to bring the MSCAN into sleep mode (SLPRQ = 1 and SLPK = 1) before requesting initialization mode.

⁸ Not including WUPE, INITRQ, and SLPRQ.

⁹ TSTAT1 and TSTAT0 are not affected by initialization mode.

¹⁰ RSTAT1 and RSTAT0 are not affected by initialization mode.

Table 16-2. TPMxSC Field Descriptions (continued)

Field	Description
4–3 CLKS[B:A]	Clock source selects. As shown in Table 16-3 , this 2-bit field is used to disable the TPM system or select one of three clock sources to drive the counter prescaler. The fixed system clock source is only meaningful in systems with a PLL-based or FLL-based system clock. When there is no PLL or FLL, the fixed-system clock source is the same as the bus rate clock. The external source is synchronized to the bus clock by TPM module, and the fixed system clock source (when a PLL or FLL is present) is synchronized to the bus clock by an on-chip synchronization circuit. When a PLL or FLL is present but not enabled, the fixed-system clock source is the same as the bus-rate clock.
2–0 PS[2:0]	Prescale factor select. This 3-bit field selects one of 8 division factors for the TPM clock input as shown in Table 16-4 . This prescaler is located after any clock source synchronization or clock source selection so it affects the clock source selected to drive the TPM system. The new prescale factor will affect the clock source on the next system clock cycle after the new value is updated into the register bits.

Table 16-3. TPM-Clock-Source Selection

CLKSB:CLKSA	TPM Clock Source to Prescaler Input
00	No clock selected (TPM counter disable)
01	Bus rate clock
10	Fixed system clock
11	External source

Table 16-4. Prescale Factor Selection

PS2:PS1:PS0	TPM Clock Source Divided-by
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

16.3.2 TPM-Counter Registers (TPMxCNTH:TPMxCNTL)

The two read-only TPM counter registers contain the high and low bytes of the value in the TPM counter. Reading either byte (TPMxCNTH or TPMxCNTL) latches the contents of both bytes into a buffer where they remain latched until the other half is read. This allows coherent 16-bit reads in either big-endian or little-endian order which makes this more friendly to various compiler implementations. The coherency mechanism is automatically restarted by an MCU reset or any write to the timer status/control register (TPMxSC).

18.3 Memory Map and Registers

This section provides a detailed description of all DBG registers accessible to the end user.

18.3.1 Module Memory Map

Table 18-1 shows the registers contained in the DBG module.

Table 18-1. Module Memory Map

Address	Use	Access
Base + \$0000	Debug Comparator A High Register (DBGCAH)	Read/write
Base + \$0001	Debug Comparator A Low Register (DBGCAL)	Read/write
Base + \$0002	Debug Comparator B High Register (DBGCBH)	Read/write
Base + \$0003	Debug Comparator B Low Register (DBGCBL)	Read/write
Base + \$0004	Debug Comparator C High Register (DBGCCH)	Read/write
Base + \$0005	Debug Comparator C Low Register (DBGCCL)	Read/write
Base + \$0006	Debug FIFO High Register (DBGFH)	Read only
Base + \$0007	Debug FIFO Low Register (DBGFL)	Read only
Base + \$0008	Debug Comparator A Extension Register (DBGCAE)	Read/write
Base + \$0009	Debug Comparator B Extension Register (DBGCBX)	Read/write
Base + \$000A	Debug Comparator C Extension Register (DBGCCX)	Read/write
Base + \$000B	Debug FIFO Extended Information Register (DBGFX)	Read only
Base + \$000C	Debug Control Register (DBGCR)	Read/write
Base + \$000D	Debug Trigger Register (DBGTR)	Read/write
Base + \$000E	Debug Status Register (DBGSR)	Read only
Base + \$000F	Debug FIFO Count Register (DBGFCNT)	Read only

18.3.3.13 Debug Control Register (DBGC)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	DBGEN	ARM	TAG	BRKEN	0	0	0	LOOP1
W								
POR or non-end-run	1	1	0	0	0	0	0	0
Reset end-run ¹	U	0	U	0	0	0	0	U

= Unimplemented or Reserved

Figure 18-14. Debug Control Register (DBGC)

¹ In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, the ARM and BRKEN bits are cleared but the remaining control bits in this register do not change after reset.

Table 18-15. DBGC Field Descriptions

Field	Description
7 DBGEN	DBG Module Enable Bit — The DBGEN bit enables the DBG module. The DBGEN bit is forced to zero and cannot be set if the MCU is secure. 0 DBG not enabled 1 DBG enabled
6 ARM	Arm Bit — The ARM bit controls whether the debugger is comparing and storing data in FIFO. See Section 18.4.4.2, “Arming the DBG Module” for more information. 0 Debugger not armed 1 Debugger armed
5 TAG	Tag or Force Bit — The TAG bit controls whether a debugger or comparator C breakpoint will be requested as a tag or force breakpoint to the CPU. The TAG bit is not used if BRKEN = 0. 0 Force request selected 1 Tag request selected
4 BRKEN	Break Enable Bit — The BRKEN bit controls whether the debugger will request a breakpoint to the CPU at the end of a trace run, and whether comparator C will request a breakpoint to the CPU. 0 CPU break request not enabled 1 CPU break request enabled
0 LOOP1	Select LOOP1 Capture Mode — This bit selects either normal capture mode or LOOP1 capture mode. LOOP1 is not used in event-only modes. 0 Normal operation - capture COF events into the capture buffer FIFO 1 LOOP1 capture mode enabled. When the conditions are met to store a COF value into the FIFO, compare the current COF address with the address in comparator C. If these addresses match, override the FIFO capture and do not increment the FIFO count. If the address does not match comparator C, capture the COF address, including the PPACC indicator, into the FIFO and into comparator C.

18.3.3.14 Debug Trigger Register (DBGT)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	TRGSEL	BEGIN	0	0	TRG			
W ²								
POR or non-end-run	0	1	0	0	0	0	0	0
Reset end-run ¹	U	U	0	0	U	U	U	U

= Unimplemented or Reserved

Figure 18-15. Debug Trigger Register (DBGT)

¹ In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, the control bits in this register do not change after reset.

² The DBG trigger register (DBGT) can not be changed unless ARM=0.

Table 18-16. DBGT Field Descriptions

Field	Description
7 TRGSEL	Trigger Selection Bit — The TRGSEL bit controls the triggering condition for the comparators. See Section 18.4.4, “Trigger Break Control (TBC)” for more information. 0 Trigger on any compare address access 1 Trigger if opcode at compare address is executed
6 BEGIN	Begin/End Trigger Bit — The BEGIN bit controls whether the trigger begins or ends storing of data in FIFO. 0 Trigger at end of stored data 1 Trigger before storing data
3–0 TRG	Trigger Mode Bits — The TRG bits select the trigger mode of the DBG module as shown in Table 18-17 .

Table 18-17. Trigger Mode Encoding

TRG Value	Meaning
0000	A Only
0001	A Or B
0010	A Then B
0011	Event Only B
0100	A Then Event Only B
0101	A And B (Full Mode)
0110	A And Not B (Full mode)
0111	Inside Range
1000	Outside Range

- $DBGCAx=0x00$, $DBGCAH=0xFF$, $DBGCAL=0xFE$ so comparator A is set to match when the 16-bit CPU address $0xFFFFE$ appears during the reset vector fetch
- $DBGC=0xC0$ to enable and arm the DBG module
- $DBGT=0x40$ to select a force-type trigger, a BEGIN trigger, and A-only trigger mode

18.6 Interrupts

The DBG contains no interrupt source.

18.7 Electrical Specifications

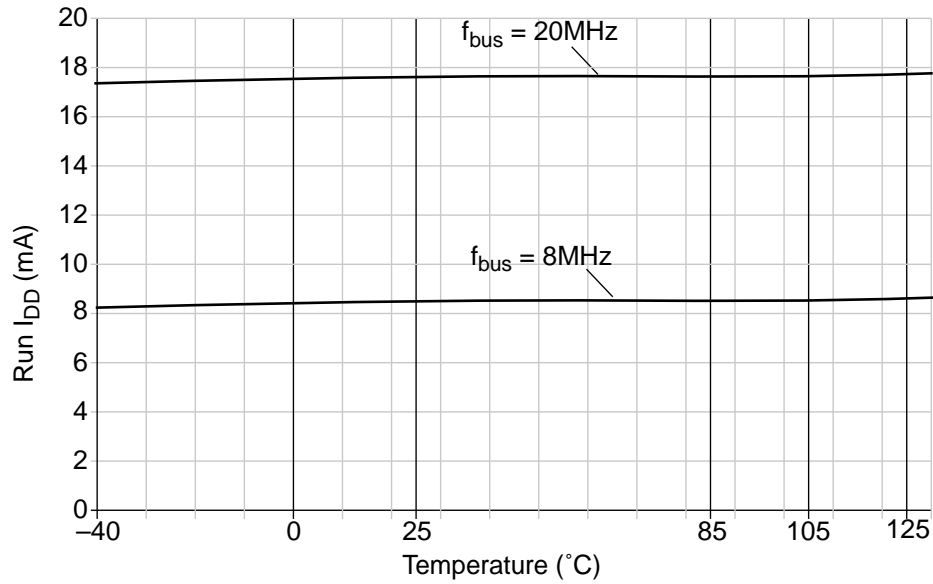
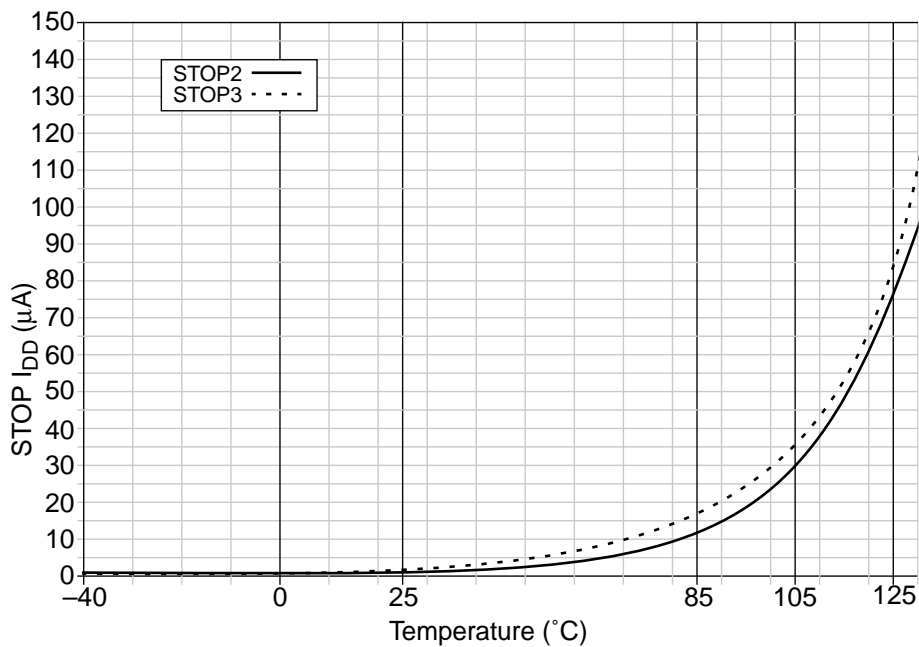
The DBG module contain no electrical specifications.

A.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table A-7. Supply Current Characteristics

Num	C	Parameter	Symbol	V _{DD} (V)	Typ ¹	Max ²	Unit
1	C	Run supply current ³ measured at (CPU clock = 2 MHz, f _{Bus} = 1 MHz)	R _I DD	5	2.1	3 ⁴	mA
	C			3	2.0	2.5	
2	C	Run supply current ³ measured at (CPU clock = 16 MHz, f _{Bus} = 8 MHz)	R _I DD	5	8.4	9 ⁴	4.6
	C			3	8.3	8.7	
3	P	Run supply current ⁴ measured at (CPU clock = 40 MHz, f _{Bus} = 20MHz)	R _I DD	5	17.9	24	mA
	C			3	17.8	23	
Stop3 mode supply current							
4	C	-40°C (C,V, & M suffix) 25°C (All parts) 85°C (C suffix only) 105°C (V suffix only) 125°C (M suffix only)	S ₃ I _{DD}	5	0.7	—	μA
	P				1.1	—	
	p ⁵				14.8	18.5	
	p ⁵				38.8	49	
	p ⁵				172	257	
	C	-40°C (C,V, & M suffix) 25°C (All parts) 85°C (C suffix only) 105°C (V suffix only) 125°C (M suffix only)	S ₃ I _{DD}	3	0.34	—	μA
	P				0.79	—	
	p ⁵				12.7	15	
	p ⁵				33.6	42.4	
	p ⁵				159	208	
Stop2 mode supply current							
5	C	-40°C (C,M, & V suffix) 25°C (All parts) 85°C (C suffix only) 105°C (V suffix only) 125°C (M suffix only)	S ₂ I _{DD}	5	0.65	—	μA
	P				0.94	—	
	p ⁵				11.3	14	
	p ⁵				29.7	37.4	
	p ⁵				140	220	
	C	-40°C (C,M, & V suffix) 25°C (All parts) 85°C (C suffix only) 105°C (V suffix only) 125°C (M suffix only)	S ₂ I _{DD}	3	0.33	—	μA
	P				0.69	—	
	p ⁵				9.4	11.6	
	p ⁵				25	31.3	
	p ⁵				95	155	
6	P	RTC adder to stop2 or stop3 ⁶	S ₂₃ I _{DDRTI}	5	300	500	nA
	P			3	300	500	nA
7	P	LVD adder to stop3 (LVDE = LVDSE = 1)	S ₃ I _{DDLVD}	5	110	180	μA
	P			3	90	160	μA


 Figure A-6. Typical Run I_{DD} vs. Temperature ($V_{DD} = 5V$)

 Figure A-7. Typical Stop I_{DD} vs. Temperature ($V_{DD} = 5V$)

A.8 Analog Comparator (ACMP) Electricals

Table A-8. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

△4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

△5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.

△6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

△7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

△8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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	CASE NUMBER: 840F-02	11 AUG 2006	
	STANDARD: JEDEC MS-026 BCD		