NXP USA Inc. - <u>S9S08DZ128F2CLH Datasheet</u>





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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08dz128f2clh

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Table 1-2 provides the functional version of the on-chip modules.Table 1-2. Module Versions

Module		Version
Central Processor Unit	(CPU)	5
Analog Comparator (5V)	(ACMP_5V)	3
Analog-to-Digital Converter	(ADC)	1
Debug Module	(DBG)	3
Inter-Integrated Circuit	(IIC)	2
Multi-Purpose Clock Generator	(MCG)	2
Freescale's Controller Area Network	(MSCAN)	1
Serial Peripheral Interface	(SPI)	3
Serial Communications Interface	(SCI)	4
Real-Time Counter	(RTC)	1
Timer Pulse Width Modulator	(TPM)	3

1.2 MCU Block Diagram

Figure 1-1 is the MC9S08DZ128 Series system-level block diagram.





Figure 2-2. MC9S08DZ128 Series in 64-Pin LQFP Package



Vector Number	Address (High/Low)	Vector Name	Module	Source	Enable	Description
6	0xFFF2/0xFFF3	Vtpm1ch1	TPM1	CH1F	CH1IE	TPM1 channel 1
5	0xFFF4/0xFFF5	Vtpm1ch0	TPM1	CH0F	CH0IE	TPM1 channel 0
4	0xFFF6/0xFFF7	Vlol	MCG	LOLS	LOLIE	MCG loss of lock
3	0xFFF8/0xFFF9	Vlvd	System control	LVWF	LVWIE	Low-voltage warning
2	0xFFFA/0xFFFB	Virq	IRQ	IRQF	IRQIE	IRQ pin
1	0xFFFC/0xFFFD	Vswi	Core	SWI Instruction	—	Software interrupt
0	0xFFFE/0xFFFF	Vreset	System control	COP, LOC, LVD, RESET, ILOP, ILAD, POR, BDFR	COPT CME LVDRE — — — — — — —	Watchdog timer Loss-of-clock Low-voltage detect External pin Illegal opcode Illegal address Power-on-reset BDM-forced reset

¹ Vector priority is shown from lowest (first row) to highest (last row). For example, Vreset is the highest priority vector.

5.6 Low-Voltage Detect (LVD) System

The MC9S08DZ128 Series includes a system to protect against low-voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. The system is comprised of a power-on reset (POR) circuit and a LVD circuit with trip voltages for warning and detection. The LVD circuit is enabled when LVDE in SPMSC1 is set to 1. The LVD is disabled upon entering any of the stop modes unless LVDSE is set in SPMSC1. If LVDSE and LVDE are both set, then the MCU cannot enter stop2 (it will enter stop3 instead), and the current consumption in stop3 with the LVD enabled will be higher.

5.6.1 Power-On Reset Operation

When power is initially applied to the MCU, or when the supply voltage drops below the power-on reset rearm voltage level, V_{POR} , the POR circuit will cause a reset condition. As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above the low-voltage detection low threshold, V_{LVDL} . Both the POR bit and the LVD bit in SRS are set following a POR.

5.6.2 Low-Voltage Detection (LVD) Reset Operation

The LVD can be configured to generate a reset upon detection of a low-voltage condition by setting LVDRE to 1. The low-voltage detection threshold is determined by the LVDV bit. After an LVD reset has occurred, the LVD system will hold the MCU in reset until the supply voltage has risen above the low-voltage detection threshold. The LVD bit in the SRS register is set following either an LVD reset or POR.



Chapter 6 Parallel Input/Output Control

6.5.4 Port D Registers

Port D is controlled by the registers listed below.

6.5.4.1 Port D Data Register (PTDD)



Figure 6-24. Port D Data Register (PTDD)

Table 6-22. PTDD Register Field Descriptions

Field	Description
7:0 PTDD[7:0]	Port D Data Register Bits — For port D pins that are inputs, reads return the logic level on the pin. For port D pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port D pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTDD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups/pull-downs disabled.

6.5.4.2 Port D Data Direction Register (PTDDD)

_	7	6	5	4	3	2	1	0
R	דחחדם	DTDDE			20072	נחחדם	וחחדם	
w	FIDDDI	FIDDDo	FIDDD3	FIDDD4	FIDD03	FIDDDZ	ועסטוא	FIDDDU
Reset:	0	0	0	0	0	0	0	0

Figure 6-25. Port D Data Direction Register (PTDDD)

Table 6-23. PTDDD Register Field Descriptions

Field	Description
7:0 PTDDD[7:0]	Data Direction for Port D Bits — These read/write bits control the direction of port D pins and what is read for PTDD reads.
	 Input (output driver disabled) and reads return the pin value. Output driver enabled for port D bit n and PTDD reads return the contents of PTDDn.



Chapter 7 Central Processor Unit (S08CPUV5)



Figure 7-2. Condition Code Register

Table 7-1. CCR Register Field Descriptions

Field	Description
7 V	 Two's Complement Overflow Flag — The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag. No overflow Overflow
4 H	 Half-Carry Flag — The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C condition code bits to automatically add a correction value to the result from a previous ADD or ADC on BCD operands to correct the result to a valid BCD value. 0 No carry between bits 3 and 4 1 Carry between bits 3 and 4
3	Interrupt Mask Bit — When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the first instruction of the interrupt service routine is executed. Interrupts are not recognized at the instruction boundary after any instruction that clears I (CLI or TAP). This ensures that the next instruction after a CLI or TAP will always be executed without the possibility of an intervening interrupt, provided I was set. 0 Interrupts enabled 1 Interrupts disabled
2 N	 Negative Flag — The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result. Simply loading or storing an 8-bit or 16-bit value causes N to be set if the most significant bit of the loaded or stored value was 1. 0 Non-negative result 1 Negative result
1 Z	 Zero Flag — The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of 0x00 or 0x0000. Simply loading or storing an 8-bit or 16-bit value causes Z to be set if the loaded or stored value was all 0s. 0 Non-zero result 1 Zero result
0 C	 Carry/Borrow Flag — The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag. 0 No carry out of bit 7 1 Carry out of bit 7



7.6 HCS08 Instruction Set Summary

Table 7-2 provides a summary of the HCS08 instruction set in all possible addressing modes. The table shows operand construction, execution time in internal bus clock cycles, and cycle-by-cycle details for each addressing mode variation of each instruction.

Source	Operation	dress lode	Object Code	rcles	Cyc-by-Cyc	Affect on CCR	
		Ρq Ad		ටි	Details	V 11 H	INZC
ADC #opr8i ADC opr8a ADC opr16a ADC oprx16,X ADC oprx8,X ADC ,X ADC oprx16,SP ADC oprx8,SP	Add with Carry A \leftarrow (A) + (M) + (C)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A9 ii B9 dd C9 hh 11 D9 ee ff E9 ff F9 9E D9 ee ff 9E E9 ff	2 3 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	\$11\$	- \$ \$ \$
ADD #opr8i ADD opr8a ADD opr16a ADD oprx16,X ADD oprx8,X ADD ,X ADD oprx16,SP ADD oprx8,SP	Add without Carry A \leftarrow (A) + (M)	IMM DIR EXT IX2 IX1 IX SP2 SP1	AB ii BB dd CB hh 11 DB ee ff EB ff FB 9E DB ee ff 9E EB ff	2 3 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	\$11\$	- \$ \$ \$
AIS #opr8i	Add Immediate Value (Signed) to Stack Pointer $SP \leftarrow (SP) + (M)$	ІММ	A7 ii	2	qq	- 1 1 -	
AIX #opr8i	Add Immediate Value (Signed) to Index Register (H:X) H:X \leftarrow (H:X) + (M)	ІММ	AF ii	2	qq	- 1 1 -	
AND #opr8i AND opr8a AND opr16a AND oprx16,X AND oprx8,X AND ,X AND oprx16,SP AND oprx8,SP	Logical AND A ← (A) & (M)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A4 ii B4 dd C4 hh ll D4 ee ff E4 ff F4 9E D4 ee ff 9E E4 ff	2 3 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	011-	- \$ \$ -
ASL opr8a ASLA ASLX ASL oprx8,X ASL ,X ASL oprx8,SP	Arithmetic Shift Left C = 0 b7 b0 (Same as LSL)	DIR INH INH IX1 IX SP1	38 dd 48 58 68 ff 78 9E 68 ff	5 1 1 5 4 6	rfwpp p rfwpp rfwp prfwpp	↓ 1 1 -	- \$ \$ \$
ASR opr8a ASRA ASRX ASR oprx8,X ASR ,X ASR oprx8,SP	Arithmetic Shift Right	DIR INH INH IX1 IX SP1	37 dd 47 57 67 ff 77 9E 67 ff	5 1 1 5 4 6	rfwpp p rfwpp rfwp prfwpp	↓ 1 1 -	- ↓ ↓ ↓

Table 7-2. Instruction Set Summary (Sheet 1 of 9)



Source	Operation	dress ode	Object Code	rcles	Cyc-by-Cyc	Affect on CCR		
		β Ad		ට	Details	V 1 1 H	INZC	
RSP	Reset Stack Pointer (Low Byte) SPL ← \$FF (High Byte Not Affected)	INH	9C	1	p	- 1 1 -		
RTC	Return from CALL	INH	8D	7	uuufppp	- 1 1 -		
RTI	Return from Interrupt SP ← (SP) + \$0001; Pull (CCR) SP ← (SP) + \$0001; Pull (A) SP ← (SP) + \$0001; Pull (X) SP ← (SP) + \$0001; Pull (PCH) SP ← (SP) + \$0001; Pull (PCL)	INH	80	9	uuuuufppp	↓11↓	↓↓↓↓	
RTS	Return from Subroutine SP \leftarrow SP + \$0001; Pull (PCH) SP \leftarrow SP + \$0001; Pull (PCL)	INH	81	5	ufppp	- 1 1 -		
SBC #opr8i SBC opr8a SBC opr16a SBC oprx16,X SBC oprx8,X SBC ,X SBC oprx16,SP SBC oprx8,SP	Subtract with Carry A \leftarrow (A) – (M) – (C)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A2 ii B2 dd C2 hh ll D2 ee ff E2 ff F2 9E D2 ee ff 9E E2 ff	2 3 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	↓11-	- \$ \$ \$	
SEC	Set Carry Bit $(C \leftarrow 1)$	INH	99	1	p	- 1 1 -	1	
SEI	Set Interrupt Mask Bit $(I \leftarrow 1)$	INH	9в	1	q	- 1 1 -	1 – – –	
STA opr8a STA opr16a STA oprx16,X STA oprx8,X STA ,X STA oprx16,SP STA oprx8,SP	Store Accumulator in Memory $M \leftarrow (A)$	DIR EXT IX2 IX1 IX SP2 SP1	B7 dd C7 hh 11 D7 ee ff E7 ff F7 9E D7 ee ff 9E E7 ff	3 4 3 2 5 4	MDD bMDD MDD MDD MDD MDD MDD MDD MDD MDD	011-	- \$ \$ -	
STHX opr8a STHX opr16a STHX oprx8,SP	Store H:X (Index Reg.) (M:M + \$0001) ← (H:X)	DIR EXT SP1	35 dd 96 hh 11 9E FF ff	4 5 5	adamab bamab bamab	011-	- \$ \$ -	
STOP	Enable Interrupts: Stop Processing Refer to MCU Documentation I bit \leftarrow 0; Stop Processing	INH	8E	2	fp	- 1 1 -	0	
STX opr8a STX opr16a STX oprx16,X STX oprx8,X STX ,X STX oprx16,SP STX oprx8,SP	Store X (Low 8 Bits of Index Register) in Memory $M \leftarrow (X)$	DIR EXT IX2 IX1 IX SP2 SP1	BF dd CF hh ll DF ee ff EF ff FF 9E DF ee ff 9E EF ff	3 4 3 2 5 4	bmbb bmbb bmbb bmbb bmbb	011-	- \$ \$ -	

Table 7-2. Instruction	Set	Summary	(Sheet 7	of 9))
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Chapter 8 Multi-Purpose Clock Generator (S08MCGV2)

8.1.2 Modes of Operation

There are several modes of operation for the MCG:

- FLL Engaged Internal (FEI)
- FLL Engaged External (FEE)
- FLL Bypassed Internal (FBI)
- FLL Bypassed External (FBE)
- PLL Engaged External (PEE)
- PLL Bypassed External (PBE)
- Bypassed Low Power Internal (BLPI)
- Bypassed Low Power External (BLPE)
- Stop

For details see Section 8.4.1, "Operational Modes.

8.2 External Signal Description

There are no MCG signals that connect off chip.



Chapter 8 Multi-Purpose Clock Generator (S08MCGV2)

factor, as selected by the DRS and DMX32 bits, times the internal reference frequency. The MCGLCLK is derived from the FLL and the PLL is disabled in a low power state.

8.4.1.4 FLL Bypassed External (FBE)

In FLL bypassed external (FBE) mode, the MCGOUT clock is derived from the external reference clock and the FLL is operational but its output clock is not used. This mode is useful to allow the FLL to acquire its target frequency while the MCGOUT clock is driven from the external reference clock.

The FLL bypassed external mode is entered when all the following conditions occur:

- CLKS bits are written to 10
- IREFS bit is written to 0
- PLLS bit is written to 0
- RDIV bits are written to divide reference clock to be within the range of 31.25 kHz to 39.0625 kHz
- LP bit is written to 0

In FLL bypassed external mode, the MCGOUT clock is derived from the external reference clock. The external reference clock which is enabled can be an external crystal/resonator or it can be another external clock source. The FLL clock is controlled by the external reference clock, and the FLL clock frequency locks to a multiplication factor, as selected by the DRS and DMX32 bits, times the external reference frequency, as selected by the RDIV, RANGE and DIV32 bits. The MCGLCLK is derived from the FLL and the PLL is disabled in a low power state.

8.4.1.5 PLL Engaged External (PEE)

The PLL engaged external (PEE) mode is entered when all the following conditions occur:

- CLKS bits are written to 00
- IREFS bit is written to 0
- PLLS bit is written to 1
- RDIV bits are written to divide reference clock to be within the range of 1 MHz to 2 MHz

In PLL engaged external mode, the MCGOUT clock is derived from the PLL clock which is controlled by the external reference clock. The external reference clock which is enabled can be an external crystal/resonator or it can be another external clock source The PLL clock frequency locks to a multiplication factor, as selected by the VDIV bits, times the external reference frequency, as selected by the RDIV, RANGE and DIV32 bits. If BDM is enabled then the MCGLCLK is derived from the DCO (open-loop mode) divided by two. If BDM is not enabled then the FLL is disabled in a low power state.

In this mode, the DRST bit reads 0 regardless of whether the DRS bit is set to 1 or 0.



Chapter 11 Inter-Integrated Circuit (S08IICV2)



NOTES:

1. If general call is enabled, a check must be done to determine whether the received address was a general call address (0x00). If the received address was a general call address, then the general call must be handled by user software.

2. When 10-bit addressing is used to address a slave, the slave sees an interrupt following the first byte of the extended address. User software must ensure that for this interrupt, the contents of IICD are ignored and not treated as a valid data transfer

Figure 11-12. Typical IIC Interrupt Routine

MC9S08DZ128 Series Data Sheet, Rev. 1



Chapter 12 Freescale's Controller Area Network (S08MSCANV1)



Figure 12-3. CAN System

12.3 Register Definition

This section describes in detail all the registers and register bits in the MSCAN module. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order. All bits of all registers in this module are completely synchronous to internal clocks during a register read.

12.3.1 MSCAN Control Register 0 (CANCTL0)

The CANCTL0 register provides various control bits of the MSCAN module as described below.



Figure 12-4. MSCAN Control Register 0 (CANCTL0)

NOTE

The CANCTL0 register, except WUPE, INITRQ, and SLPRQ, is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Read: Anytime

Write: Anytime when out of initialization mode; exceptions are read-only RXACT and SYNCH, RXFRM (which is set by the module only), and INITRQ (which is also writable in initialization mode).

MC9S08DZ128 Series Data Sheet, Rev. 1



Chapter 13 Serial Peripheral Interface (S08SPIV3)



15.3.2 RTC Counter Register (RTCCNT)

RTCCNT is the read-only value of the current RTC count of the 8-bit counter.



Figure 15-4. RTC Counter Register (RTCCNT)

Table 15-4. RTCCNT Field Descriptions

Field	Description
7:0 RTCCNT	RTC Count. These eight read-only bits contain the current value of the 8-bit counter. Writes have no effect to this register. Reset, writing to RTCMOD, or writing different values to RTCLKS and RTCPS clear the count to 0x00.

15.3.3 RTC Modulo Register (RTCMOD)



 Table 15-5. RTCMOD Field Descriptions

Field	Description
7:0 RTCMOD	RTC Modulo. These eight read/write bits contain the modulo value used to reset the count to 0x00 upon a compare match and set the RTIF status bit. A value of 0x00 sets the RTIF bit on each rising edge of the prescaler output. Writing to RTCMOD resets the prescaler and the RTCCNT counters to 0x00. Reset sets the modulo to 0x00.

15.4 Functional Description

The RTC is composed of a main 8-bit up-counter with an 8-bit modulo register, a clock source selector, and a prescaler block with binary-based and decimal-based selectable values. The module also contains software selectable interrupt logic.

After any MCU reset, the counter is stopped and reset to 0x00, the modulus register is set to 0x00, and the prescaler is off. The 1-kHz internal oscillator clock is selected as the default clock source. To start the prescaler, write any value other than zero to the prescaler select bits (RTCPS).

Three clock sources are software selectable: the low power oscillator clock (LPO), the external clock (ERCLK), and the internal clock (IRCLK). The RTC clock select bits (RTCLKS) select the desired clock source. If a different value is written to RTCLKS, the prescaler and RTCCNT counters are reset to 0x00.



Chapter 15 Real-Time Counter (S08RTCV1)

CLKSB:CLKSA	TPM Clock Source to Prescaler Input
00	No clock selected (TPM counter disabled)
01	Bus rate clock
10	Fixed system clock
11	External source

Table 16-7. TPM Clock Source Selection

The bus rate clock is the main system bus clock for the MCU. This clock source requires no synchronization because it is the clock that is used for all internal MCU activities including operation of the CPU and buses.

In MCUs that have no PLL and FLL or the PLL and FLL are not engaged, the fixed system clock source is the same as the bus-rate-clock source, and it does not go through a synchronizer. When a PLL or FLL is present and engaged, a synchronizer is required between the crystal divided-by two clock source and the timer counter so counter transitions will be properly aligned to bus-clock transitions. A synchronizer will be used at chip level to synchronize the crystal-related source clock to the bus clock.

The external clock source may be connected to any TPM channel pin. This clock source always has to pass through a synchronizer to assure that counter transitions are properly aligned to bus clock transitions. The bus-rate clock drives the synchronizer; therefore, to meet Nyquist criteria even with jitter, the frequency of the external clock source must not be faster than the bus rate divided-by four. With ideal clocks the external clock can be as fast as bus clock divided by four.

When the external clock source shares the TPM channel pin, this pin should not be used for other channel timing functions. For example, it would be ambiguous to configure channel 0 for input capture when the TPM channel 0 pin was also being used as the timer external clock source. (It is the user's responsibility to avoid such settings.) The TPM channel could still be used in output compare mode for software timing functions (pin controls set not to affect the TPM channel pin).

16.4.1.2 Counter Overflow and Modulo Reset

An interrupt flag and enable are associated with the 16-bit main counter. The flag (TOF) is a software-accessible indication that the timer counter has overflowed. The enable signal selects between software polling (TOIE=0) where no hardware interrupt is generated, or interrupt-driven operation (TOIE=1) where a static hardware interrupt is generated whenever the TOF flag is equal to one.

The conditions causing TOF to become set depend on whether the TPM is configured for center-aligned PWM (CPWMS=1). In the simplest mode, there is no modulus limit and the TPM is not in CPWMS=1 mode. In this case, the 16-bit timer counter counts from 0x0000 through 0xFFFF and overflows to 0x0000 on the next counting clock. TOF becomes set at the transition from 0xFFFF to 0x0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to 0x0000. When the TPM is in center-aligned PWM mode (CPWMS=1), the TOF flag gets set as the counter changes direction at the end of the count value set in the modulus register (that is, at the transition from the value set in the modulus register to the next lower count value). This corresponds to the end of a PWM period (the 0x0000 count value corresponds to the center of a period).



Command Mnemonic	Active BDM/ Non-intrusive	Coding Structure	Description
SYNC	Non-intrusive	n/a ¹	Request a timed reference pulse to determine target BDC communication speed
ACK_ENABLE	Non-intrusive	D5/d	Enable acknowledge protocol. Refer to Freescale document order no. HCS08RMv1/D.
ACK_DISABLE	Non-intrusive	D6/d	Disable acknowledge protocol. Refer to Freescale document order no. HCS08RMv1/D.
BACKGROUND	Non-intrusive	90/d	Enter active background mode if enabled (ignore if ENBDM bit equals 0)
READ_STATUS	Non-intrusive	E4/SS	Read BDC status from BDCSCR
WRITE_CONTROL	Non-intrusive	C4/CC	Write BDC controls in BDCSCR
READ_BYTE	Non-intrusive	E0/AAAA/d/RD	Read a byte from target memory
READ_BYTE_WS	Non-intrusive	E1/AAAA/d/SS/RD	Read a byte and report status
READ_LAST	Non-intrusive	E8/SS/RD	Re-read byte from address just read and report status
WRITE_BYTE	Non-intrusive	C0/AAAA/WD/d	Write a byte to target memory
WRITE_BYTE_WS	Non-intrusive	C1/AAAA/WD/d/SS	Write a byte and report status
READ_BKPT	Non-intrusive	E2/RBKP	Read BDCBKPT breakpoint register
WRITE_BKPT	Non-intrusive	C2/WBKP	Write BDCBKPT breakpoint register
GO	Active BDM	08/d	Go to execute the user application program starting at the address currently in the PC
TRACE1	Active BDM	10/d	Trace 1 user instruction at the address in the PC, then return to active background mode
TAGGO	Active BDM	18/d	Same as GO but enable external tagging (HCS08 devices have no external tagging pin)
READ_A	Active BDM	68/d/RD	Read accumulator (A)
READ_CCR	Active BDM	69/d/RD	Read condition code register (CCR)
READ_PC	Active BDM	6B/d/RD16	Read program counter (PC)
READ_HX	Active BDM	6C/d/RD16	Read H and X register pair (H:X)
READ_SP	Active BDM	6F/d/RD16	Read stack pointer (SP)
READ_NEXT	Active BDM	70/d/RD	Increment H:X by one then read memory byte located at H:X
READ_NEXT_WS	Active BDM	71/d/SS/RD	Increment H:X by one then read memory byte located at H:X. Report status and data.
WRITE_A	Active BDM	48/WD/d	Write accumulator (A)
WRITE_CCR	Active BDM	49/WD/d	Write condition code register (CCR)
WRITE_PC	Active BDM	4B/WD16/d	Write program counter (PC)
WRITE_HX	Active BDM	4C/WD16/d	Write H and X register pair (H:X)
WRITE_SP	Active BDM	4F/WD16/d	Write stack pointer (SP)
WRITE_NEXT	Active BDM	50/WD/d	Increment H:X by one, then write memory byte located at H:X
WRITE_NEXT_WS	Active BDM	51/WD/d/SS	Increment H:X by one, then write memory byte located at H:X. Also report status.

Table 17-1. BDC Command Summary

¹ The SYNC command is a special operation that does not have a command code.



18.3.3 Register Descriptions

This section consists of the DBG register descriptions in address order.

Note: For all registers below, consider: U = Unchanged, bit maintain its value after reset.

18.3.3.1 Debug Comparator A High Register (DBGCAH)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
POR or non- end-run	1	1	1	1	1	1	1	1
Reset end-run ¹	U	U	U	U	U	U	U	U

Figure 18-2. Debug Comparator A High Register (DBGCAH)

¹ In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, the bits in this register do not change after reset.

Table 18-3. DBGCAH Field Descriptions

Field	Description
Bits 15–8	 Comparator A High Compare Bits — The Comparator A High compare bits control whether Comparator A will compare the address bus bits [15:8] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0 1 Compare corresponding address bit to a logic 1

18.3.3.2 Debug Comparator A Low Register (DBGCAL)

7 6 5 4 3 2 1 0 R Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 W POR or non-1 1 1 1 1 1 1 0 end-run Reset U U U U U U U U end-run¹

Figure 18-3. Debug Comparator A Low Register (DBGCAL)

¹ In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, the bits in this register do not change after reset.

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Module Base + 0x0001



Table 18-9. DBGFH Field Descriptions

Field	Description
Bits 15–8	FIFO High Data Bits — The FIFO High data bits provide access to bits [15:8] of data in the FIFO. This register is not used in event only modes and will read a \$00 for valid FIFO words.

18.3.3.8 Debug FIFO Low Register (DBGFL)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
w								
POR or non- end-run	0	0	0	0	0	0	0	0
Reset end-run ¹	U	U	U	U	U	U	U	U

= Unimplemented or Reserved

Figure 18-9. Debug FIFO Low Register (DBGFL)

¹ In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, the bits in this register do not change after reset.

Table 18-10. DBGFL Field Descriptions

Field	Description
Bits 7–0	FIFO Low Data Bits — The FIFO Low data bits contain the least significant byte of data in the FIFO. When reading FIFO words, read DBGFX and DBGFH before reading DBGFL because reading DBGFL causes the FIFO pointers to advance to the next FIFO location. In event-only modes, there is no useful information in DBGFX and DBGFH so it is not necessary to read them before reading DBGFL.



Appendix A Electrical Characteristics



Figure A-8. ADC Input Impedance Equivalency Diagram