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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t635-gm

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Figure 1.1. C8051T630/1/2/3/4/5 Block Diagram



## SFR Definition 6.2. ADC0H: ADC0 Data Word MSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0H[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBE

Bit	Name	Function
7:0	ADC0H[7:0]	ADC0 Data Word High-Order Bits.
		For AD0LJST = 0: Bits 7–2 will read 000000b. Bits 1–0 are the upper 2 bits of the 10- bit ADC0 Data Word.
		For AD0LJST = 1: Bits 7–0 are the most-significant bits of the 10-bit ADC0 Data Word.
		<b>Note:</b> In 8-bit mode AD0LJST is ignored, and ADC0H holds the 8-bit data word.

# SFR Definition 6.3. ADC0L: ADC0 Data Word LSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0L[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBD

Bit	Name	Function
7:0	ADC0L[7:0]	ADC0 Data Word Low-Order Bits.
		For AD0LJST = 0: Bits $7-0$ are the lower 8 bits of the 10-bit Data Word.
		For AD0LJST = 1: Bits 7–6 are the lower 2 bits of the 10-bit Data Word. Bits 5–0 will read 000000b.
		<b>Note:</b> In 8-bit mode AD0LJST is ignored, and ADC0L will read back 00000000b.



# SFR Definition 13.1. EMI0CN: External Memory Interface Control

Bit	7	6	5	4	3	2	1	0
Name								PGSEL
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAA

Bit	Name	Function
7:1	Unused	Unused. Read = 0000000b; Write = Don't Care
0	PGSEL	XRAM Page Select.
		The EMI0CN register provides the high byte of the 16-bit external data memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM. Since the upper (unused) bits of the register are always zero, the PGSEL determines which page of XRAM is accessed. For Example: If EMI0CN = 0x01, addresses 0x0100 through 0x01FF will be accessed.



## Table 14.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
POMAT	0xFD	Port 0 Match Configuration	119
POMDIN	0xF1	Port 0 Input Mode Configuration	122
P0MDOUT	0xA4	Port 0 Output Mode Configuration	122
P0SKIP	0xD4	Port 0 Skip	123
P1	0x90	Port 1 Latch	123
P1MASK	0xEE	Port 1Mask Configuration	120
P1MAT	0xED	Port 1 Match Configuration	120
P1MDIN	0xF2	Port 1 Input Mode Configuration	124
P1MDOUT	0xA5	Port 1 Output Mode Configuration	124
P1SKIP	0xD5	Port 1 Skip	125
P2	0xA0	Port 2 Latch	125
P2MDOUT	0xA6	Port 2 Output Mode Configuration	126
PCA0CN	0xD8	PCA Control	204
PCA0CPH0	0xFC	PCA Capture 0 High	209
PCA0CPH1	0xEA	PCA Capture 1 High	209
PCA0CPH2	0xEC	PCA Capture 2 High	209
PCA0CPL0	0xFB	PCA Capture 0 Low	209
PCA0CPL1	0xE9	PCA Capture 1 Low	209
PCA0CPL2	0xEB	PCA Capture 2 Low	209
PCA0CPM0	0xDA	PCA Module 0 Mode Register	207
PCA0CPM1	0xDB	PCA Module 1 Mode Register	207
PCA0CPM2	0xDC	PCA Module 2 Mode Register	207
PCA0H	0xFA	PCA Counter High	208
PCA0L	0xF9	PCA Counter Low	208
PCA0MD	0xD9	PCA Mode	205
PCA0PWM	0xF7	PCA PWM Configuration	206
PCON	0x87	Power Control	94
PSW	0xD0	Program Status Word	71
REF0CN	0xD1	Voltage Reference Control	54
REG0CN	0xC7	Voltage Regulator Control	56
RSTSRC	0xEF	Reset Source Configuration/Status	100
SBUF0	0x99	UART0 Data Buffer	154
SCON0	0x98	UART0 Control	153
SMB0ADM	0xE7	SMBus Slave Address Mask	138



# 15. Interrupts

The C8051T630/1/2/3/4/5 includes an extended interrupt system supporting a total of 14 interrupt sources with two priority levels. The allocation of interrupt sources between on-chip peripherals and external input pins varies according to the specific version of the device. Each interrupt source has one or more associated interrupt-pending flag(s) located in an SFR. When a peripheral or external source meets a valid interrupt condition, the associated interrupt-pending flag is set to logic 1.

If interrupts are enabled for the source, an interrupt request is generated when the interrupt-pending flag is set. As soon as execution of the current instruction is complete, the CPU generates an LCALL to a predetermined address to begin execution of an interrupt service routine (ISR). Each ISR must end with an RETI instruction, which returns program execution to the next instruction that would have been executed if the interrupt request had not occurred. If interrupts are not enabled, the interrupt-pending flag is ignored by the hardware and program execution continues as normal. (The interrupt-pending flag is set to logic 1 regard-less of the interrupt's enable/disable state.)

Each interrupt source can be individually enabled or disabled through the use of an associated interrupt enable bit in an SFR (IE–EIE1). However, interrupts must first be globally enabled by setting the EA bit (IE.7) to logic 1 before the individual interrupt enables are recognized. Setting the EA bit to logic 0 disables all interrupt sources regardless of the individual interrupt-enable settings.

**Note:** Any instruction that clears a bit to disable an interrupt should be immediately followed by an instruction that has two or more opcode bytes. Using EA (global interrupt enable) as an example:

```
// in 'C':
EA = 0; // clear EA bit.
EA = 0; // this is a dummy instruction with two-byte opcode.
; in assembly:
CLR EA ; clear EA bit.
CLR EA ; this is a dummy instruction with two-byte opcode.
```

For example, if an interrupt is posted during the execution phase of a "CLR EA" opcode (or any instruction which clears a bit to disable an interrupt source), and the instruction is followed by a single-cycle instruction, the interrupt may be taken. However, a read of the enable bit will return a '0' inside the interrupt service routine. When the bit-clearing opcode is followed by a multi-cycle instruction, the interrupt will not be taken.

Some interrupt-pending flags are automatically cleared by the hardware when the CPU vectors to the ISR. However, most are not cleared by the hardware and must be cleared by software before returning from the ISR. If an interrupt-pending flag remains set after the CPU completes the return-from-interrupt (RETI) instruction, a new interrupt request will be generated immediately and the CPU will re-enter the ISR after the completion of the next instruction.



### 18.1. Power-On Reset

During power-up, the device is held in a reset state and the  $\overline{RST}$  pin is driven low until V<sub>DD</sub> settles above V<sub>RST</sub>. A delay occurs before the device is released from reset; the delay decreases as the V<sub>DD</sub> ramp time increases (V<sub>DD</sub> ramp time is defined as how fast V<sub>DD</sub> ramps from 0 V to V<sub>RST</sub>). Figure 18.2. plots the power-on and V<sub>DD</sub> monitor event timing. The maximum V<sub>DD</sub> ramp time is 1 ms; slower ramp times may cause the device to be released from reset before V<sub>DD</sub> reaches the V<sub>RST</sub> level. For ramp times less than 1 ms, the power-on reset delay (T<sub>PORDelay</sub>) is typically less than 0.3 ms.

On exit from a power-on or  $V_{DD}$  monitor reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V<sub>DD</sub> monitor is enabled following a power-on reset.



Figure 18.2. Power-On and V<sub>DD</sub> Monitor Reset Timing



## SFR Definition 18.2. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name		MEMERR	CORSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Туре	R	R	R/W	R/W	R	R/W	R/W	R
Reset	0	Varies						

SFR Address = 0xEF

Bit	Name	Description	Write	Read
7	Unused	Unused.	Don't care.	0
6	MEMERR	EPROM Error Reset Flag.	N/A	Set to 1 if EPROM read/write error caused the last reset.
5	CORSEF	Comparator0 Reset Enable and Flag.	Writing a 1 enables Comparator0 as a reset source (active-low).	Set to 1 if Comparator0 caused the last reset.
4	SWRSF	Software Reset Force and Flag.	Writing a 1 forces a sys- tem reset.	Set to 1 if last reset was caused by a write to SWRSF.
3	WDTRSF	Watchdog Timer Reset Flag.	N/A	Set to 1 if Watchdog Timer overflow caused the last reset.
2	MCDRSF	Missing Clock Detector Enable and Flag.	Writing a 1 enables the Missing Clock Detector. The MCD triggers a reset if a missing clock condition is detected.	Set to 1 if Missing Clock Detector timeout caused the last reset.
1	PORSF	Power-On/V <sub>DD</sub> Monitor Reset Flag, and V <sub>DD</sub> monitor Reset Enable.	Writing a 1 enables the $V_{DD}$ monitor as a reset source. Writing 1 to this bit before the $V_{DD}$ monitor is enabled and stabilized may cause a system reset.	Set to 1 anytime a power- on or V <sub>DD</sub> monitor reset occurs. When set to 1 all other RSTSRC flags are inde- terminate.
0	PINRSF	HW Pin Reset Flag.	N/A	Set to 1 if RST pin caused the last reset.
Note:	Do not use	read-modify-write operations on this	s register	



# SFR Definition 20.1. XBR0: Port I/O Crossbar Register 0

Bit	7	6	5	4	3	2	1	0
Name			CP0AE	CP0E	SYSCKE	SMB0E	SPI0E	URT0E
Туре	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE1

Bit	Name	Function
7:6	Unused	Unused. Read = 00b; Write = Don't Care.
5	CP0AE	Comparator0 Asynchronous Output Enable.
		0: Asynchronous CP0 unavailable at Port pin.
		1: Asynchronous CP0 routed to Port pin.
4	CP0E	Comparator0 Output Enable.
		0: CP0 unavailable at Port pin.
		1: CP0 routed to Port pin.
3	SYSCKE	/SYSCLK Output Enable.
		0: /SYSCLK unavailable at Port pin.
		1: /SYSCLK output routed to Port pin.
2	SMB0E	SMBus I/O Enable.
		0: SMBus I/O unavailable at Port pins.
		1: SMBus I/O routed to Port pins.
1	SPI0E	SPI I/O Enable.
		0: SPI I/O unavailable at Port pins.
		1: SPI I/O routed to Port pins. Note that the SPI can be assigned either 3 or 4 GPIO
		pins.
U	URIUE	UART I/O Output Enable.
		0: UART I/O unavailable at Port pin.
		1: UART TX0, RX0 routed to Port pins P0.4 and P0.5.



# SFR Definition 21.1. SMB0CF: SMBus Clock/Configuration

Bit	7	6	5	4	3	2	1	0
Name	ENSMB	INH	BUSY	EXTHOLD	SMBTOE	SMBFTE	SMBC	:S[1:0]
Туре	R/W	R/W	R	R/W	R/W	R/W	R/	W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC1

Bit	Name	Function
7	ENSMB	SMBus Enable.
		This bit enables the SMBus interface when set to 1. When enabled, the interface constantly monitors the SDA and SCL pins.
6	INH	SMBus Slave Inhibit.
		When this bit is set to logic 1, the SMBus does not generate an interrupt when slave events occur. This effectively removes the SMBus slave from the bus. Master Mode interrupts are not affected.
5	BUSY	SMBus Busy Indicator.
		This bit is set to logic 1 by hardware when a transfer is in progress. It is cleared to logic 0 when a STOP or free-timeout is sensed.
4	EXTHOLD	SMBus Setup and Hold Time Extension Enable.
		This bit controls the SDA setup and hold times according to Table 21.2.
		0: SDA Extended Setup and Hold Times disabled.
3	SMBTOF	SMBus SCI Timeout Detection Enable
		This bit enables SCL low timeout detection. If set to logic 1, the SMBus forces Timer 3 to reload while SCL is high and allows Timer 3 to count when SCL goes low. If Timer 3 is configured to Split Mode, only the High Byte of the timer is held in reload while SCL is high. Timer 3 should be programmed to generate interrupts at 25 ms, and the Timer 3 interrupt service routine should reset SMBus communication.
2	SMBFTE	SMBus Free Timeout Detection Enable.
		When this bit is set to logic 1, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods.
1:0	SMBCS[1:0]	SMBus Clock Source Selection.
		These two bits select the SMBus clock source, which is used to generate the SMBus bit rate. The selected device should be configured according to Equation 21.1. 00: Timer 0 Overflow 01: Timer 1 Overflow 10: Timer 2 High Byte Overflow 11: Timer 2 Low Byte Overflow



#### 22.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB80 (SCON0.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB80 (SCON0.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: (1) RI0 must be logic 0, and (2) if MCE0 is logic 1, the 9th bit must be logic 1 (when MCE0 is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF0, the ninth bit is stored in RB80, and the RI0 flag is set to 1. If the above conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set to 1. A UART0 interrupt will occur if enabled when either TI0 or RI0 is set to 1.



Figure 22.5. 9-Bit UART Timing Diagram



## SFR Definition 24.1. CKCON: Clock Control

Bit	7	6	5	4	3	2	1	0
Name	ТЗМН	T3ML	T2MH	T2ML	T1M	ТОМ	SCA	[1:0]
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/	W
Reset	0	0	0	0	0	0	0	0

#### SFR Address = 0x8E

Bit	Name	Function
7	ТЗМН	<b>Timer 3 High Byte Clock Select.</b> Selects the clock supplied to the Timer 3 high byte (split 8-bit timer mode only). 0: Timer 3 high byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 high byte uses the system clock.
6	T3ML	Timer 3 Low Byte Clock Select
		Selects the clock supplied to Timer 3. Selects the clock supplied to the lower 8-bit timer in split 8-bit timer mode. 0: Timer 3 low byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 low byte uses the system clock.
5	T2MH	Timer 2 High Byte Clock Select.
		Selects the clock supplied to the Timer 2 high byte (split 8-bit timer mode only). 0: Timer 2 high byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 high byte uses the system clock.
4	T2ML	Timer 2 Low Byte Clock Select.
		<ul> <li>Selects the clock supplied to Timer 2. If Timer 2 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer.</li> <li>0: Timer 2 low byte uses the clock defined by the T2XCLK bit in TMR2CN.</li> <li>1: Timer 2 low byte uses the system clock.</li> </ul>
3	T1	Timer 1 Clock Select.
		Selects the clock source supplied to Timer 1. Ignored when C/T1 is set to 1. 0: Timer 1 uses the clock defined by the prescale bits SCA[1:0]. 1: Timer 1 uses the system clock.
2	Т0	Timer 0 Clock Select.
		Selects the clock source supplied to Timer 0. Ignored when C/T0 is set to 1. 0: Counter/Timer 0 uses the clock defined by the prescale bits SCA[1:0]. 1: Counter/Timer 0 uses the system clock.
1:0	SCA[1:0]	Timer 0/1 Prescale Bits.
		These bits control the Timer 0/1 Clock Prescaler: 00: System clock divided by 12 01: System clock divided by 4 10: System clock divided by 48 11: External clock divided by 8 (synchronized with the system clock)



## SFR Definition 24.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	9			TH0	[7:0]			
Туре	Type R/W							
Rese	<b>t</b> 0	0	0	0	0	0	0	0
SFR A	ddress = 0x8	С						
Bit	Name		Function					
7:0	TH0[7:0]	Timer 0 Hig	Timer 0 High Byte.					
		The TH0 re	gister is the l	high byte of	the 16-bit Tir	mer 0.		

## SFR Definition 24.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH1[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0
SFR Address = 0x8D								

Bit	Name	Function
7:0	TH1[7:0]	Timer 1 High Byte.
		The TH1 register is the high byte of the 16-bit Timer 1.



## SFR Definition 24.13. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3	T3XCI	_K[1:0]
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/	W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91

Bit	Name	Function
7	TF3H	<b>Timer 3 High Byte Overflow Flag.</b> Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit
		mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	Timer 3 Low Byte Overflow Flag.
		Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	Timer 3 Low Byte Interrupt Enable.
		When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	Timer 3 Low-Frequency Oscillator Capture Enable.
		When set to 1, this bit enables Timer 3 Low-Frequency Oscillator Capture Mode. If TF3CEN is set and Timer 3 interrupts are enabled, an interrupt will be generated on a falling edge of the low-frequency oscillator output, and the current 16-bit timer value in TMR3H:TMR3L will be copied to TMR3RLH:TMR3RLL.
3	T3SPLIT	Timer 3 Split Mode Enable.
		When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload.
		0: Timer 3 operates in 16-bit auto-reload mode.
2	TR3	Timer 3 Bun Control
_	1110	Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables
		TMR3H only; TMR3L is always enabled in split mode.
1:0	T3XCLK[1:0]	Timer 3 External Clock Select.
		This bit selects the "external" clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 00: System clock divided by 12.
		<ul> <li>01: External clock divided by 8 (synchronized with SYSCLK when not in suspend).</li> <li>10: Reserved.</li> <li>11: Internal LFO/8 (synchronized with SYSCLK when not in suspend).</li> </ul>



#### 25.3.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

**Important Note About Capture/Compare Registers**: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.



Figure 25.5. PCA Software Timer Mode Diagram



#### 25.3.5.1. 8-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 8-bit PWM mode is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 25.8). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the module's capture/compare high byte (PCA0CPHn) without software intervention. Setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to 00b enables 8-Bit Pulse Width Modulator mode. If the MATn bit is set to 1, the CCFn flag for the module will be set each time an 8-bit comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 256 PCA clock cycles. The duty cycle for 8-Bit PWM Mode is given in Equation 25.2.

**Important Note About Capture/Compare Registers**: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

Duty Cycle = 
$$\frac{(256 - PCA0CPHn)}{256}$$

#### Equation 25.2. 8-Bit PWM Duty Cycle

Using Equation 25.2, the largest duty cycle is 100% (PCA0CPHn = 0), and the smallest duty cycle is 0.39% (PCA0CPHn = 0xFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.



Figure 25.8. PCA 8-Bit PWM Mode Diagram



### 25.5. Register Descriptions for PCA0

Following are detailed descriptions of the special function registers related to the operation of the PCA.

### SFR Definition 25.1. PCA0CN: PCA Control

Bit	7	6	5	4	3	2	1	0
Name	CF	CR				CCF2	CCF1	CCF0
Туре	R/W	R/W	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### SFR Address = 0xD8; Bit-Addressable

Bit	Name	Function
7	CF	PCA Counter/Timer Overflow Flag.
		Set by hardware when the PCA Counter/Timer overflows from 0xFFFF to 0x0000. When the Counter/Timer Overflow (CF) interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.
6	CR	PCA Counter/Timer Run Control.
		This bit enables/disables the PCA Counter/Timer.
		0: PCA Counter/Timer disabled.
		1: PCA Counter/Timer enabled.
5:3	Unused	Unused. Read = 000b, Write = Don't care.
2	CCF2	PCA Module 2 Capture/Compare Flag.
		This bit is set by hardware when a match or capture occurs. When the CCF2 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service rou- tine. This bit is not automatically cleared by hardware and must be cleared by software.
1	CCF1	PCA Module 1 Capture/Compare Flag.
		This bit is set by hardware when a match or capture occurs. When the CCF1 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service rou- tine. This bit is not automatically cleared by hardware and must be cleared by software.
0	CCF0	PCA Module 0 Capture/Compare Flag.
		This bit is set by hardware when a match or capture occurs. When the CCF0 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service rou- tine. This bit is not automatically cleared by hardware and must be cleared by software.



## SFR Definition 25.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0	
Name	e CIDL	WDTE	WDLCK		CPS2	CPS1	CPS0	ECF	
Туре	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Rese	t 0	1	0	0	0	0	0	0	
SFR A	ddress = 0	xD9	L		•	•	I		
Bit	Name				Function				
7	CIDL	PCA Counter	/Timer Idle	Control.					
		Specifies PCA 0: PCA contin 1: PCA operat	Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.						
6	WDTE	Watchdog Timer Enable. If this bit is set, PCA Module 2 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA Module 2 enabled as Watchdog Timer.							
5	WDLCK	Watchdog Timer Lock. This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked.							
4	Unused	Unused. Read	Unused. Read = 0b, Write = Don't care.						
3:1	CPS[2:0]	PCA Counter/Timer Pulse Select. These bits select the timebase source for the PCA counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) 11x: Reserved							
0	ECF	PCA Counter/Timer Overflow Interrupt Enable.							
		<ul> <li>This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt.</li> <li>0: Disable the CF interrupt.</li> <li>1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.</li> </ul>					ICN.7) is		
Note:	When the V contents of	VDTE bit is set to the PCA0MD reg	o 1, the other b gister, the Wat	oits in the PC	A0MD register must first be c	cannot be mo lisabled.	odified. To cha	ange the	



## C2 Register Definition 26.6. EPDAT: C2 EPROM Data

Bit	7	6	5	4	3	2	1	0
Name	EPDAT[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xBF

Bit	Name	Function
7:0	EPDAT[7:0]	C2 EPROM Data Register.
		This register is used to pass EPROM data during C2 EPROM operations.

## C2 Register Definition 26.7. EPSTAT: C2 EPROM Status

Bit	7	6	5	4	3	2	1	0
Name	WRLOCK	RDLOCK						ERROR
Туре	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xB7

Bit	Name	Function
7	WRLOCK	Write Lock Indicator.
		Set to '1' if EPADDR currently points to a write-locked address.
6	RDLOCK	Read Lock Indicator.
		Set to '1' if EPADDR currently points to a read-locked address.
5:1	Unused	Unused. Read = 00000b; Write = don't care.
0	ERROR	Error Indicator.
		Set to '1' if last EPROM read or write operation failed due to a security restriction.



# **CONTACT INFORMATION**

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