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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	23
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega48v-10aur

- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Six PWM Channels
  - 8-channel 10-bit ADC in TQFP and QFN/MLF package
    - Temperature Measurement
  - 6-channel 10-bit ADC in PDIP Package
    - Temperature Measurement
  - Two Master/Slave SPI Serial Interface
  - One Programmable Serial USART
  - One Byte-oriented 2-wire Serial Interface (Philips I^2C compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - One On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-pin PDIP, 32-lead TQFP, 28-pad QFN/MLF and 32-pad QFN/MLF
- Operating Voltage:
  - 2.7 - 5.5V for ATmega48/88/168
  - 1.8 - 5.5V for ATmega48V/88V/168V
- Temperature Range:
  - -40°C to 85°C
- Speed Grade:
  - ATmega48/88/168: 0 - 10MHz @ 2.7V - 5.5V, 0 - 20MHz @ 4.5V - 5.5V
  - ATmega48V/88V/168V: 0 - 4MHz @ 1.8V - 5.5V, 0 - 10MHz @ 2.7V - 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active Mode: 0.3mA
  - Power-down Mode: 0.1µA
  - Power-save Mode: 0.8µA (Including 32kHz RTC)

Bit 0 – C: Carry Flag

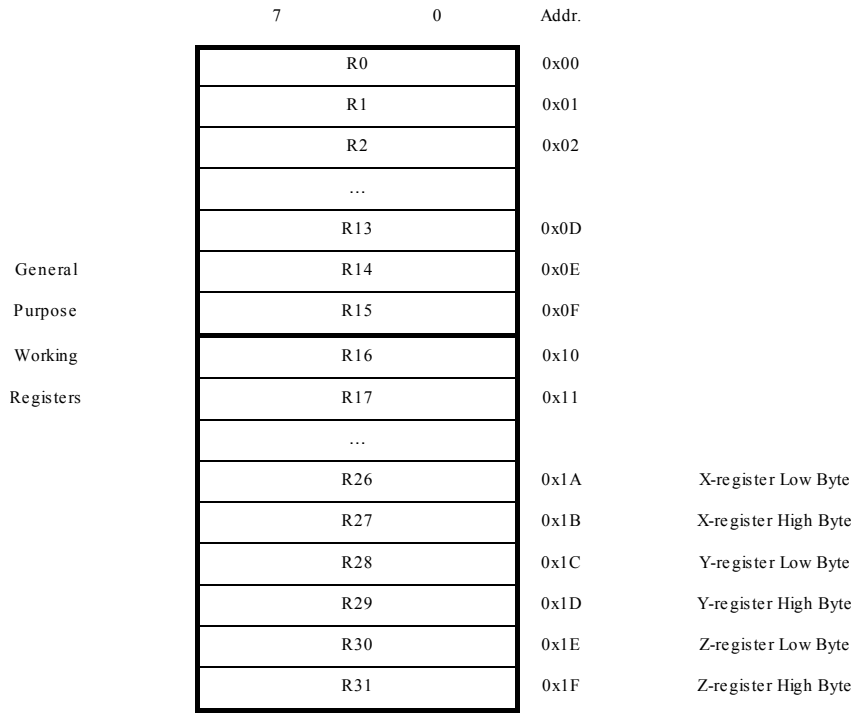
The Carry Flag C indicates a carry in an arithmetic or logic operation. See the *Instruction Set Description* for detailed information.

11.4. General Purpose Register File

The Register File is optimized for the AVR Enhanced RISC instruction set. In order to achieve the required performance and flexibility, the following input/output schemes are supported by the Register File:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Figure 11-2. AVR CPU General Purpose Working Registers



Most of the instructions operating on the Register File have direct access to all registers, and most of them are single cycle instructions. As shown in the figure, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-pointer registers can be set to index any register in the file.

11.4.1. The X-register, Y-register, and Z-register

The registers R26...R31 have some added functions to their general purpose usage. These registers are 16-bit address pointers for indirect addressing of the data space. The three indirect address registers X, Y, and Z are defined as described in the figure.

```
      rjmp     EEPROM_write
      ; Set up address (r18:r17) in address register
      out      EEARH, r18
      out      EEARL, r17
      ; Write data (r16) to Data Register
      out      EEDR,r16
      ; Write logical one to EEMPE
      sbi      EECR,EEMPE
      ; Start eeprom write by setting EEPE
      sbi      EECR,EEPE
      ret
```

C Code Example(1)

```
void EEPROM_write(unsigned int uiAddress, unsigned char ucData)
{
    /* Wait for completion of previous write */
    while(EECR & (1<<EEPE))
    ;
    /* Set up address and Data Registers */
    EEAR = uiAddress;
    EEDR = ucData;
    /* Write logical one to EEMPE */
    EECR |= (1<<EEMPE);
    /* Start eeprom write by setting EEPE */
    EECR |= (1<<EEPE);
}
```

Note: (1) Please refer to *About Code Examples*

The next code examples show assembly and C functions for reading the EEPROM. The examples assume that interrupts are controlled so that no interrupts will occur during execution of these functions.

Assembly Code Example(1)

```
EEPROM_read:
   ; Wait for completion of previous write
   sbic     EECR,EEPE
   rjmp     EEPROM_read
   ; Set up address (r18:r17) in address register
   out      EEARH, r18
   out      EEARL, r17
   ; Start eeprom read by writing EERE
   sbi      EECR,EERE
   ; Read data from Data Register
   in       r16,EEDR
   ret
```

C Code Example(1)

```
unsigned char EEPROM_read(unsigned int uiAddress)
{
    /* Wait for completion of previous write */
    while(EECR & (1<<EEPE))
    ;
    /* Set up address register */
    EEAR = uiAddress;
    /* Start eeprom read by writing EERE */
    EECR |= (1<<EERE);
    /* Return data from Data Register */
    return EEDR;
}
```

1. Refer to *About Code Examples*.

Vector No	Program Address	Source	Interrupts definition
24	0x0017	ANALOG COMP	Analog Comparator
25	0x0018	TWI	2-wire Serial Interface (I^2C)
26	0x0019	SPM READY	Store Program Memory Ready

The most typical and general program setup for the Reset and Interrupt Vector Addresses is:

```
Address   Labels    Code                        Comments
0x0000              jmp     RESET               ; Reset
0x0001              jmp     INT0                ; IRQ0
0x0002              jmp     INT1                ; IRQ1
0x0003              jmp     PCINT0              ; PCINT0
0x0004              jmp     PCINT1              ; PCINT1
0x0005              jmp     PCINT2              ; PCINT2
0x0006              jmp     WDT                 ; Watchdog Timeout
0x0007              jmp     TIM2_COMPA          ; Timer2 CompareA
0x0008              jmp     TIM2_COMPB          ; Timer2 CompareB
0x0009              jmp     TIM2_OVF            ; Timer2 Overflow
0x000A              jmp     TIM1_CAPT           ; Timer1 Capture
0x000B              jmp     TIM1_COMPA          ; Timer1 CompareA
0x000C              jmp     TIM1_COMPB          ; Timer1 CompareB
0x000C              jmp     TIM1_OVF            ; Timer1 Overflow
0x000E              jmp     TIM0_COMPA          ; Timer0 CompareA
0x000F              jmp     TIM0_COMPB          ; Timer0 CompareB
0x0010              jmp     TIM0_OVF            ; Timer0 Overflow
0x0011              jmp     SPI_STC             ; SPI Transfer Complete
0x0012              jmp     USART_RXC           ; USART RX Complete
0x0013              jmp     USART_UDRE          ; USART UDR Empty
0x0014              jmp     USART_TXC           ; USART TX Complete
0x0015              jmp     ADC                 ; ADC Conversion Complete
0x0016              jmp     EE_RDY              ; EEPROM Ready
0x0017              jmp     ANA_COMP            ; Analog Comparator
0x0018              jmp     TWI                 ; 2-wire Serial
0x0019              jmp     SPM_RDY             ; SPM Ready
;
0x001A    RESET:    ldi     r16,high(RAMEND)    ; Main program start
0x001B              out     SPH,r16             ; Set Stack Pointer to top of RAM
0x001C              ldi     r16,low(RAMEND)
0x001D              out     SPL,r16
0x001E              sei                         ; Enable interrupts
0x001F              <instr> xxx
...       ...       ...                            ...
```

16.2. Interrupt Vectors in ATmega88/V

Table 16-2. Reset and Interrupt Vectors in ATmega88/V

Vector No	Program Address(2)	Source	Interrupts definition
1	0x0000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
2	0x0001	INT0	External Interrupt Request 0
3	0x0002	INT1	External Interrupt Request 0
4	0x0003	PCINT0	Pin Change Interrupt Request 0
5	0x0004	PCINT1	Pin Change Interrupt Request 1
6	0x0005	PCINT2	Pin Change Interrupt Request 2
7	0x0006	WDT	Watchdog Time-out Interrupt
8	0x0007	TIMER2_COMPA	Timer/Counter2 Compare Match A
9	0x0008	TIMER2_COMPB	Timer/Coutner2 Compare Match B

17.2.4. Pin Change Interrupt Control Register

Name: PCICR
Offset: 0x68
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
						PCIE2	PCIE1	PCIE0
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – PCIE2: Pin Change Interrupt Enable 2
When the PCIE2 bit is set and the I-bit in the Status Register (SREG) is set, pin change interrupt 2 is enabled. Any change on any enabled PCINT[23:16] pin will cause an interrupt. The corresponding interrupt of Pin Change Interrupt Request is executed from the PCI2 Interrupt Vector. PCINT[23:16] pins are enabled individually by the PCMSK2 Register.

Bit 1 – PCIE1: Pin Change Interrupt Enable 1
When the PCIE1 bit is set and the I-bit in the Status Register (SREG) is set, pin change interrupt 1 is enabled. Any change on any enabled PCINT[14:8] pin will cause an interrupt. The corresponding interrupt of Pin Change Interrupt Request is executed from the PCI1 Interrupt Vector. PCINT[14:8] pins are enabled individually by the PCMSK1 Register.

Bit 0 – PCIE0: Pin Change Interrupt Enable 0
When the PCIE0 bit is set and the I-bit in the Status Register (SREG) is set, pin change interrupt 0 is enabled. Any change on any enabled PCINT[7:0] pin will cause an interrupt. The corresponding interrupt of Pin Change Interrupt Request is executed from the PCI0 Interrupt Vector. PCINT[7:0] pins are enabled individually by the PCMSK0 Register.

MAX	The counter reaches its Maximum when it becomes 0xFF (decimal 255, for 8-bit counters) or 0xFFFF (decimal 65535, for 16-bit counters).
TOP	The counter reaches the TOP when it becomes equal to the highest value in the count sequence. The TOP value can be assigned to be the fixed value MAX or the value stored in the OCR0A Register. The assignment is dependent on the mode of operation.

19.2.2. Registers

The Timer/Counter 0 register (TCNT0) and Output Compare TC0x registers (OCR0x) are 8-bit registers. Interrupt request (abbreviated to Int.Req. in the block diagram) signals are all visible in the Timer Interrupt Flag Register 0 (TIFR0). All interrupts are individually masked with the Timer Interrupt Mask Register 0 (TIMSK0). TIFR0 and TIMSK0 are not shown in the figure.

The TC can be clocked internally, via the prescaler, or by an external clock source on the T0 pin. The Clock Select logic block controls which clock source and edge is used by the Timer/Counter to increment (or decrement) its value. The TC is inactive when no clock source is selected. The output from the Clock Select logic is referred to as the timer clock (clk_{T0}).

The double buffered Output Compare Registers (OCR0A and OCR0B) are compared with the Timer/Counter value at all times. The result of the compare can be used by the Waveform Generator to generate a PWM or variable frequency output on the Output Compare pins (OC0A and OC0B). See Output Compare Unit for details. The compare match event will also set the Compare Flag (OCF0A or OCF0B) which can be used to generate an Output Compare interrupt request.

Related Links

Timer/Counter 0, 1 Prescalers on page 193

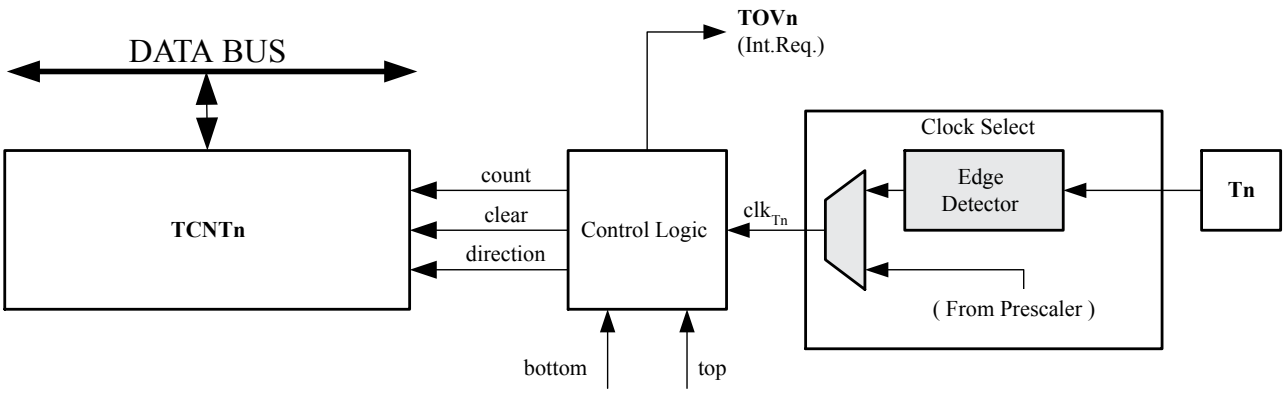
19.3. Timer/Counter Clock Sources

The TC can be clocked by an internal or an external clock source. The clock source is selected by writing to the Clock Select (CS0[2:0]) bits in the Timer/Counter Control Register (TCCR0B).

19.4. Counter Unit

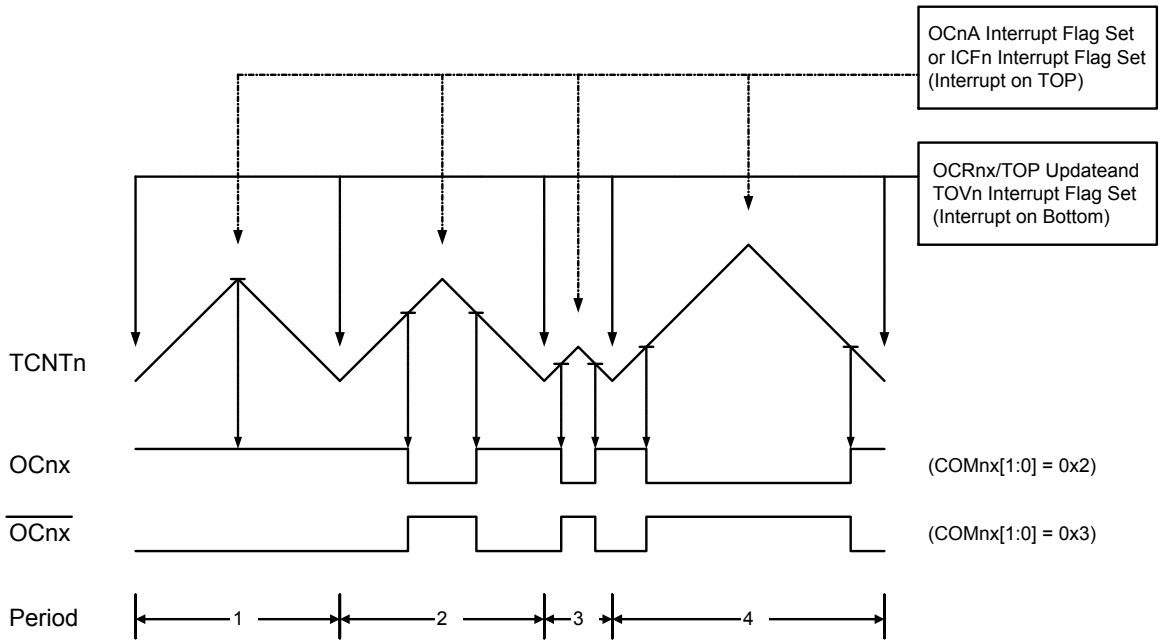
The main part of the 8-bit Timer/Counter is the programmable bi-directional counter unit. Below is the block diagram of the counter and its surroundings.

Figure 19-2. Counter Unit Block Diagram



Note: The “n” in the register and bit names indicates the device number (n = 0 for Timer/Counter 0), and the “x” indicates Output Compare unit (A/B).

Figure 20-9. Phase and Frequency Correct PWM Mode, Timing Diagram



Note: The “n” in the register and bit names indicates the device number (n = 1 for Timer/Counter 1), and the “x” indicates Output Compare unit (A/B).

The Timer/Counter Overflow Flag (TOV1) is set at the same timer clock cycle as the OCR1x Registers are updated with the double buffer value (at BOTTOM). When either OCR1A or ICR1 is used for defining the TOP value, the OC1A or ICF1 Flag set when TCNT1 has reached TOP. The Interrupt Flags can then be used to generate an interrupt each time the counter reaches the TOP or BOTTOM value.

When changing the TOP value the program must ensure that the new TOP value is higher or equal to the value of all of the Compare Registers. If the TOP value is lower than any of the Compare Registers, a compare match will never occur between the TCNT1 and the OCR1x.

As shown in the timing diagram above, the output generated is, in contrast to the phase correct mode, symmetrical in all periods. Since the OCR1x Registers are updated at BOTTOM, the length of the rising and the falling slopes will always be equal. This gives symmetrical output pulses and is therefore frequency correct.

Using the ICR1 Register for defining TOP works well when using fixed TOP values. By using ICR1, the OCR1A Register is free to be used for generating a PWM output on OC1A. However, if the base PWM frequency is actively changed by changing the TOP value, using the OCR1A as TOP is clearly a better choice due to its double buffer feature.

In phase and frequency correct PWM mode, the compare units allow generation of PWM waveforms on the OC1x pins. Setting the COM1x[1:0] bits to 0x2 will produce a non-inverted PWM and an inverted PWM output can be generated by setting the COM1x[1:0] to 0x3 (See description of TCCRA.COM1x). The actual OC1x value will only be visible on the port pin if the data direction for the port pin is set as output (DDR_OC1x). The PWM waveform is generated by setting (or clearing) the OC1x Register at the compare match between OCR1x and TCNT1 when the counter increments, and clearing (or setting) the OC1x Register at compare match between OCR1x and TCNT1 when the counter decrements. The PWM frequency for the output when using phase and frequency correct PWM can be calculated by the following equation:

$$f_{\mathrm{OCnxPFCPWM}} = \frac{f_{\mathrm{clk\_I/O}}}{2 \cdot N \cdot \mathrm{TOP}}$$

Mode	WGM13	WGM12 (CTC1)[1]	WGM11 (PWM11)[1]	WGM10 (PWM10)[1]	Timer/ Counter Mode of Operation	TOP	Update of OCR1x at	TOV1 Flag Set on
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	Reserved	-	-	-
14	1	1	1	0	Fast PWM	ICR1	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCR1A	BOTTOM	TOP

Note:

1. The CTC1 and PWM1[1:0] bit definition names are obsolete. Use the WGM1[3:0] definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

20.14.3. TC1 Control Register C

Name: TCCR1C
Offset: 0x82
Reset: 0x00
Property: -

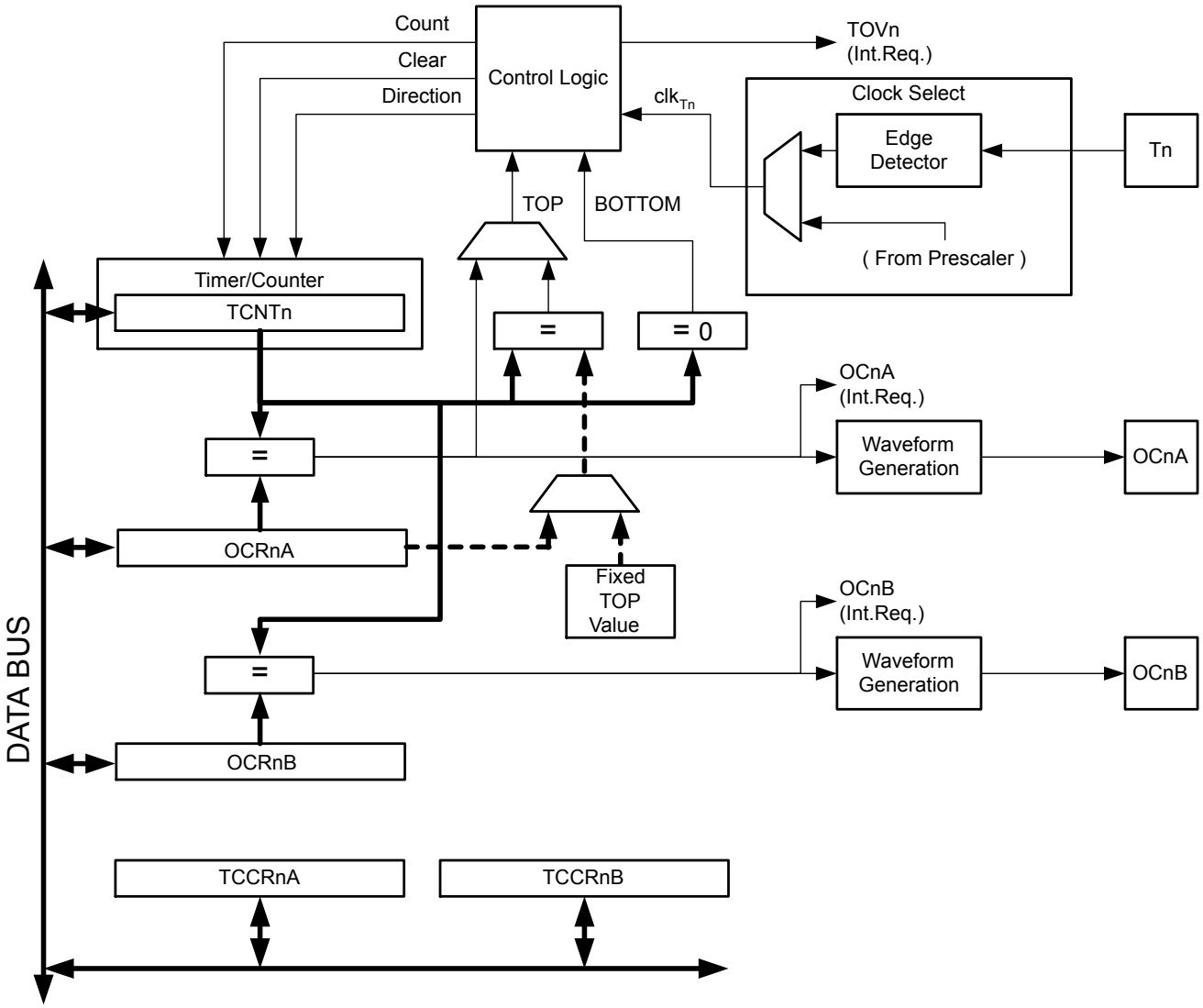
Bit	7	6	5	4	3	2	1	0
	FOC1A	FOC1B						
Access	R/W	R/W						
Reset	0	0						

Bit 7 – FOC1A: Force Output Compare for Channel A

Bit 6 – FOC1B: Force Output Compare for Channel B
The FOC1A/FOC1B bits are only active when the WGM1[3:0] bits specifies a non-PWM mode. When writing a logical one to the FOC1A/FOC1B bit, an immediate compare match is forced on the Waveform Generation unit. The OC1A/OC1B output is changed according to its COM1x[1:0] bits setting. Note that the FOC1A/FOC1B bits are implemented as strobes. Therefore it is the value present in the COM1x[1:0] bits that determine the effect of the forced compare.

A FOC1A/FOC1B strobe will not generate any interrupt nor will it clear the timer in Clear Timer on Compare match (CTC) mode using OCR1A as TOP. The FOC1A/FOC1B bits are always read as zero.

Figure 22-1. 8-bit Timer/Counter Block Diagram



Related Links

Pin Configurations on page 16

22.2.1. Definitions

Many register and bit references in this section are written in general form:

- n=2 represents the Timer/Counter number
- x=A,B represents the Output Compare Unit A or B

However, when using the register or bit definitions in a program, the precise form must be used, i.e., TCNT2 for accessing Timer/Counter2 counter value.

The following definitions are used throughout the section:

23.5.1. SPI Control Register 0

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

Name: SPCR0
Offset: 0x4C
Reset: 0x00
Property: When addressing as I/O Register: address offset is 0x2C

Bit	7	6	5	4	3	2	1	0
	SPIE0	SPE0	DORD0	MSTR0	CPOL0	CPHA0	SPR01	SPR00
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – SPIE0: SPI0 Interrupt Enable
This bit causes the SPI interrupt to be executed if SPIF bit in the SPSR Register is set and if the Global Interrupt Enable bit in SREG is set.

Bit 6 – SPE0: SPI0 Enable
When the SPE bit is written to one, the SPI is enabled. This bit must be set to enable any SPI operations.

Bit 5 – DORD0: Data0 Order
When the DORD bit is written to one, the LSB of the data word is transmitted first.

When the DORD bit is written to zero, the MSB of the data word is transmitted first.

Bit 4 – MSTR0: Master/Slave0 Select
This bit selects Master SPI mode when written to one, and Slave SPI mode when written logic zero. If SS is configured as an input and is driven low while MSTR is set, MSTR will be cleared, and SPIF in SPSR will become set. The user will then have to set MSTR to re-enable SPI Master mode.

Bit 3 – CPOL0: Clock0 Polarity
When this bit is written to one, SCK is high when idle. When CPOL is written to zero, SCK is low when idle. Refer to Figure 23-3 and Figure 23-4 for an example. The CPOL functionality is summarized below:

Table 23-3. CPOL0 Functionality

CPOL0	Leading Edge	Trailing Edge
0	Rising	Falling
1	Falling	Rising

Bit 2 – CPHA0: Clock0 Phase
The settings of the Clock Phase bit (CPHA) determine if data is sampled on the leading (first) or trailing (last) edge of SCK. Refer to Figure 23-3 and Figure 23-4 for an example. The CPHA functionality is summarized below:

Table 24-7. Examples of UBRRn Settings for Commonly Used Oscillator Frequencies

Baud Rate [bps]	f_{osc} = 16.0000MHz				f_{osc} = 18.4320MHz				f_{osc} = 20.0000MHz			
	U2Xn = 0		U2Xn = 1		U2Xn = 0		U2Xn = 1		U2Xn = 0		U2Xn = 1	
	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error	UBRRn	Error
2400	416	-0.1%	832	0.0%	479	0.0%	959	0.0%	520	0.0%	1041	0.0%
4800	207	0.2%	416	-0.1%	239	0.0%	479	0.0%	259	0.2%	520	0.0%
9600	103	0.2%	207	0.2%	119	0.0%	239	0.0%	129	0.2%	259	0.2%
14.4k	68	0.6%	138	-0.1%	79	0.0%	159	0.0%	86	-0.2%	173	-0.2%
19.2k	51	0.2%	103	0.2%	59	0.0%	119	0.0%	64	0.2%	129	0.2%
28.8k	34	-0.8%	68	0.6%	39	0.0%	79	0.0%	42	0.9%	86	-0.2%
38.4k	25	0.2%	51	0.2%	29	0.0%	59	0.0%	32	-1.4%	64	0.2%
57.6k	16	2.1%	34	-0.8%	19	0.0%	39	0.0%	21	-1.4%	42	0.9%
76.8k	12	0.2%	25	0.2%	14	0.0%	29	0.0%	15	1.7%	32	-1.4%
115.2k	8	-3.5%	16	2.1%	9	0.0%	19	0.0%	10	-1.4%	21	-1.4%
230.4k	3	8.5%	8	-3.5%	4	0.0%	9	0.0%	4	8.5%	10	-1.4%
250k	3	0.0%	7	0.0%	4	-7.8%	8	2.4%	4	0.0%	9	0.0%
0.5M	1	0.0%	3	0.0%	–	–	4	-7.8%	–	–	4	0.0%
1M	0	0.0%	1	0.0%	–	–	–	–	–	–	–	–
Max.(1)	1Mbps		2Mbps		1.152Mbps		2.304Mbps		1.25Mbps		2.5Mbps	

(1) UBRRn = 0, Error = 0.0%

Related Links

Asynchronous Operational Range on page 245

24.12. Register Description

24.12.4. USART Control and Status Register 0 C

Name: UCSR0C
Offset: 0xC2
Reset: 0x06
Property: -

Bit	7	6	5	4	3	2	1	0
	UMSEL01	UMSEL00	UPM01	UPM00	USBS0	UCSZ01 / UDORD0	UCSZ00 / UCPHA0	UCPOL0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	0

Bits 7:6 – UMSEL0n: USART Mode Select 0 n [n = 1:0]
These bits select the mode of operation of the USART0

Table 24-8. USART Mode Selection

UMSEL0[1:0]	Mode
00	Asynchronous USART
01	Synchronous USART
10	Reserved
11	Master SPI (MSPIM)(1)

Note:
1. The UDORD0, UCPHA0, and UCPOL0 can be set in the same write operation where the MSPIM is enabled.

Bits 5:4 – UPM0n: USART Parity Mode 0 n [n = 1:0]
These bits enable and set type of parity generation and check. If enabled, the Transmitter will automatically generate and send the parity of the transmitted data bits within each frame. The Receiver will generate a parity value for the incoming data and compare it to the UPM0 setting. If a mismatch is detected, the UPE0 Flag in UCSR0A will be set.

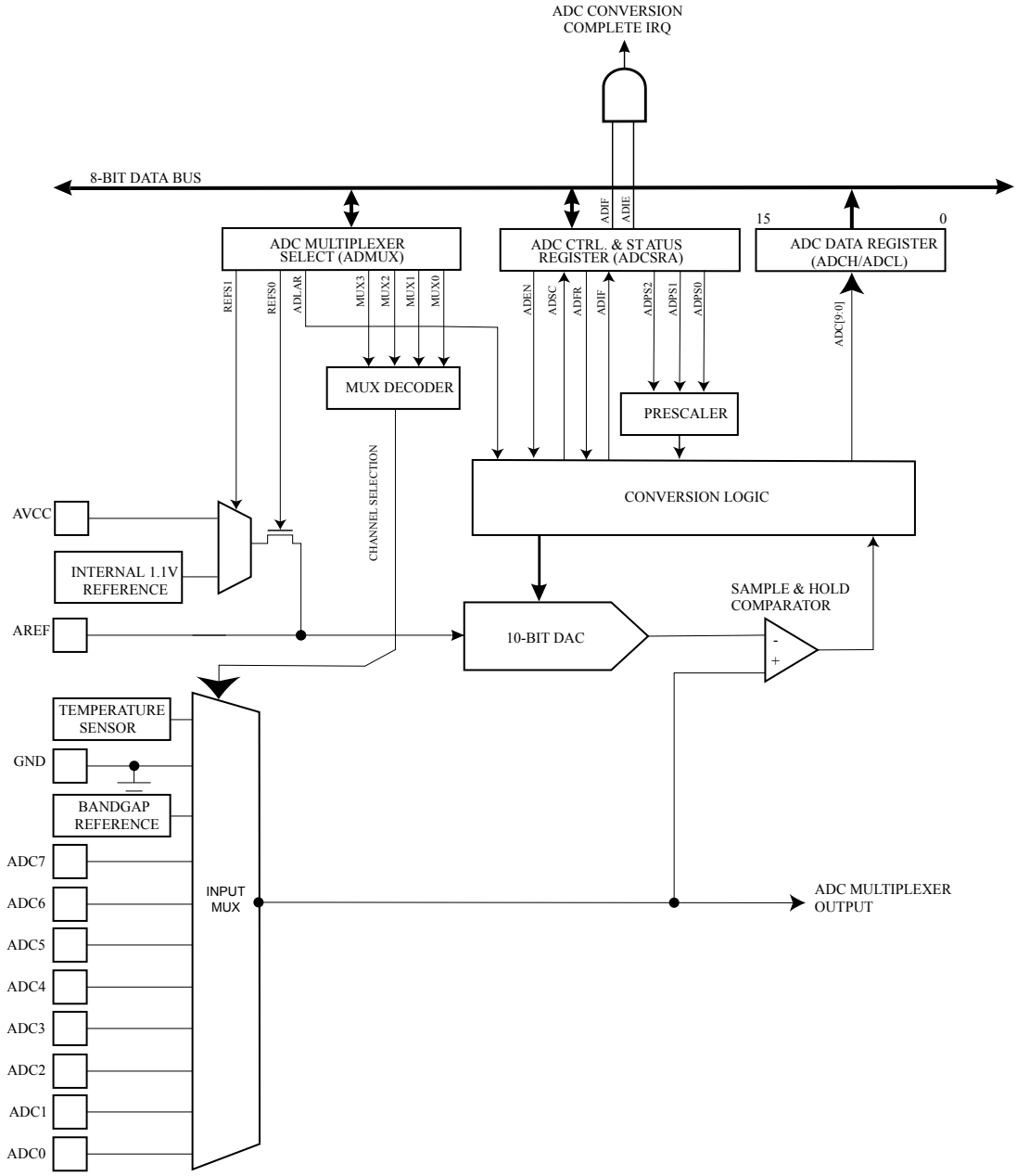
Table 24-9. USART Mode Selection

UPM0[1:0]	ParityMode
00	Disabled
01	Reserved
10	Enabled, Even Parity
11	Enabled, Odd Parity

These bits are reserved in Master SPI Mode (MSPIM).

Bit 3 – USBS0: USART Stop Bit Select 0
This bit selects the number of stop bits to be inserted by the Transmitter. The Receiver ignores this setting.

Figure 28-1. Analog to Digital Converter Block Schematic Operation



The analog input channel is selected by writing to the MUX bits in the ADC Multiplexer Selection register ADMUX.MUX[3:0]. Any of the ADC input pins, as well as GND and a fixed bandgap voltage reference, can be selected as single ended inputs to the ADC. The ADC is enabled by writing a '1' to the ADC Enable bit in the ADC Control and Status Register A (ADCSRA.ADEN). Voltage reference and input channel selections will not take effect until ADEN is set. The ADC does not consume power when ADEN is cleared, so it is recommended to switch off the ADC before entering power saving sleep modes.

The ADC generates a 10-bit result which is presented in the ADC Data Registers, ADCH and ADCL. By default, the result is presented right adjusted, but can optionally be presented left adjusted by setting the ADC Left Adjust Result bit ADMUX.ADLAR.

If the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH, to ensure that the content of the Data Registers belongs to the same conversion: Once ADCL is read, ADC access to Data Registers is blocked. This means that if

MUX[3:0]	Single Ended Input
0110	ADC6
0111	ADC7
1000	Temperature sensor
1001	Reserved
1010	Reserved
1011	Reserved
1100	Reserved
1101	Reserved
1110	1.1V (V_{BG})
1111	0V (GND)

30. Self-Programming the Flash

30.1. Overview

In ATmega48/V, there is no Read-While-Write support and no separate Boot Loader Section. The SPM instruction can be executed from the entire Flash.

The device provides a Self-Programming mechanism for downloading and uploading program code by the MCU itself. The Self-Programming can use any available data interface and associated protocol to read code and write (program) that code into the Program Memory.

The Program Memory is updated in a page by page fashion. Before programming a page with the data stored in the temporary page buffer, the page must be erased. The temporary page buffer is filled with one word at a time using SPM, and the buffer can be filled either before the Page Erase command or between a Page Erase and a Page Write operation:

Alternative 1, fill the buffer before a Page Erase

- Fill temporary page buffer
- Perform a Page Erase
- Perform a Page Write

Alternative 2, fill the buffer after Page Erase

- Perform a Page Erase
- Fill temporary page buffer
- Perform a Page Write

If only a part of the page needs to be changed, the rest of the page must be stored (for example in the temporary page buffer) before the erase, and then be re-written. When using alternative 1, the Boot Loader provides an effective Read-Modify-Write feature which allows the user software to first read the page, do the necessary changes, and then write back the modified data. If alternative 2 is used, it is not possible to read the old data while loading since the page is already erased. The temporary page buffer can be accessed in a random sequence. It is essential that the page address used in both the Page Erase and Page Write operation is addressing the same page.

30.1.1. Performing Page Erase by Store Program Memory (SPM)

To execute Page Erase, set up the address in the Z-pointer (R30 and R31), write “0x00000011” to Store Program Memory Control and Status Register (SPMCSR) and execute Store Program Memory (SPM) within four clock cycles after writing SPMCSR. The data in R1 and R0 is ignored. The page address must be written to PCPAGE ([Z12:Z6]) in the Z-register. Other bits in the Z-pointer will be ignored during this operation.

- The CPU is halted during the Page Erase operation
  Note: If an interrupt occurs in the time sequence the four cycle access cannot be guaranteed. In order to ensure atomic operation you should disable interrupts before writing to SPMCSR.

30.1.2. Filling the Temporary Buffer (Page Loading)

To write an instruction word, set up the address in the Z-pointer (R30 and R31) and data in R1:R0, write “0x00000001” to SPMCSR and execute SPM within four clock cycles after writing SPMCSR. The content of PCWORD ([Z5:Z1]) in the Z-register is used to address the data in the temporary buffer. The temporary buffer will auto-erase after a Page Write operation or by writing the RWWSRE bit in SPMCSR. It is also

Symbol	Minimum Wait Delay
t_{WD_ERASE}	10.5ms
t_{WD_FUSE}	4.5ms

32.8.3. Serial Programming Instruction Set

This section describes the Instruction Set.

Table 32-18. Serial Programming Instruction Set (Hexadecimal values)

Instruction/Operation	Instruction Format			
	Byte 1	Byte 2	Byte 3	Byte 4
Programming Enable	0xAC	0x53	0x00	0x00
Chip Erase (Program Memory/EEPROM)	0xAC	0x80	0x00	0x00
Poll RDY/$\overline{BSY}$	0xF0	0x00	0x00	data byte out
Load Instructions				
Load Extended Address byte(1)	0x4D	0x00	Extended adr	0x00
Load Program Memory Page, High byte	0x48	0x00	adr LSB	high data byte in
Load Program Memory Page, Low byte	0x40	0x00	adr LSB	low data byte in
Load EEPROM Memory Page (page access)	0xC1	0x00	0000 000aa	data byte in
Read Instructions				
Read Program Memory, High byte	0x28	adr MSB	adr LSB	high data byte out
Read Program Memory, Low byte	0x20	adr MSB	adr LSB	low data byte out
Read EEPROM Memory	0xA0	0000 00aa	aaaa aaaa	data byte out
Read Lock bits	0x58	0x00	0x00	data byte out
Read Signature Byte	0x30	0x00	0000 000aa	data byte out
Read Fuse bits	0x50	0x00	0x00	data byte out
Read Fuse High bits	0x58	0x08	0x00	data byte out
Read Extended Fuse Bits	0x50	0x08	0x00	data byte out
Read Calibration Byte	0x38	0x00	0x00	data byte out
Write Instructions(6)				
Write Program Memory Page	0x4C	adr MSB(8)	adr LSB(8)	0x00
Write EEPROM Memory	0xC0	0000 00aa	aaaa aaaa	data byte in
Write EEPROM Memory Page (page access)	0xC2	0000 00aa	aaaa aa00	0x00
Write Lock bits	0xAC	0xE0	0x00	data byte in
Write Fuse bits	0xAC	0xA0	0x00	data byte in

Symbol	Parameter	Condition	Min.	Typ	Max	Units
t_{BG}	Bandgap reference start-up time	V_{CC}=2.7 T_A=25°C	-	40	70	µs
I_{BG}	Bandgap reference current consumption	V_{CC}=2.7 T_A=25°C	-	10	-	µA

Note:

1. Values are guidelines only.
2. The Power-on Reset will not work unless the supply voltage has been below VPOT (falling)

Table 33-7. BODLEVEL Fuse Coding(1)

BODLEVEL [2:0] Fuses	Min. V_{BOT}	Typ. V_{BOT}	Max V_{BOT}	Units
111	BOD Disabled			
110	1.7	1.8	2.0	V
101	2.5	2.7	2.9	
100	4.1	4.3	4.5	
011	Reserved			
010				
001				
000				

Note: V_{BOT} may be below nominal minimum operating voltage for some devices. For devices where this is the case, the device is tested down to V_{CC} = V_{BOT} during the production test. This guarantees that a Brown-Out Reset will occur before V_{CC} drops to a voltage where correct operation of the microcontroller is no longer guaranteed. The test is performed using BODLEVEL = 101 and BODLEVEL = 100 for ATmega48/88/168, and BODLEVEL = 110 and BODLEVEL = 101 for ATmega48V/88V/168V.

Symbol	Parameter	Condition	Min.	Max	Units
V_{OL}(1)	Output Low-voltage	3mA sink current	0	0.4	V
t_r(1)	Rise Time for both SDA and SCL		20 + 0.1C_b(3)(2)	300	ns
t_{of}(1)	Output Fall Time from V_{IHmin} to V_{ILmax}	10pF < C_b < 400pF(3)	20 + 0.1C_b(3)(2)	250	ns
t_{SP}(1)	Spikes Suppressed by Input Filter		0	50(2)	ns
I_i	Input Current each I/O Pin	0.1V_{CC} < V_i < 0.9V_{CC}	-10	10	µA
C_i(1)	Capacitance for each I/O Pin		–	10	pF
f_{SCL}	SCL Clock Frequency	f_{CK}(4) > max(16f_{SCL}, 250kHz)(5)	0	400	kHz
Rp	Value of Pull-up resistor	f_{SCL} ≤ 100kHz	$\frac{V_{CC} - 0.4V}{3mA}$	$\frac{1000ns}{C_b}$	Ω
		f_{SCL} > 100kHz	$\frac{V_{CC} - 0.4V}{3mA}$	$\frac{300ns}{C_b}$	Ω
$t_{HD;STA}$	Hold Time (repeated) START Condition	f_{SCL} ≤ 100kHz	4.0	–	µs
		f_{SCL} > 100kHz	0.6	–	µs
t_{LOW}	Low Period of the SCL Clock	f_{SCL} ≤ 100kHz	4.7	–	µs
		f_{SCL} > 100kHz	1.3	–	µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100kHz	4.0	–	µs
		f_{SCL} > 100kHz	0.6	–	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	f_{SCL} ≤ 100kHz	4.7	–	µs
		f_{SCL} > 100kHz	0.6	–	µs
$t_{HD;DAT}$	Data hold time	f_{SCL} ≤ 100kHz	0	3.45	µs
		f_{SCL} > 100kHz	0	0.9	µs
$t_{SU;DAT}$	Data setup time	f_{SCL} ≤ 100kHz	250	–	ns
		f_{SCL} > 100kHz	100	–	ns
$t_{SU;STO}$	Setup time for STOP condition	f_{SCL} ≤ 100kHz	4.0	–	µs
		f_{SCL} > 100kHz	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	f_{SCL} ≤ 100kHz	4.7	–	µs
		f_{SCL} > 100kHz	1.3	–	µs

Note:

1. This parameter is characterized and not 100% tested.
2. Required only for f_{SCL} > 100kHz.
3. C_b = capacitance of one bus line in pF.

12. Updated note in Bit Rate Generator Unit.
13. Updated “Bit 6 – ACBG: Analog comparator bandgap select”.
14. Updated Features in ADC - Analog to Digital Converter.
15. Updated Prescaling and Conversion Timing.
16. Updated Limitations of debugWIRE.
17. Added Table 33-4.
18. Updated Figure 20-7, Figure 34-44.
19. Updated rev. A in Errata ATmega48/V.
20. Added rev. C and D in Errata ATmega48/V.

39.18. Rev. 2545F-05/05

1. Added Resources.
2. Update Calibrated Internal RC Oscillator.
3. Updated Serial Programming Instruction Set.
4. Table notes in Common DC Characteristics updated.
5. Updated Errata.

39.19. Rev. 2545E-02/05

1. MLF-package alternative changed to “Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF”.
2. Updated EECR.
3. Updated Calibrated Internal RC Oscillator.
4. Updated External Clock.
5. Updated Table 33-6, Table 33-8, Table 33-5 and Table 32-18.
6. Added Pin Change Interrupt Timing.
7. Updated Figure 19-1.
8. Updated SPMCSR.
9. Updated Enter Programming Mode.
10. Updated Common DC Characteristics.
11. Updated Ordering Information .
12. Updated Errata ATmega88/V and Errata ATmega168/V.

39.20. Rev. 2545D-07/04

1. Updated instructions used with WDTCSR in relevant code examples.
2. Updated Table 13-5, Table 33-7, Table 31-10, and Table 31-12.
3. Updated System Clock Prescaler.
4. Moved TIMSK2 and TIFR2 to Register Description.
5. Updated cross-reference in Electrical Interconnection.
6. Updated equation in Bit Rate Generator Unit.
7. Added Page Size.
8. Updated Serial Programming Algorithm.
9. Updated Ordering Information for ATmega168/V.
10. Updated Errata ATmega88/V and Errata ATmega168/V.