Zilog - Z8018006FSC Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006fsc

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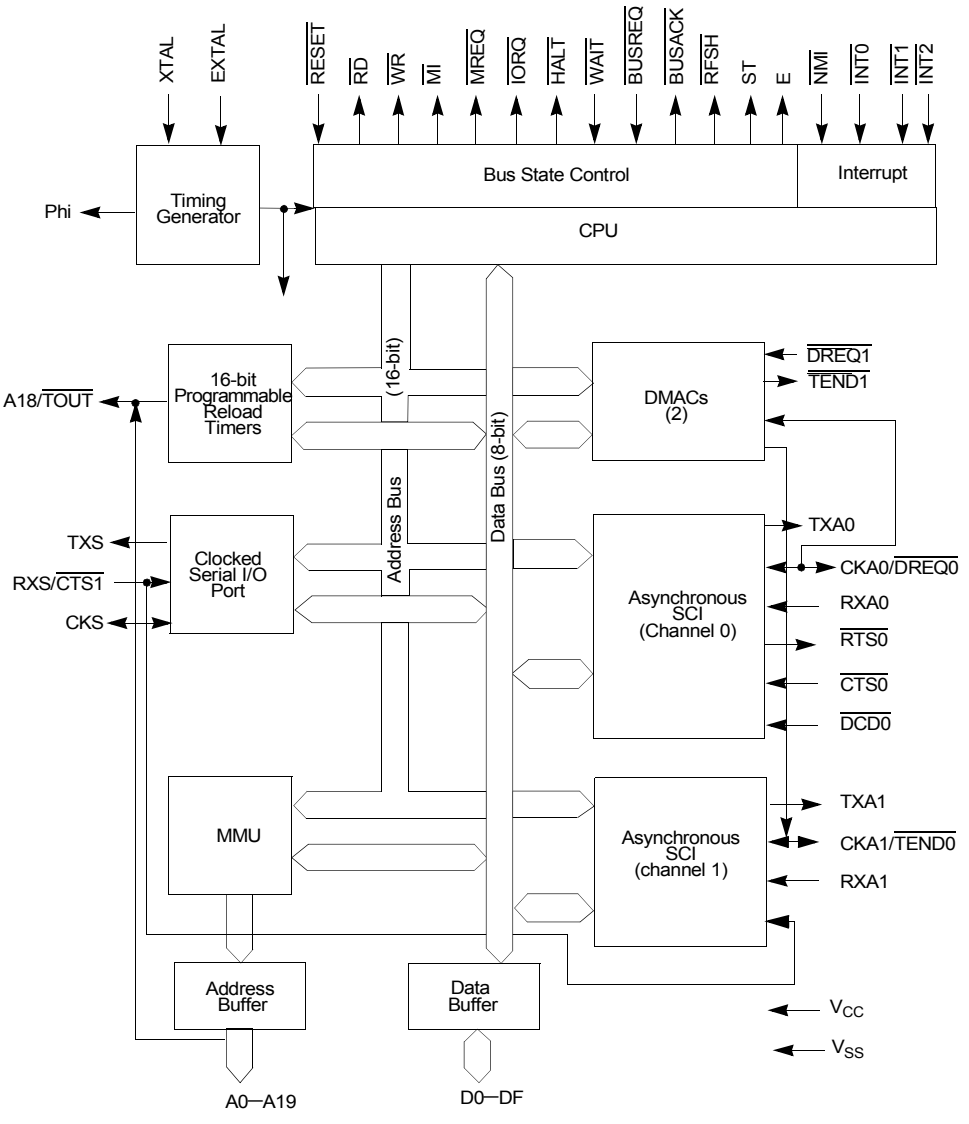


Figure 4. Z80180/Z8S180/Z8L180 Block Diagram

The external bus is IDLE while the CPU computes the effective address. Finally, the computed memory location is written with the contents of the CPU register (g).

RESET Timing

Figure 15 depicts the Z8X180 hardware RESET timing. If the $\overline{\text{RESET}}$ pin is Low for six or more clock cycles, processing is terminated and the Z8X180 restarts execution from (logical and physical) address `00000H`.

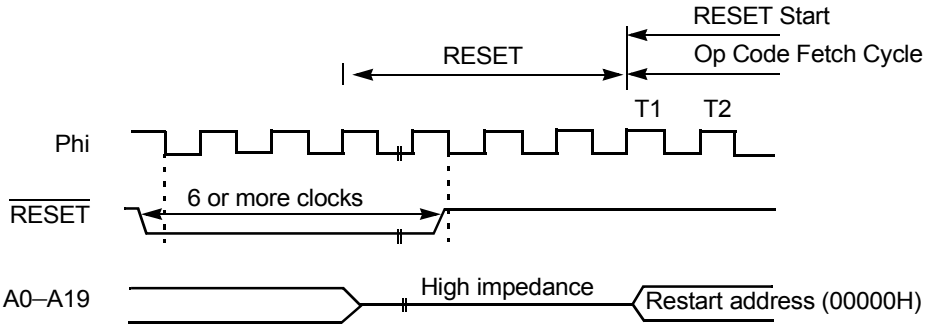


Figure 15. RESET Timing Diagram

$\overline{\text{BUSREQ}}$/$\overline{\text{BUSACK}}$ Bus Exchange Timing

The Z8X180 can coordinate the exchange of control, address and data bus ownership with another bus master. The alternate bus master can request the bus release by asserting the $\overline{\text{BUSREQ}}$ (Bus Request) input Low. After the Z8X180 releases the bus, it relinquishes control to the alternate bus master by asserting the $\overline{\text{BUSACK}}$ (Bus Acknowledge) output Low.

The bus may be released by the Z8X180 at the end of each machine cycle. In this context, a machine cycle consists of a minimum of three clock cycles (more if wait states are inserted) for Op Code fetch, memory read/write, and I/O read/write cycles. Except for these cases, a machine cycle corresponds to one clock cycle.

- Data Bus, 3-state

SLEEP mode is exited in one of two ways as described below.

- RESET Exit from SLEEP mode. If the $\overline{\text{RESET}}$ input is held Low for at least six clock cycles, it exits SLEEP mode and begins the normal RESET sequence with execution starting at address (logical and physical) 00000H.

- Interrupt Exit from SLEEP mode. The SLEEP mode is exited by detection of an external ($\overline{\text{NMI}}$, $\overline{\text{INT0}}$, $\overline{\text{INT2}}$) or internal (ASCI, CSI/O, PRT) interrupt.

In case of $\overline{\text{NMI}}$, SLEEP mode is exited and the CPU begins the normal $\overline{\text{NMI}}$ interrupt response sequence.

In the case of all other interrupts, the interrupt response depends on the state of the global interrupt enable flag IEF1 and the individual interrupt source enable bit.

If the individual interrupt condition is disabled by the corresponding enable bit, occurrence of that interrupt is ignored and the CPU remains in the SLEEP mode.

Assuming the individual interrupt condition is enabled, the response to that interrupt depends on the global interrupt enable flag (IEF1). If interrupts are globally enabled (IEF1 is 1) and an individually enabled interrupt occurs, SLEEP mode is exited and the appropriate normal interrupt response sequence is executed.

If interrupts are globally disabled (IEF1 is 0) and an individually enabled interrupt occurs, SLEEP mode is exited and instruction execution begins with the instruction following the SLP instruction. This feature provides a technique for synchronization with high speed external events without incurring the latency imposed by an interrupt response sequence.

Figure 21 depicts SLEEP timing.

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
DMA	DMA Source Address Register Ch 0L	SAR0L	XX100000	20H	93
	DMA Source Address Register Ch 0H	SAR0H	XX100001	21H	93
	DMA Source Address Register Ch 0B	SAR0B	XX100010	22H	93
	DMA Destination Address Register Ch 0L	DAR0L	XX100011	23H	94
	DMA Destination Address Register Ch 0H	DAR0H	XX100100	24H	94
	DMA Destination Address Register Ch 0B	DAR0B	XX100101	25H	94
	DMA Byte Count Register Ch 0L	BCR0L	XX100110	26H	94
	DMA Byte Count Register Ch 0H	BCR0H	XX100111	27H	94
	DMA Memory Address Register Ch 1L	MAR1L	XX101000	28H	94
	DMA Memory Address Register Ch 1H	MAR1H	XX101001	29H	94
	DMA Memory Address Register Ch 1B	MAR1B	XX101010	2AH	94
	DMA I/O Address Register Ch 1L	IAR1L	XX101011	2BH	102
	DMA I/O Address Register Ch 1H	IAR1H	XX101100	2CH	102
	DMA I/O Address Register Ch 1	IAR1B	XX101101	2DH	94
	DMA Byte Count Register Ch 1L	BCR1L	XX101110	2EH	94
	DMA Byte Count Register Ch 1H	BCR1H	XX101111	2FH	94
	DMA Status Register	DSTAT	XX110000	30H	95
	DMA Mode Register	DMODE	XX110001	31H	97
	DMA/WAIT Control Register	DCNTL	XX110010	32H	101

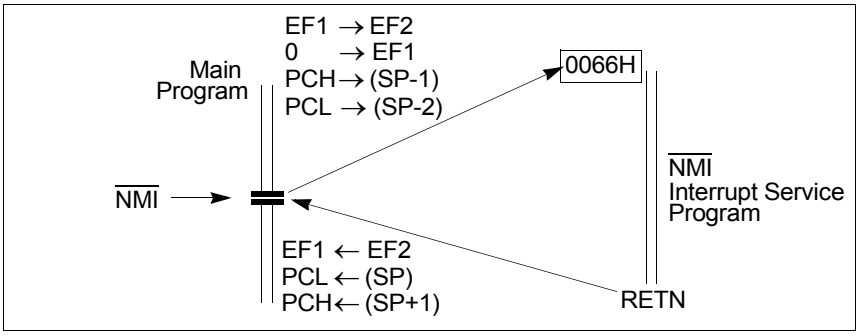
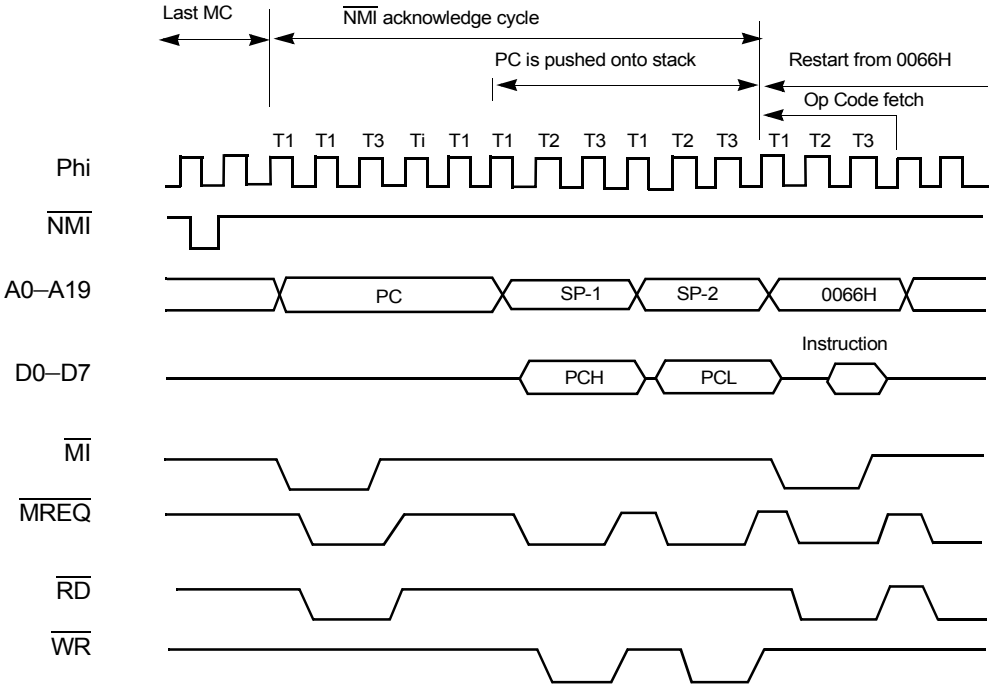


Figure 34. NMI Use



Bit Position	Bit/Field	R/W	Value	Description
0	DME	R		**DMA Main Enable** — A DMA operation is only enabled when its DE bit DE0 for channel 0, DE1 for channel 1) and the DME bit are set to 1. When $\overline{\text{NMI}}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{\text{NMI}}$ interrupt service routine. To restart DMA, DE0 and/or DE1 must be written with 1 (even if the contents are already 1). This action automatically sets DME to 1, allowing DMA operations to continue. DME cannot be directly written. It is cleared to 0 by $\overline{\text{NMI}}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1.DME is cleared to 0 during RESET.

DMA Mode Register (DMODE)

DMODE is used to set the addressing and transfer mode for channel 0.

DMA Mode Register (DMODE: 31H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	?		DM1	DM0	SM1	SM0	MMOD	?
R/W	?		R/W	R/W	R/W	R/W	R/W	?
Reset	?		0	0	0	0	0	?

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
5–4	DM1:0	R/W		**Destination Mode Channel 0** — Specifies whether the destination for channel 0 transfers is memory, I/O or memory mapped I/O and the corresponding address modifier. Reference Table 12.

$\overline{\text{DREQ0}}$ for ASCI transmission and reception respectively. To initiate memory to/from ASCI DMA transfer, perform the following operations:

1. Load the source and destination addresses into SAR0 and DAR0 Specify the I/O (ASCI) address as follows:
   a. Bits A0–A7 must contain the address of the ASCI channel transmitter or receiver (I/O addresses 6H-9H).
   b. Bits A8–A15 must equal 0.
   c. Bits SAR17–SAR16 must be set according to Table 16 to enable use of the appropriate ASCI status bit as an internal DMA request.

Table 16. DMA Transfer Request

SAR18	SAR17	SAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	RDRF (ASCI channel 0)
X	1	0	RDRF (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

DAR18	DAR17	DAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	TDRE (ASCI channel O)
X	1	0	TDRE (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

Bit Position	Bit/Field	R/W	Value	Description
5	PE	R		**Parity Error** — PE is set to 1 when a parity error is detected on an incoming data byte and ASCI parity detection is enabled (the MOD1 bit of CNTLA is set to 1). PE is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.
4	FE	R		**Framing Error** — If a receive data byte frame is delimited by an invalid stop bit (that is, 0, should be 1), FE is set to 1. FE is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.
3	RIE	R/W		**Receive Interrupt Enable** — RIE must be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, if any of the flags RDRF, OVRN, PE, or FE become set to 1, an interrupt request is generated. For channel 0, an interrupt is also generated by the transition of the external $\overline{\text{DCD0}}$ input from Low to High.
2	$\overline{\text{DCD0}}$	R		**Data Carrier Detect** — Channel 0 has an external $\overline{\text{DCD0}}$ input pin. The $\overline{\text{DCD0}}$ bit is set to 1 when the $\overline{\text{DCD0}}$ input is HIGH. It is cleared to 0 on the first read of (STAT0, following the $\overline{\text{DCD0}}$ input transition from HIGH to LOW and during RESET. When $\overline{\text{DCD0}}$ is 1, receiver unit is reset and receiver operation is inhibited.
1	TDRE	R		**Transmit Data Register Empty** — TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. When the external $\overline{\text{CTS}}$ input is High, TDRE is reset to 0.

pins are initialized as ASCI data clock inputs. If SS2, SS1 and SS0 are reprogrammed (any other value than SS2, SS1, SS0 = 1) these pins become ASCI data clock inputs. However, if DMAC channel 0 is configured to perform memory to/from I/O (and memory mapped I/O) transfers the CKA0/$\overline{\text{DREQ0}}$ pin reverts to DMA control signals regardless of SS2, SS1, SS0 programming.

Also, if the CKA1D bit in the CNTLA register is 1, then the CKA1/$\overline{\text{TEND0}}$ reverts to the DMA Control output function regardless of SS2, SS1 and SS0 programming. Final data clock rates are based on $\overline{\text{CTS}}$/PS (prescale), DR, SS2, SS1, SS0 and the Z8X180 system clock frequency (Reference Table 19).

Table 18. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷ 1
0	0	1	÷ 2
0	1	0	÷ 4
0	1	1	÷ 8
1	0	0	÷ 16
1	0	1	÷ 32
1	1	0	÷ 64
1	1	1	external clock

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

Z80180 DC CHARACTERISTICS

V_{CC} = 5V ± 10%, V_{SS} = OV, Ta = 0° to +70°C, unless otherwise noted.)

Table 28. Z80180 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VIH1	Input High Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		V_{CC} –0.6	–	V_{CC} +0.3	V
VIH2	Input High Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		2.0		V_{CC} +0.3	V
VIL1	Input Low Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.6	V
VIL2	Input Low Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.8 Standard 7 TL_{VIL}	V
VOH	Output High Voltage all outputs	IOH = –200 µA IOH = –20 µA	2.4 V_{CC} –1.2	– –	– –	V V
VOL	Output Low Voltage all outputs	IOL = 2.2 mA	–	–	0.45	V
I_{IL}	Input Leakage Current all inputs except XTAL, EXTAL	V_{IN} = 0.5~ V_{CC} –0.5	–	–	1.0	µA
ITL	Three-State Leakage Current		–	–	1.0	µA
ICC	Power Dissipation* (Normal Operation)	f = 6 MHz f = 8 MHz f = 33 MHz	– – –	15 20 25	40 50 60	mA mA mA

Table 45. Program Control Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Jump	JR Zj	00 101 000							D	2	6	continue : Z = 0	•	•	•	•	•	•
		<j-2>								2	8	PC_R, + j→PC_R : Z = 1						
	JR NZj	00 100 000							D	2	6	continue : Z = 1						
		<j-2>								2	8	PC_R + j→PC_R : Z = 0						
Return	RET	11001001						D		1	9	$(SP)_M$→PCLr	•	•	•	•	•	•
												$(SP + 1)_M$→PCHr						
												$SP_R + 2 → SP_R$						
	RET f	11f 000							D	1	5 (f : false)	continue : f is false	•	•	•	•	•	•
										1	10 (f : true)	RET : f is true						
	RETI	11101101						D		2	12 (R0,R1)	$(SP)_M$→PCLr	•	•	•	•	•	•
		01001101									ZZ(z)	$(SP + 1)_M$→PCHr						
												$SP_R + 2 → SP_R$						
	RETN	11101101						D		2	12	$(SP)_M$→PCLr	•	•	•	•	•	•
		01000101										$(SP + 1)_M$→PCHr						
												$SP_R + 2 → SP_R$						
												IEF2→IEF1						
Restart	RST v	11 v 111						D		1	11	PCHr→$(SP-1)_M$	•	•	•	•	•	•
												PCLr→$(SP-2)_M$						
												0→PCHr						
												v→PCLr						
												$SP_R-2 → SP_R$						

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
EX (SP),IX EX (SP),IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
	MC5	Ti	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	SP+1	IXH IYH	1	0	0	1	1	1	1
	MC7	T1T2T3	SP	IXL IYL	1	0	0	1	1	1	1
HALT	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	—	—	Next Op Code Address	Next Op Code	0	1	0	1	0	0	0
IM0 IM1 IM2	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
INC g DEC g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
INC (HL) DEC (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	HL	DATA	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
OTIM** OTDM**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC5	T1T2T3	C to A0~A7 00H to A8~A15	DATA	1	0	1	0	1	1	1
	MC6	Ti	*	Z	1	1	1	1	1	1	1
OTIMR** OTDMR** (If Br≠0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC5	T1T2T3	C to A0~A7 00H to A8~A15	DATA	1	0	1	0	1	1	1
	MC6~MC8	TiTiTi	*	Z	1	1	1	1	1	1	1

Operating Modes Summary

REQUEST ACCEPTANCES IN EACH OPERATING MODE

Table 53. Request Acceptances in Each Operating Mode

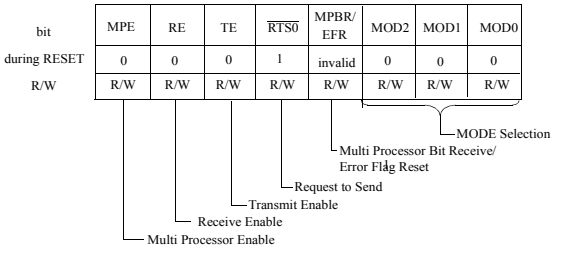
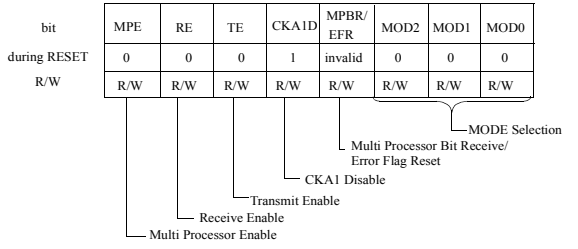
Current Status / Request		Normal Operation (CPU mode and IOSTOP Mode)	WAIT State	Refresh Cycle	Interrupt Acknowledge Cycle	DMA Cycle	BUS RELEASE Mode	SLEEP Mode	SYSTEM STOP Mode
$\overline{WAIT}$		Acceptable	Acceptable	Not acceptable	Acceptable	Acceptable	Not acceptable	Not acceptable	Not acceptable
Refresh Request Request of Refresh by the on-chip Refresh Controller		Refresh cycle begins at the end of Machine Cycle (MC)	Not acceptable	Not acceptable	Refresh cycle begins at the end MC	Refresh cycle begins at the end of MC	Not acceptable	Not acceptable	Not acceptable
$\overline{DREQ0}$ $\overline{DREQ1}$		DMA cycle begins at the end of MC	DMA cycle begins at the end of MC	Acceptable Refresh cycle precedes. DMA cycle begins at the end of one MC	Acceptable DMA cycle begins at the end of MC.	Acceptable Refer to "DMA Controller" for details.	Acceptable *After BUS RELEASE cycle, DMA cycle begins at the end of one MC	Not acceptable	Not acceptable
$\overline{BUSREQ}$		Bus is released at the end of MC	Not acceptable	Not acceptable	Bus is released at the end of MC	Bus is released at the end of MC	Continue BUS RELEASE mode	Acceptable	Acceptable
Interrupt	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$	Accepted after executing the current instruction.	Accepted after executing the current instruction	Not acceptable	Not acceptable	Not acceptable	Not acceptable	Acceptable Return from SLEEP mode to normal operation.	Acceptable Return from SYSTEM STOP mode to normal operation

I/O Registers

INTERNAL I/O REGISTERS

By programming IOA7 and IOA6 as the I/O control register, internal I/O register addresses are relocatable within ranges from 0000H to 00FFH in the I/O address space.

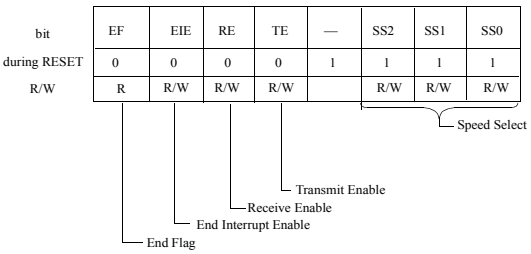
Table 57. Internal I/O Registers

Register	Mnemonics	Address		Remarks
ASCI Control Register A Channel 0:	CNTLA0	0	0	
ASCI Control Register A Channel 1:	CNTLA1	0	1	

MOD 2 1 0
0 0 0 Start + 7 bit Data + 1 Stop
0 0 1 Start + 7 bit Data + 2 Stop
0 1 0 Start + 7 bit Data + Parity + 1 Stop
0 1 1 Start + 7 bit Data + Parity + 2 Stop
1 0 0 Start + 8 bit Data + 1 Stop
1 0 1 Start + 8 bit Data + 2 Stop
1 1 0 Start + 8 bit Data + Parity + 1 Stop
1 1 1 Start + 8 bit Data + Parity + 2 Stop

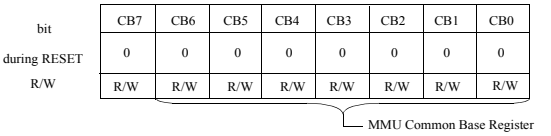
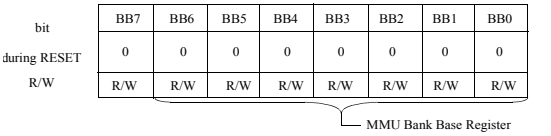
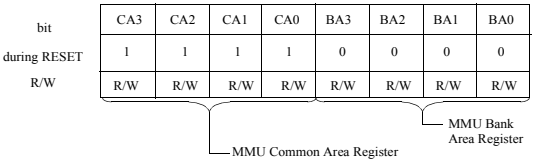
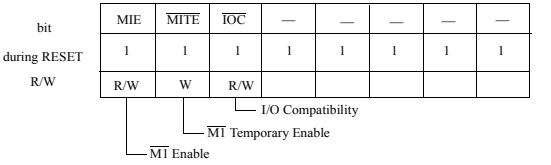
Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Transmit Data Register Channel 0:	TDR0	0	6	
ASCI Transmit Data Register Channel 1:	TDR1	0	7	
ASCI Receive Data Register Channel 0:	TSR0	0	8	
ASCI Receive Data Register Channel 1:	TSR1	0	9	
CSI/O Control Register:	CNTR	0	A	



SS2 1 0	Baud Rate	SS2 1 0	Baud Rate
0 0 0	Phi ÷ 20	1 0 0	Phi ÷ 320
0 0 1	÷ 40	1 0 1	÷ 640
0 1 0	÷ 80	1 1 0	÷ 1280
0 1 1	÷ 160	1 1 1	External frequency < ÷ 20)

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
MMU Common Base Register:	CBR	3	8	
MMU Bank Base Register	BBR	3	9	
MMU Common/Bank Register	CBAR	3	A	
Operation Mode Control Register	OMCR	3	E	
I/O Control Register:	ICR	3	F