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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006fsg

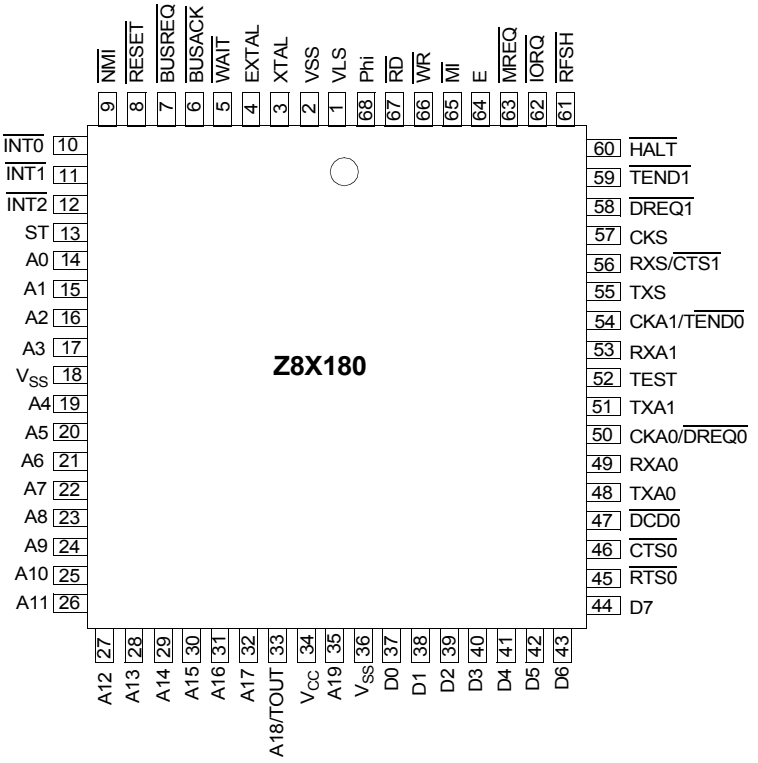

Figure 2. 68-Pin PLCC

PIN DESCRIPTION

A0–A19. *Address Bus (Output, Active High, 3-state).* A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges, up to 1 MB, and I/O data bus exchanges, up to 64K. The address bus enters a high impedance state during RESET and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (TOUT, selected as address output on RESET) and address line A19 is not available in DIP versions of the Z8X180.

$\overline{\text{BUSACK}}$. *Bus Acknowledge (Output, Active Low).* $\overline{\text{BUSACK}}$ indicates that the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

$\overline{\text{BUSREQ}}$. *Bus Request (Input, Active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions and places the address and data buses, and other control signals, into the high impedance state.

CKA0, CKA1. *Asynchronous Clock 0 and 1 (Bidirectional, Active High).* These pins are the transmit and receive clocks for the ASCI channels. CKA0, is multiplexed with $\overline{\text{DREQ0}}$ and CKA1 is multiplexed with $\overline{\text{TEND0}}$.

CKS. *Serial Clock (Bidirectional, Active High).* This line is the clock for the CSIO channel.

CLOCK (PHI). *System Clock (Output, Active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency.

$\overline{\text{CTS0}}$, $\overline{\text{CTS1}}$. *Clear to Send 0 and 1 (Inputs, Active Low).* These lines are modem control signals for the ASCI channels. $\overline{\text{CTS1}}$ is multiplexed with RXS.

Low Power Modes (Z8S180/Z8L180 only)

The following section is a detailed description of the enhancements to the Z8S180/L180 from the standard Z80180 in the areas of STANDBY, IDLE and STANDBY QUICK RECOVERY modes.

Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce current consumption. The Z8S180 features two additional power-down modes, STANDBY and IDLE, to reduce current consumption even further. The differences in these power-down modes are summarized in Table 5.

Z8X180. Figure 43 illustrates the INT1, INT2 and internal interrupts timing.

Table 10. RETI Control Signal States

Machine Cycle	States	Address	Data	$\overline{MI}$							
				$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1E=1}$	$\overline{M1E=0}$	$\overline{HALT}$	ST
1	T1-T3	1st Op Code	EDH	0	1	0	1	0	1	1	0
2	TI-T3	2nd Op Code	4DH	0	1	0	1	0	1	1	1
3	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
4	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
5	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
6	T1-T3	1st Op Code	EDH	0	1	0	1	0	0	1	1
7	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
8	T1-T3	2nd Op Code	4DH	0	1	0	1	0	1	1	1
9	T1-T3	SP	data	0	1	0	1	1	1	1	1
10	T1-T3	SP+1	data	0	1	0	1	1	1	1	1

IOC affects the IORQ/RD signals. M1E affects the assertion of M1. One state also reflects a 1 while the other reflects a 0

Bit Position	Bit/Field	R/W	Value	Description
2–0	MOD2–0	R/W		**ASCI Data Format Mode 2, 1, 0** — These bits program the ASCI data format as follows. **MOD2** 0: 7 bit data 1: 8 bit data **MOD1** 0: No parity 1: Parity enabled **MOD0** 0: 1 stop bit 1: 2 stop bits The data formats available based on all combinations of MOD2, MOD1 and MOD0 are described in Table 17.

ASCI to/from DMAC Operation

Operation of the ASCI with the on-chip DMAC channel 0 requires that the DMAC be correctly configured to use the ASCI flags as DMA request signals.

ASCI and RESET

During RESET, the ASCI status and control registers are initialized as defined in the individual register descriptions.

Receive and Transmit operations are stopped during RESET. However, the contents of the transmit and receive data registers (TDR and RDR) are not changed by RESET.

ASCI Clock

When in external clock input mode, the external clock is directly input to the sampling rate (÷16/÷64) as depicted in Figure 56.

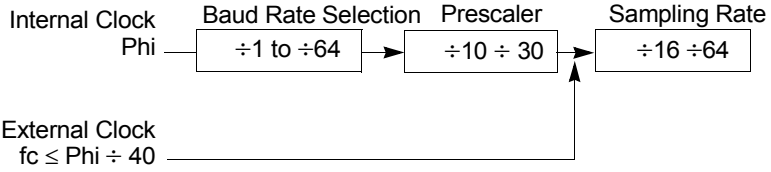

Figure 56. ASCI Clock

Table 19. ASCI Baud Rate Selection

Prescaler		Sampling Rate		Baud Rate				General Divide Ratio	Baud Rate (Example) (BPS)			CKA	
PS	Divide Ratio	DR	Rate	SS2	SS1	SS0	Divide Ratio		ϕ = 6.144 MHz	ϕ = 4.608 MHz	ϕ = 3.072 MHz	I/O	Clock Frequency
0	$\phi \div 10$	0	16	0	0	0	÷1	$\phi \div 160$	38400		19200		$\phi \div 10$
				0	0	1	2	320	19200		9600		20
				0	1	0	4	640	9600		4800		40
				0	1	1	8	1280	4800		2400	0	80
				1	0	0	16	2560	2400		1200		160
				1	0	1	32	5120	1200		600		320
				1	1	0	64	10240	600		300		640
				1	1	1	—	fc ÷ 16	—	—	—	I	fc
		1	64	0	0	0	÷1	0÷640	9600		4800		$\phi \div 10$
				0	0	1	2	1280	4800		2400		20
				0	1	0	4	2560	2400		1200		40
				0	1	1	8	5120	1200		600	0	80
				1	0	0	16	10240	600		300		160
				1	0	1	32	20480	300		150		320
				1	1	0	64	40960	150		75		640
				1	1	1	—	fc ÷ 64	—	—	—	I	fc

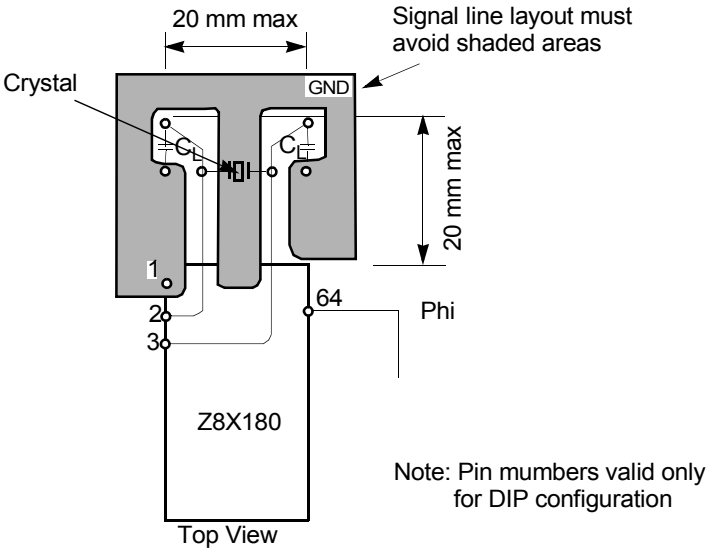

Figure 73. Example of Board Design

Circuit Board design should observe the following parameters.

- Locate the crystal and load capacitors as close to the IC as physically possible to reduce noise.
- Signal lines must not run parallel to the clock oscillator inputs. In particular, the clock input circuitry and the system clock output (pin 64) must be separated as much as possible.
- V_{CC} power lines must be separated from the clock oscillator input circuitry.
- Resistivity between XTAL or EXTAL and the other pins must be greater than 10M ohms.

Signal line layout must avoid areas marked with the shaded area of Figure 73.

Software Architecture

INSTRUCTION SET

The Z80180 is object code-compatible with the Z80 CPU. Refer to the *Z80 CPU Technical Manual* or the *Z80 Assembly Language Programming Manual* for further details.

Table 26. Instruction Set Summary

New Instructions	Operation
SLP	Enter SLEEP mode
MLT	8-bit multiply with 16-bit result
INO g, (m)	Input contents of immediate I/O address
OUT0 (m), g	Output register contents to immediate I/O address
OTIM	Block output - increment
OTIMR	Block output - increment and repeat
OTDM	Block output - decrement
OTDMR	Block output - decrement and repeat
TSTIO m	Non-destructive AND, I/O port, and accumulator
TST g	Non-destructive AND, register, and accumulator
TST m	Non-destructive AND, immediate data, and accumulator
TST (HL)	Non-destructive AND, memory data, and accumulator

SLP - Sleep

The SLP instruction causes the Z80180 to enter the SLEEP low power consumption mode. See page 32 for a complete description of the SLEEP state.

Instruction Set

This section explains the symbols in the instruction set.

REGISTER

g, g', ww, xx, yy, and zz specify a register to be used. g and g' specify an 8-bit register. ww, xx, yy, and zz specify a pair of 8-bit registers. Table 32 describes the correspondence between symbols and registers.

Table 32. Register Values

g,g'	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

ww	Reg.
00	BC
01	DE
10	HL
11	SP

xx	Reg.
00	BC
01	DE
10	IX
11	SP

yy	Reg.
00	BC
01	DE
10	IY
11	SP

zz	Reg.
00	BC
01	DE
10	HL
11	AF

Note: Suffixed H and L to ww, xx, yy, zz (ex. wwH, IXL) indicate upper and lower 8-bit of the 16-bit register respectively.

BIT

b specifies a bit to be manipulated in the bit manipulation instruction. Table 33 indicates the correspondence between **b** and bits.

Table 43. Block Transfer (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	CPI	11101101					S	S		2	12	Ar-$(HL)_M$	↑	↑	↑	↑	S	•
		10100001										BC_R-1→BC_R						
												HL_R + 1→HL_R		(3)		(2)		
	CPIR	11101101					S	S		2	14	$BC_R \neq 0$ Ar*$(HL)_M$	↑	↑	↑	↑	S	•
		10110001									12	BC_R = 0 or Ar = $(HL)_M$						
												Q: Ar-$(HL)_M$; BC_R-1→BC_R; HL_R + 1→HL_R						
												Repeat Q until						
												Ar = $(HL)_M$ or BC_R = 0				(2)		
	LDD	11 101 101					S/D			2	12	$(HL)_M \rightarrow (DE)_M$	•	•	R	↑	R	•
		10 101 000										BC_R -1→BC_R						
												DE_R-1→DE_R						
												HL_R-1→HL_R						
	LDDR	11 101 101					S/D			2	14($BC_R \neq 0$)	Q: $(HL)_M \rightarrow (DE)_M$; BC_R -1 → BC_R; DE_R -1 → DE_R; HL_R -1 → HL_R	•	•	R	R	R	•
		10 111 000									12(BC_R = 0)	Repeat Q until						
												BC_R = 0				(2)		
	LDI	11 101 101					S/D			2	12	$(HL)_M \rightarrow (DE)_R$	•	•	R	↑	R	•
		10 100 000										BC_R-1→BC_R						
												DE_R + 1→DE_R						
												HL_R + 1→HL_R						
	LDIR	11 101 101					S/D			2	14($BC_R \neq 0$)	Q: $(HL)_M \rightarrow (DE)_M$; BC_R-1→BC_R; DE_R + 1→DE_R; HL_R + 1→HL_R	•	•	R	R	R	•
		10 110 000									12(BC_R = 0)	Repeat Q until						
												BC_R = 0						

(2) P/V = 0: BC_R-1 = 0
P/V = 1: BC_R-1 ≠ 0
(3) Z = 1: Ar = $(HL)_M$
Z = 0 :Ar ≠ $(HL)_M$

MNEMONICS	Bytes	Machine Cycles	States
RRC (IY+d)	4	7	19
RRC g	2	3	7
RRD	2	8	16
RR (HL)	2	5	13
RR (IX+d)	4	7	19
RR (IY+d)	4	7	19
RR g	2	3	7
RST v	1	5	11
SBC A,(HL)	1	2	6
SBC A, (IX+d)	3	6	14
SBC A,(IY+d)	3	6	14
SBC A,m	2	2	6
SBC A,g	1	2	4
SBC HL,ww	2	6	10
SCF	1	1	3
SET b,(HL)	2	5	13
SET b,(IX+d)	4	7	19
SET b,(IY+d)	4	7	19
SET b,g	2	3	7
SLA (HL)	2	5	13
SLA (IX+d)	4	7	19
SLA (IY+d)	4	7	19
SLA g	2	3	7
SLP**	2	2	8
SRA (HL)	2	5	13
SRA (IX+d)	4	7	19
SRA (IY+d)	4	7	19
SRA g	2	3	7
SRL (HL)	2	5	13
SRL (IX+d)	4	7	19

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
IN g,(C)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	BC	DATA	0	1	1	0	1	1	1
INO g,(m)**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC4	T1T2T3	m to A0~A7 00H to A8~A15	DATA	0	1	1	0	1	1	1
INI IND	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	BC	DATA	0	1	1	0	1	1	1
	MC4	T1T2T3	HL	DATA	1	0	0	1	1	1	1
INIR INDR (If Br≠0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	BC	DATA	0	1	1	0	1	1	1
	MC4	T1T2T3	HL	DATA	1	0	0	1	1	1	1
	MC5~MC6	TiTi	*	Z	1	1	1	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
OTIM** OTDM**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC5	T1T2T3	C to A0~A7 00H to A8~A15	DATA	1	0	1	0	1	1	1
	MC6	Ti	*	Z	1	1	1	1	1	1	1
OTIMR** OTDMR** (If Br≠0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC5	T1T2T3	C to A0~A7 00H to A8~A15	DATA	1	0	1	0	1	1	1
	MC6~MC8	TiTiTi	*	Z	1	1	1	1	1	1	1

INTERRUPTS

Table 52. Interrupts

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
$\overline{NMI}$	MC1	T1T2T3	Next Op Code Address (PC)		0	1	0	1	0	1	0
	MC2 ~MC3	T1T1	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 0 (RST Inserted)	MC1	T1T2TW TWT3	Next Op Code Address	1st(PC) Op Code	1	1	1	0	0	1	0
	MC2 ~MC3	T1T1	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 0 (Call Inserted)	MC1	T1T2Tw TWT3	Next Op Code Address (PC)	1st Op Code	1	1	1	0	0	1	0
	MC2	T1T2T3	PC	n	0	1	0	1	1	1	1
	MC3	T1T2T3	PC+1	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP-1	PC+2(H)	1	0	0	1	1	1	1
	MC6	T1T2T3	SP-2	PC+2(L)	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 1	MC1	T1T2TW TWT3	Next Op Code Address (PC)		1	1	1	0	0	1	0
	MC2	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC3	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1

Note: If Bus Request and Refresh Request occur simultaneously, Bus Request is accepted but Refresh Request is cleared.

OPERATION MODE TRANSITION

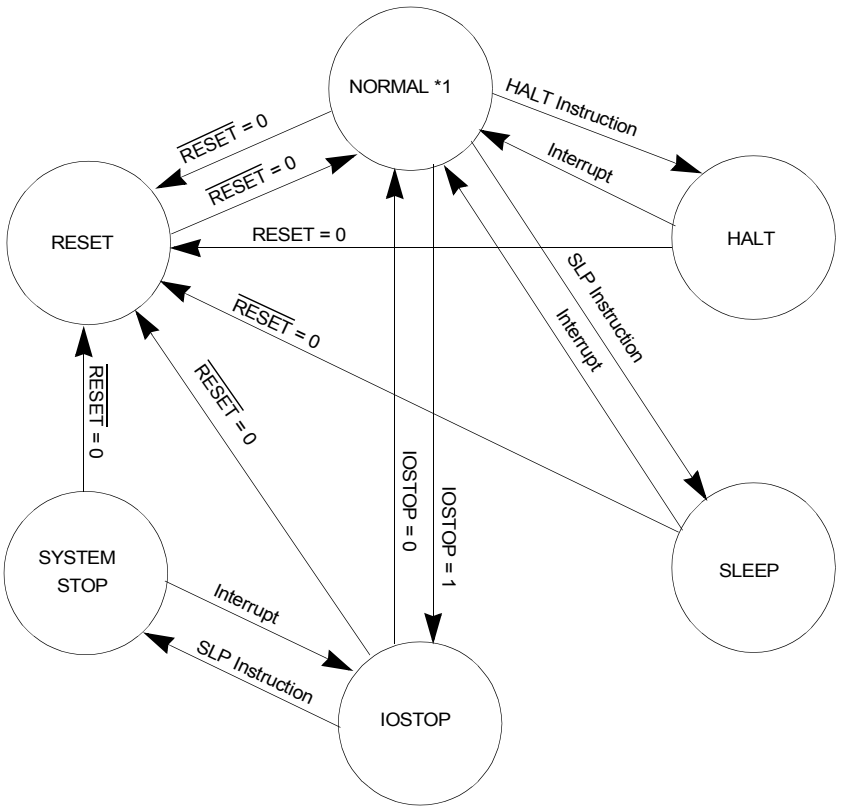

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
Timer Data Register Channel 1L:	TMDR1L	1	4	
Timer Data Register Channel 1H:	TMDR1H	1	5	
Timer Reload Register Channel 1L	RLDR1L	1	6	
Timer Reload Register Channel 1H:	RLDR1H	1	7	
Free Running Counter:	FRC	1	8	Read only
DMA Source Address Register Channel 0L:	SAR0L	2	0	
DMA Source Address Register Channel 0H:	SAR0H	2	1	
DMA Source Address Register Channel 0B:	SAR0B	2	2	Bits 0-2 (3) are used for SAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — RDR0 (ASCI0) X X 1 0 — RDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Destination Address Register Channel 0L:	DAR0L	2	3	
DMA Destination Address Register Channel 0H:	DAR0H	2	4	
DMA Destination Address Register Channel 0B:	DAR0B	2	5	Bits 0-2 (3) are used for DAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — TDR0 (ASCI0) X X 1 0 — TDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Byte Count Register Channel 0L:	BCROL	2	6	
DMA Byte Count Register Channel 0H:	BCROH	2	7	
DMA Memory Address Register Channel 1L:	MAR1L	2	8	
DMA Memory Address Register Channel 1H:	MAR1H	2	9	

* In the R1 and Z mask, these DMAC registers are expanded from 4 bits to 3 bits in the package version of CP-68.