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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006pec

Sections

Z8018X MPU Operation

Presents features, a general description, pins descriptions, block diagrams, registers, and details of operating modes for the Z8018x MPUs.

Software Architecture

Provides instruction sets and CPU registers for the Z8018x MPUs.

DC Characteristics

Presents the DC parameters and absolute maximum ratings for the Z8X180 MPUs.

AC Characteristics

Presents the AC parameters for the Z8018x MPUs.

Timing Diagrams

Contains timing diagrams and standard test conditions for the Z8018x MPUs.

Appendices

The appendixes in this manual provide additional information applicable to the Z8018x family of ZiLOG MPUs:

- Instruction set
- Instruction summary table
- Op Code map
- Bus Control signal conditions in each machine cycle and interrupt conditions
- Operating mode summary
- Status signals
- I/O registers and ordering information

Wait States (TW) are inserted as previously described for Op Code fetch cycles. Figure 11 illustrates the read/write timing without Wait States (Tw), while Figure 12 illustrates read/write timing with Wait States (TW).

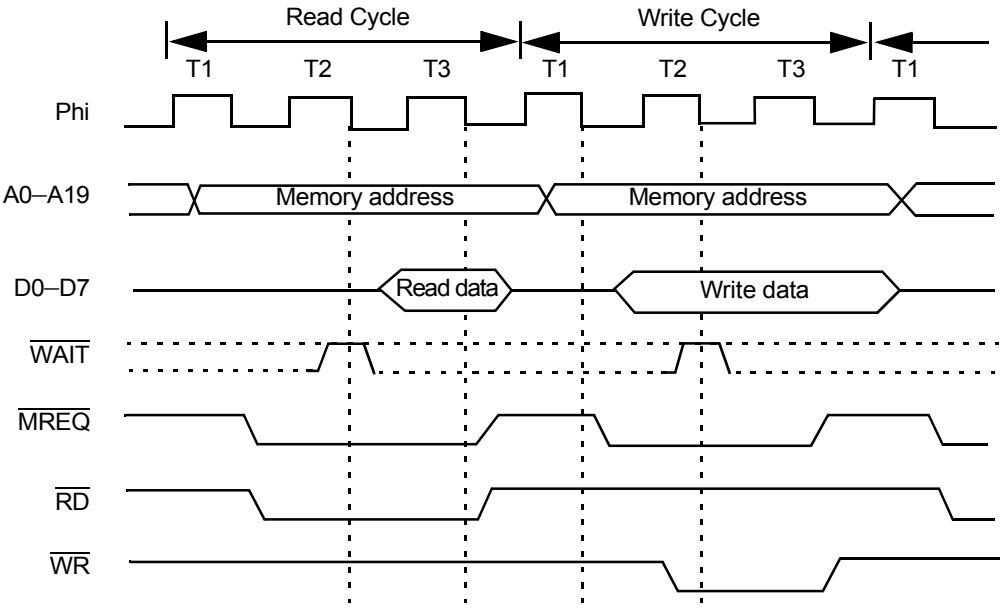

Figure 11. Memory Read/Write (without Wait State) Timing Diagram

- Data Bus, 3-state

SLEEP mode is exited in one of two ways as described below.

- RESET Exit from SLEEP mode. If the $\overline{\text{RESET}}$ input is held Low for at least six clock cycles, it exits SLEEP mode and begins the normal RESET sequence with execution starting at address (logical and physical) 00000H.

- Interrupt Exit from SLEEP mode. The SLEEP mode is exited by detection of an external ($\overline{\text{NMI}}$, $\overline{\text{INT0}}$, $\overline{\text{INT2}}$) or internal (ASCI, CSI/O, PRT) interrupt.

In case of $\overline{\text{NMI}}$, SLEEP mode is exited and the CPU begins the normal $\overline{\text{NMI}}$ interrupt response sequence.

In the case of all other interrupts, the interrupt response depends on the state of the global interrupt enable flag IEF1 and the individual interrupt source enable bit.

If the individual interrupt condition is disabled by the corresponding enable bit, occurrence of that interrupt is ignored and the CPU remains in the SLEEP mode.

Assuming the individual interrupt condition is enabled, the response to that interrupt depends on the global interrupt enable flag (IEF1). If interrupts are globally enabled (IEF1 is 1) and an individually enabled interrupt occurs, SLEEP mode is exited and the appropriate normal interrupt response sequence is executed.

If interrupts are globally disabled (IEF1 is 0) and an individually enabled interrupt occurs, SLEEP mode is exited and instruction execution begins with the instruction following the SLP instruction. This feature provides a technique for synchronization with high speed external events without incurring the latency imposed by an interrupt response sequence.

Figure 21 depicts SLEEP timing.

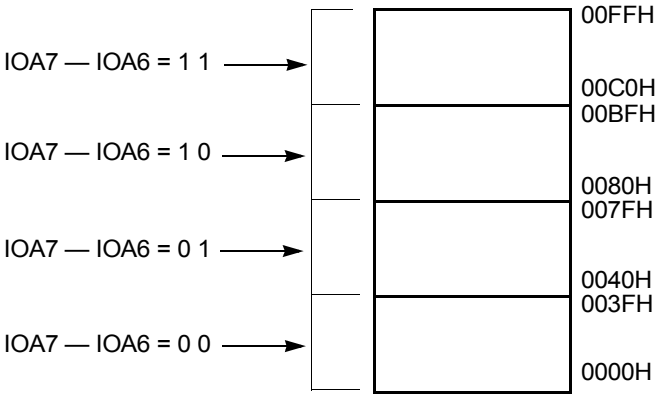

Figure 22. I/O Address Relocation

Internal I/O Registers Address Map

The internal I/O register addresses are described in Table 6 and Table 7. These addresses are relative to the 64-byte boundary base address specified in ICR.

I/O Addressing Notes

The internal I/O register addresses are located in the I/O address space from `0000H` to `00FFH` (16-bit I/O addresses). Thus, to access the internal I/O registers (using I/O instructions), the high-order 8 bits of the 16-bit I/O address must be `0`.

The conventional I/O instructions (OUT (m), A/IN A, (m) / OUTI/INI, for example) place the contents of a CPU register on the high-order 8 bits of the address bus, and thus may be difficult to use for accessing internal I/O registers.

For efficient internal I/O register access, a number of new instructions have been added, which force the high-order 8 bits of the 16-bit I/O

Bit Position	Bit/Field	R/W	Value	Description
2	LNIO	R/W	0 1	Standard Drive 33% Drive on certain external I/O
1	LNCPUCTL	R/W	0 1	Standard Drive 33% Drive on CPU control signals
0	LNAD/ DATA	R/W	0 1	Standard Drive 33% drive on A10–A0, D7–D0

Memory Management Unit (MMU)

The Z8X180 features an on-chip MMU which performs the translation of the CPU 64KB (16-bit addresses 0000H to FFFFH) logical memory address space into a 1024KB (20-bit addresses 00000H to FFFFFH) physical memory address space. Address translation occurs internally in parallel with other CPU operation.

Logical Address Spaces

The 64KB CPU logical address space is interpreted by the MMU as consisting of up to three separate logical address areas, Common Area 0, Bank Area, and Common Area 1.

As depicted in Figure 23, a variety of logical memory configurations are possible. The boundaries between the Common and Bank Areas can be programmed with 4KB resolution.

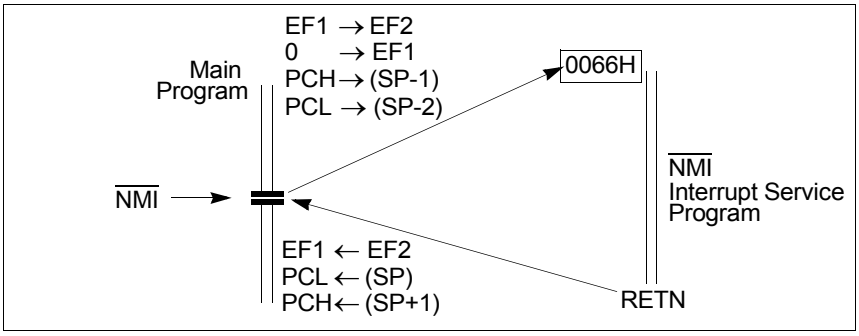

Figure 34. NMI Use

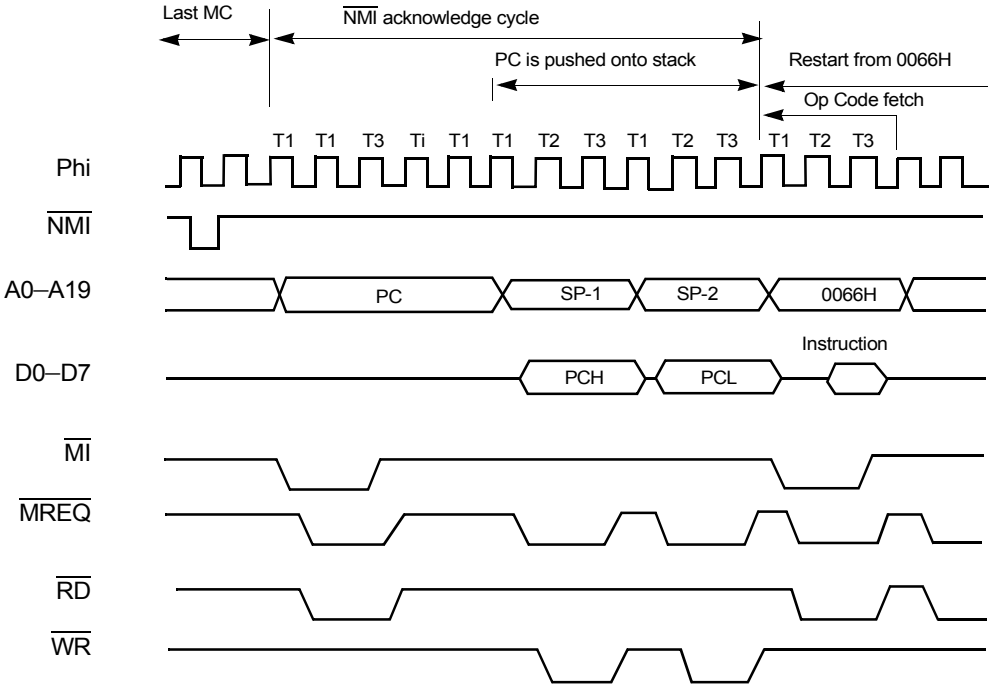

Table 11. DRAM Refresh Intervals

CYC1	CYC0	Insertion Interval	Time Interval				
			10 MHz	8 MHz	6 MHz	4 MHz	2.5 MHz
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.8 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

* Calculated interval

Refresh Control And RESET

After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of ten clock cycles and are three clock cycles in duration.

Dynamic Ram Refresh Operation Notes

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   - During RESET
   - When the bus is released in response to $\overline{\text{BUSREQ}}$
   - During SLEEP mode
   - During Wait States
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. Thus, the time at which the first refresh cycle occurs after the Z8X180 re-acquires the bus depends on the refresh timer and has no timing relationship with the bus exchange.

memory mapped I/O. transfers, the CKA0/$\overline{\text{DREQ0}}$ pin automatically functions as input pin or output pin even if it has been programmed as output pin for CKA0. And the CKA1/$\overline{\text{TEND0}}$ pin functions as an input or an output pin for $\overline{\text{TEND0}}$ by setting CKA1D to 1 in CNTLA1.

To initiate memory to/from I/O (and memory to/from memory mapped I/O) DMA transfer for channel 0, perform the following operations:

1. Load the memory and I/O or memory mapped I/O source and destination addresses into SAR0 and DAR0.

   I/O addresses (not memory mapped I/O are limited to 16 bits (A0–A15). Make sure that bits A16, A17 and A19 are 0 (A18 is a don't care) to correctly enable the external $\overline{\text{DREQ0}}$ input.

2. Specify memory to/from I/O or memory to/from memory mapped I/O mode and address increment/decrement in the SM0, SM1, DM0 and DM1 bits of DMODE.

3. Load the number of bytes to transfer in BCR0.

4. Specify whether $\overline{\text{DREQ0}}$ is edge- or level-sense by programming the DMS0 bit of DCNTL.

5. Enable or disable DMA termination interrupt with the DIE0 bit in DSTAT.

6. Program DE0: = 1 (with $\overline{\text{DWEO}}$ = 0 in the same access) in DSTAT and the DMA operation begins under the control of the $\overline{\text{DREQ0}}$ input.

Memory to ASCI - Channel 0

Channel 0 has extra capability to support DMA transfer to/from the on-chip two channel ASCI. In this case, the external $\overline{\text{DREQ0}}$ input is not used for DMA timing. Rather, the ASCI status bits are used to generate an internal $\overline{\text{DREQ0}}$ The TDRE (Transmit Data Register Empty) bit and the RDRF (Receive Data Register Full) bit are used to generate an internal

ASCI Control Register B 0 (CNTLB0: 02H)
ASCI Control Register B 1 (CNTLB1: 03H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	MPBT	MP	$\overline{\text{CTS}}$/PS	PE0	DR	SS2	SS1	SS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	0	0	0	0	1	1	1

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	MPBT	R/W		**Multiprocessor Bit Transmit** — When multiprocessor communication format is selected (MP bit is 1), MPBT is used to specify the MPB data bit for transmission. If MPBT is 1, then MPB = 1 is transmitted. If MPBT is 0, then MPBT = 0 is transmitted. MPBT state is undefined during and after RESET.
6	MP	R/W		**Multiprocessor Mode** — When MP is set to 1, the data format is configured for multiprocessor mode based on the MOD2 (number of data bits) and MOD0 (number of stop bits) bits in CNTLA. The format is as follows. Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits Multiprocessor (MP = 1) format has no provision for parity. If MP is 0, the data format is based on MOD0 MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

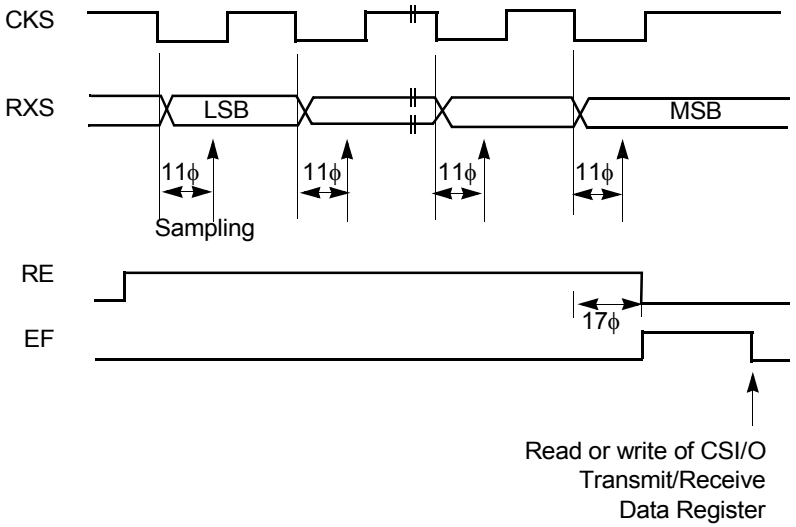

Figure 61. CSI/O Receive Timing–Internal Clock

control register. The PRT input clock for both channels is equal to the system clock divided by 20.

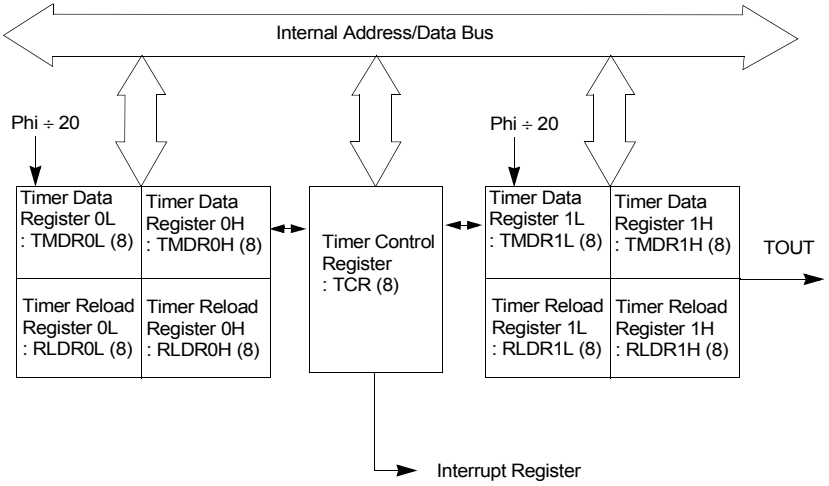

Figure 63. PRT Block Diagram

PRT Register Description

Timer Data Register (TMDR: I/O Address - CH0: 0CH, 0DH; CH1: 15H, 14H). PRT0 and PRT1 each contain 16-bit timer Data Registers (TMDR). TMDR0 and TMDR1 are each accessed as low and high byte registers (TMDR0H, TMDR0L and TMDR1H, TMDR1L). During RESET, TMDR0 and TMDR1 are set to FFFFH.

TMDR is decremented once every twenty clocks. When TMDR counts down to 0, it is automatically reloaded with the value contained in the Reload Register (RLDR).

TMDR is read and written by software using the following procedures. The read procedure uses a PRT internal temporary storage register to

These devices require connection with the Z8X180 synchronous E clock output. The speed (access time) required for the peripheral devices are determined by the Z8X180 clock rate. Table 24, and Figure 67 through Figure 70 define E clock output timing.

Wait States are inserted in Op Code fetch, memory read/write, and I/O read/write cycles which extend the duration of E clock output High. During I/O read/write cycles with no Wait States (only occurs during on-chip I/O register accesses), E does not go High.

Table 24. E Clock Timing in Each Condition

Condition	**Duration of E Clock Output High**	
Op Code Fetch Cycle Memory Read/Write Cycle	T2 rise - T3 fall	(1.5 Phi + nw x Phi)
I/O read Cycle	1st Tw rise - T3 fall	(0.5Phi + nw x Phi)
I/O Write Cycle	1st Tw rise - T3 rise	In_w x Phi)
$\overline{NMI}$ Acknowledge 1st MC	T2 rise - T3 fall	(1.5 Phi)
$\overline{INT0}$ Acknowledge 1st MC	1st Tw rise - T3 fall	(0.50 + nw x Phi)
BUS RELEASE mode SLEEP mode SYSTEM STOP mode	Phi fall - Phi fall	(2 Phi or 1 Phi)
Note: nw = the number of Wait States; MC: Machine Cycle		

TST (HL) - Test Memory

The contents of memory pointed to by HL are ANDed with the accumulator (A) and the status flags are updated. The memory contents and accumulator are not changed (non-destructive AND).

INO g, (m) - Input, Immediate I/O address

The contents of immediately specified 8-bit I/O address are input into the specified register. When I/O is accessed, `00H` is output in high-order bits of the address automatically.

OUTO (m), g - Output, Immediate I/O address

The contents of the specified register are output to the immediately specified 8-bit I/O address. When I/O is accessed, 00H is output in high-order bits of the address automatically.

CPU REGISTERS

The Z80180 CPU registers consist of Register Set GR, Register Set GR' and Special Registers.

The Register Set GR consists of 8-bit Accumulator (A), 8-bit Flag Register (F), and three General Purpose Registers (BC, DE, and HL) which may be treated as 16-bit registers (BC, DE, and HL) or as individual 8-bit registers (B, C, D, E, H, and L) depending on the instruction to be executed. The Register Set GR' is alternate register set of Register Set GR and also contains Accumulator (A'), Flag Register (F') and three General Purpose Registers (BC', DE', and HL'). While the alternate Register Set GR' contents are not directly accessible, the contents can be programmably exchanged at high speed with those of Register Set GR.

The Special Registers consist of 8-bit Interrupt Vector Register (I), 8-bit R Counter (R), two 16-bit Index Registers (IX and IY), 16-bit Stack Pointer (SP), and 16-bit Program Counter (PC)

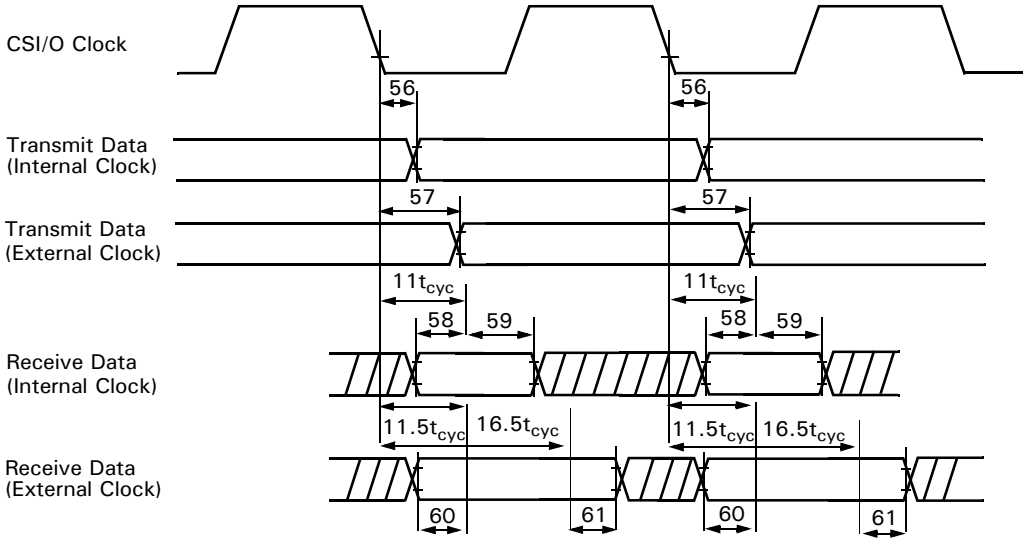

Figure 90. CSI/O Receive/Transmit Timing Diagram

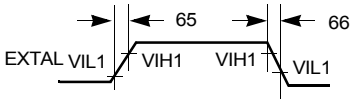

Figure 91. External Clock Rise Time and Fall Time

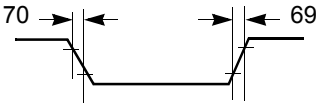

Figure 92. Input Rise Time and Fall Time (Except EXTAL, $\overline{\text{RESET}}$)

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
DEC	DEC g	00 g 101				S/D				1	4	gr-1→gr	↑	↑	↑	V	S	•
	DEC (HL)	00 110 101					S/D			1	10	$(HL)_M$-1→$(HL)_M$	↑	↑	↑	V	S	•
	DEC (IX + d)	11 011 101			S/D					3	18	$(IX + d))_M$-I→	↑	↑	↑	V	S	•
		00 110 101										$(IX + d))_M$						
		<d>																
	DEC (IY + d)	11 111 101			S/D					3	18	$(IY + d)_M$-1→	↑	↑	↑	V	S	•
		00 1101 01										$(IY + d)_M$						
		<d>																
INC	INC g	00 g 100				S/D				1	4	gr + I→gr	↑	↑	↑	V	R	•
	INC (HL)	00 110 100					S/D			1	10	$(HL)_M$ + I→$(HL)_M$	↑	↑	↑	V	R	•
	INC (IX + d)	11 011 101			S/D					3	18	$(IX + d))_M$ + 1→	↑	↑	↑	V	R	•
		00 110 100										$(1X + d))_M$						
		<d>																
	INC (IY + d)	11 111 101			S/D					3	18	(IY + d)v + 1→	↑	↑	↑	V	R	•
		00 110 100										(IY + d)v						
		<d>																
MULT	MLT ww**	11 101 101				S/D				2	17	wwHr→wwLr→wwI	•	•	•	•	•	•
		01 WWI 100																
NEGATE	NEG	11 101 101						S/D		2	6	0-Ar→Ar	↑	↑	↑	Y	S	↑
		01 000 100																

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
OR	OR g	10 110 g				S		D		1	4	Ar + gr→Ar	↑	↑	R	P	R	R
	OR (HL)	10 110 110					S	D		1	6	Ar + $(HL)_M$→Ar	↑	↑	R	P	R	R
	OR m	11 110 110	S					D		2	6	Ar + m→Ar	↑	↑	R	P	R	R
		<m>																
	OR (IX + d)	11 011 101			S			D		3	14	Ar + $(IX + d)_M$→Ar	↑	↑	R	P	R	R
		10 110 110																
		<d>																
	OR (IY + d)	11 111 101			S			D		3	14	Ar + $(IY + d)_M$→Ar	↑	↑	R	P	R	R
		10 110 110																
		<d>																
SUB	SUB g	10 010 g				S		D		1	4	Ar-gr→Ar	↑	↑	↑	V	S	↑
	SUB (HL)	10 010 110					S	D		1	6	Ar-$(HL)_M$→Ar	↑	↑	↑	V	S	↑
	SUB m	11 010 110	S					D		2	6	Ar-m→Ar	↑	↑	↑	V	S	↑
		<m>																
	SUB (IX + d)	11 011 101			S			D		3	14	Ar-$(IX + d)_M$-c→Ar	↑	↑	↑	V	S	↑
		10 011 110																
		<d>																
	SUB (IY + d)	11 111 101			S			D		3	14	Ar-$(IY + d)_M$-c→Ar	↑	↑	↑	V	S	↑
		10 010 110																
		<d>																

MNEMONICS	Bytes	Machine Cycles	States
SRL (IY+d)	4	7	19
SRL g	2	3	7
SUB (HL)	1	2	6
SUB (IX+d)	3	6	14
SUB (IY+d)	3	6	14
SUB m	2	2	6
SUB g	1	2	4
**TSTIO m	3	4	12
**TST g	2	3	7
TST m**	3	3	9
TST (HL)**	2	4	10
XOR (HL)	1	2	6
XOR (IX+d)	3	6	14
XOR (IY+d)	3	6	14
XOR m	2	2	6
XOR g	1	2	4

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (mn),IX LD (mn),IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	Ti	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	mn	IXL IYL	1	0	0	1	1	1	1
	MC7	T1T2T3	mn+1	IXH IYH	1	0	0	1	1	1	1
LD SP, HL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
LD SP,IX LD SP,IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
LDI LDD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LDIR LDDR (If BCR≠0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1
	MC5~MC6	TiTi	*	Z	1	1	1	1	1	1	1
LDIR LDDR (If BCR=0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1
MLT ww**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC13	TiTiTTi TiTiTiTi TiTiTi	*	Z	1	1	1	1	1	1	1
NEG	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
NOP	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Status Channel 0:	STAT0	0	4	

bit	RDRF	OVRN	PE	FE	RIE	$\overline{DCD0}$	TDRE	TIE
during RESET	0	0	0	0	invalid	*	**	0
R/W	R	R	R	R	R/W	R	R	R/W

Transmit Interrupt Enable
Transmit Data Register Empty
Data Carrier Detect
Receive Interrupt Enable
Framing Error
Parity Error
Overrun Error
Receive Data Register Full

** $\overline{CTS_0}$ Pin	TDRE
L	1
H	0

* $\overline{DCD_0}$: Depending on the condition of $\overline{DCD_0}$ Pin.

ASCI Status Channel 1:	STAT1	0	5

bit	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
during RESET	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R/W	R	R	R/W

Transmit Interrupt Enable
Transmit Data Register Empty
$\overline{CTS1}$ Enable
Receive Interrupt Enable
Framing Error
Parity Error
Overrun Error
Receive Data Register Full