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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006peg

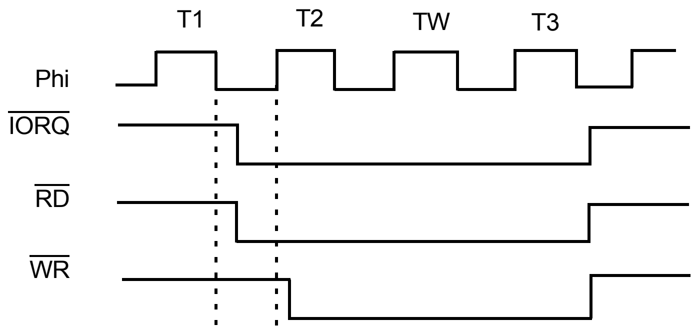


Figure 7. I/O Read and Write Cycles with $\overline{\text{IOC}}$ = 1 Timing Diagram

When $\overline{\text{IOC}}$ is `0`, the timing of the $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals match the timing required by the Z80 family of peripherals. The $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals go active as a result of the rising edge of T2. This timing allows the Z8X180 to satisfy the setup times required by the Z80 peripherals on those two signals (Figure).

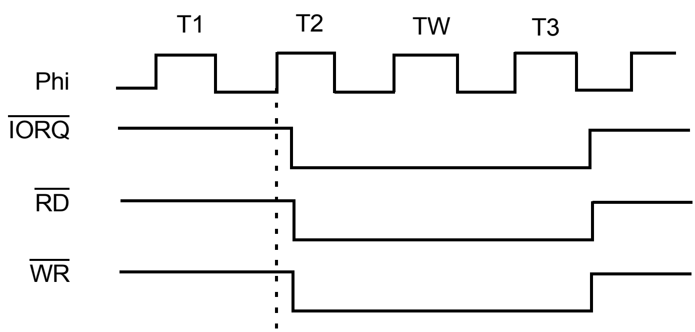


Figure 8. I/O Read and Write cycles with IOC = 0 Timing Diagram

For the remainder of this document, assume that M1E is `0` and $\overline{\text{IOC}}$ is `0`.

address to 0. These instructions are IN0, OUT0, OTIM, OTIMR, OTDM, OTDMR and TSTIO (see Instruction Set).

When writing to an internal I/O register, the same I/O write occurs on the external bus. However, the duplicate external I/O write cycle exhibits internal I/O write cycle timing. For example, the $\overline{WAIT}$ input and programmable Wait State generator are ignored. Similarly, internal I/O read cycles also cause a duplicate external I/O read cycle. However, the external read data is ignored by the Z8X180.

Normally, external I/O addresses should be chosen to avoid overlap with internal I/O addresses and duplicate I/O accesses.

Table 6. I/O Address Map for Z80180-Class Processors Only

			Address		
	Register	**Mnemonic**	**Binary**	**Hex**	**Page**
ASCI	ASCI Control Register A Ch 0	CNTLA0	XX000000	00H	125
	ASCI Control Register A Ch 1	CNTLA1	XX000001	01H	128
	ASCI Control Register B Ch 0	CNTLB0	XX000010	02H	132
	ASCI Control Register B Ch 1	CNTLB1	XX000011	03H	132
	ASCI Status Register Ch 0	STAT0	XX000100	04H	120
	ASCI Status Register Ch 1	STAT1	XX000101	05H	123
	ASCI Transmit Data Register Ch 0	TDR0	XX000110	06H	118
	ASCI Transmit Data Register Ch 1	TDR1	XX000111	07H	118
	ASCI Receive Data Register Ch 0	RDR0	XX001000	08H	119
	ASCI Receive Data Register Ch 1	RDR1	XX001001	09H	119
CSI/O	CSI/O Control Register	CNTR	XX001010	0AH	147
	CSI/O Transmit/Receive Data Register	TRD	XX1011	0BH	149

Table 6. I/O Address Map for Z80180-Class Processors Only (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
INT	IL Register (Interrupt Vector Low Register)	IL	XX110011	33H	67
	INT/TRAP Control Register	ITC	XX110100	34H	68
	Reserved		XX110101	35H	
Refresh	Refresh Control Register	RCR	XX110110	36H	88
	Reserved		XX110111	37H	
MMU	MMU Common Base Register	CBR	XX111000	38H	61
	MMU Bank Base Register	BBR	XX111001	39H	62
	MMU Common/Bank Area Register	CBAR	XX111010	3AH	60
I/O	Reserved		XX111011	3BH	
			⇕	⇕	
			XX111101	3DH	
	Operation Mode Control Register	OMCR	XX111110	3EH	15
	I/O Control Register	ICR	XX111111	3FH	42

CPU Control Register (CCR: 1FH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Clock Divide	STAND BY/ IDLE Enable	BREXT	LNPHI	STAND BY/ IDLE Enable	LNIO	LNCPU CTL	LNAD/ DATA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	Clock Divide	R/W	0 1	XTAL/2 XTAL/1
6	STANDBY /IDLE Mode	R/W	 00 01 10 11	In conjunction with Bit 3 No STANDBY IDLE after SLEEP STANDBY after SLEEP STANDBY after SLEEP 64 Cycle Exit (Quick Recovery)
5	BREXT	R/W	0 1	Ignore BUSREQ in STANDBY/IDLE STANDBY/IDLE exit on BUSREQ
4	LNPHI	R/W	0 1	Standard Drive 33% Drive on EXTPHI Clock
3	STANDBY /IDLE Mode	R/W	 00 01 10 11	In conjunction with Bit 6 No STANDBY IDLE after SLEEP STANDBY after SLEEP STANDBY after SLEEP 64 Cycle Exit (Quick Recovery)

vector table can be relocated on 32 byte boundaries. IL is initialized to `00H` during RESET.

Interrupt Vector Low Register (IL: 33H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	IL7	IL6	IL5	?				
R/W	R/W	R/W	R/W	?				
Reset	00H	00H	00H	?				
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Bit Position	Bit/Field	R/W	Value	Description
7–5	IL7–5	R/W		The IL register is an internal I/O register which is programmed with the OUT0 instruction and can be read using the IN0 instruction.
4–0	?	N/A		Interrupt source dependent code

INT/TRAP Control Register (ITC)

ITC is used to handle TRAP interrupts and to enable or disable the external maskable interrupt inputs $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$.

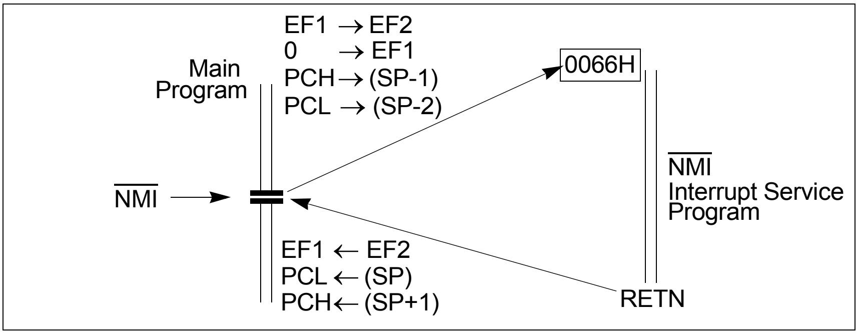
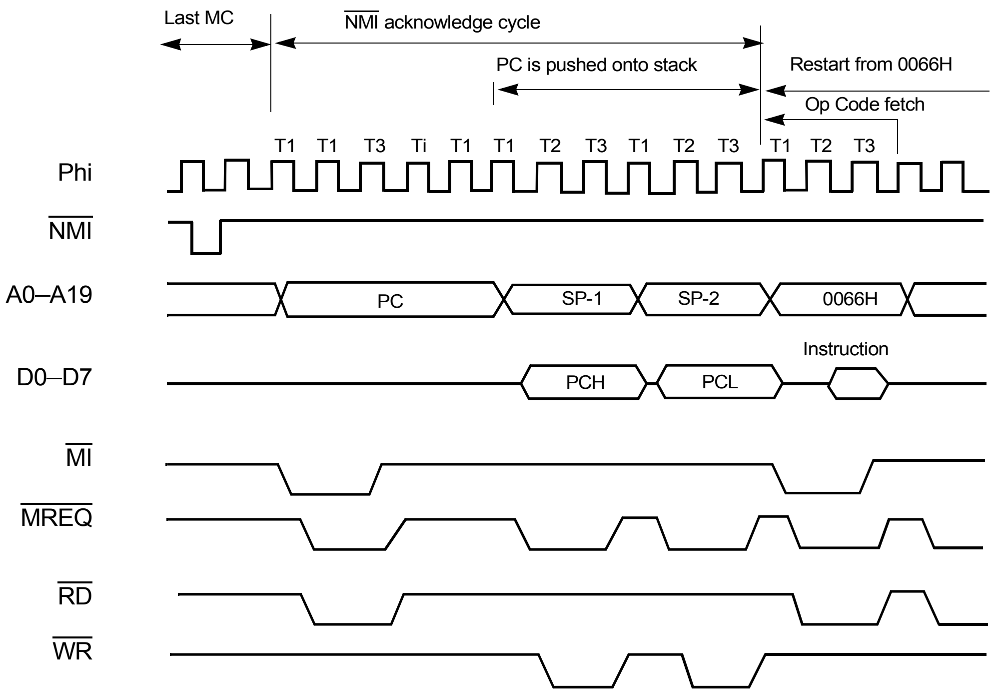


Figure 34. NMI Use



Channel 0

- SAR0–Source Address Register
- DAR0–Destination Address Register
- BCR0–Byte Count Register

Channel 1

- MAR1–Memory Address Register
- IAR1–I/O Address Register
- BCR1–Byte Count Register

The two channels share the following three additional registers in common:

- DSTAT–DMA Status Register
- DMODE–DMA Mode Register
- DCNTL–DMA Control Register

DMAC Block Diagram

Figure 45 depicts the Z8X180 DMAC Block Diagram.

The key functions for ASCI on Z80180, Z8S180 and Z8L180 class processors are listed below. Each channel is independently programmable.

- Full-duplex communication
- 7- or 8-bit data length
- Program controlled 9th data bit for multiprocessor communication
- 1 or 2 stop bits
- Odd, even, no parity
- Parity, overrun, framing error detection
- Programmable baud rate generator, /16 and /64 modes
- Modem control signals – Channel 0 contains $\overline{\text{DCD0}}$, $\overline{\text{CTS0}}$ and $\overline{\text{RTS0}}$; Channel 1 contains $\overline{\text{CTS1}}$
- Programmable interrupt condition enable and disable
- Operation with on-chip DMAC

ASCI Block Diagram for the Z8S180/Z8L180-Class Processors

Figure 52 illustrates the ASCI block diagram.

Addressing Modes

The Z80180 instruction set includes eight addressing modes.

- Implied Register
- Register Direct
- Register Indirect
- Indexed
- Extended
- Immediate
- Relative
- IO

Implied Register (IMP)

Certain Op Codes automatically imply register usage, such as the arithmetic operations that inherently reference the Accumulator, Index Registers, Stack Pointer, and General Purpose Registers.

Register Direct (REG)

Many Op Codes contain bit fields specifying registers used for operation. The exact bit field definitions vary depending on instruction depicted in Figure 75.

Z80180 DC CHARACTERISTICS

V_{CC} = 5V ± 10%, V_{SS} = OV, Ta = 0° to +70°C, unless otherwise noted.)

Table 28. Z80180 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VIH1	Input High Voltage $\overline{\text{RESET}}$, EXTAL $\overline{\text{NMI}}$		V_{CC} –0.6	–	V_{CC} +0.3	V
VIH2	Input High Voltage except $\overline{\text{RESET}}$, EXTAL $\overline{\text{NMI}}$		2.0		V_{CC} +0.3	V
VIL1	Input Low Voltage $\overline{\text{RESET}}$, EXTAL $\overline{\text{NMI}}$		–0.3		0.6	V
VIL2	Input Low Voltage except $\overline{\text{RESET}}$, EXTAL $\overline{\text{NMI}}$		–0.3		0.8 Standard 7 TL_{VIL}	V
VOH	Output High Voltage all outputs	IOH = –200 µA IOH = –20 µA	2.4 V_{CC} –1.2	– –	– –	V V
VOL	Output Low Voltage all outputs	IOL = 2.2 mA	–	–	0.45	V
I_{IL}	Input Leakage Current all inputs except XTAL, EXTAL	V_{IN} = 0.5~ V_{CC} –0.5	–	–	1.0	µA
ITL	Three-State Leakage Current		–	–	1.0	µA
ICC	Power Dissipation* (Normal Operation)	f = 6 MHz f = 8 MHz f = 33 MHz	– – –	15 20 25	40 50 60	mA mA mA

Table 28. Z80180 DC Characteristics (Continued)

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
	Power Dissipation* (SYSTEM STOP mode)	f = 6 MHz f = 8 MHz f = 33 MHz	– – –	3.8 5 6.3	12.5 15.0 17.5	mA mA mA
CP	Pin Capacitance	VIN = 0V, f = 1MHz TA = 25°C	–	–	12	pF
Notes: * VIN min = V_{CC} –1.0V. VIL max = 0.8V (All output terminals are a no load.) V_{CC} = 5.0V						

Z8S180 DC CHARACTERISTICS

V_{CC} = 5V ± 10%, V_{SS} = OV, Ta = 0° to +70°C, unless otherwise noted.

Table 29. Z8S180 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VIH1	Input High Voltage $\overline{\text{RESET}}$, EXTAL $\overline{\text{NMI}}$		V_{CC} –0.6	–	V_{CC} +0.3	V
VIH2	Input High Voltage except $\overline{\text{RESET}}$, EXTAL $\overline{\text{NMI}}$		2.0		V_{CC} +0.3	V
VIH3	Input High Voltage CKS, CKA0, CKA1		2.4		V_{DD} + 0.3	V
VIL1	Input Low Voltage $\overline{\text{RESET}}$, EXTAL $\overline{\text{NMI}}$		–0.3		0.6	V
VIL2	Input Low Voltage except $\overline{\text{RESET}}$, EXTAL $\overline{\text{NMI}}$		–0.3		0.8	V

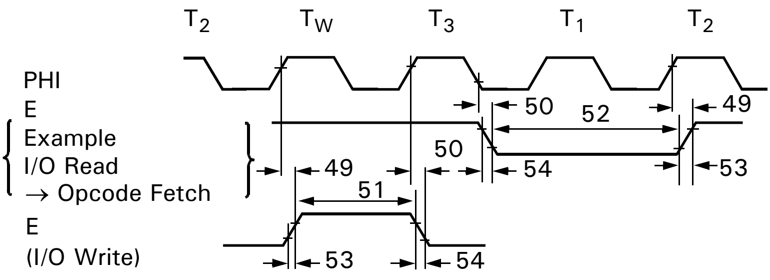


Figure 87. E Clock Timing (Minimum Timing Example of PWEL and PWEH)

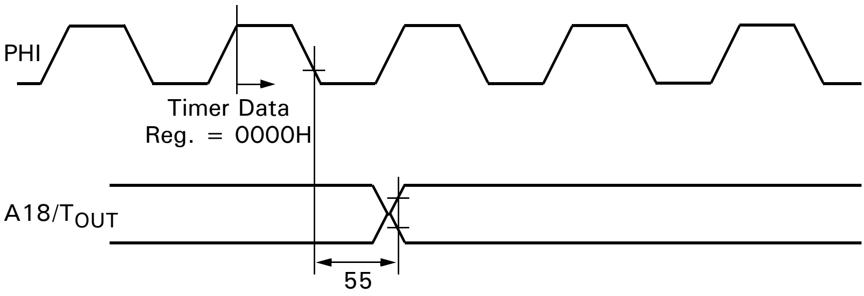


Figure 88. Timer Output Timing

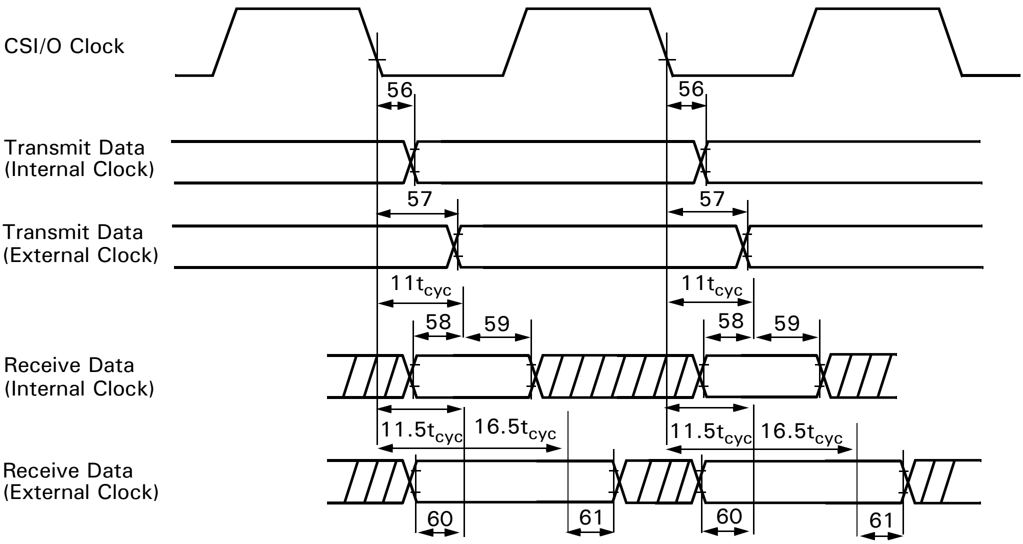


Figure 90. CSI/O Receive/Transmit Timing Diagram

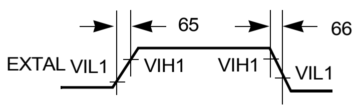


Figure 91. External Clock Rise Time and Fall Time

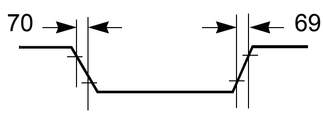


Figure 92. Input Rise Time and Fall Time (Except EXTAL, $\overline{\text{RESET}}$)

MISCELLANEOUS

Table 37 lists the operations mnemonics.

Table 37. Operations Mnemonics

$(\ )_M$	Data in the memory address
$(\ )_I$	Data in the I/O address
m or n	8-bit data
mn	16-bit data
r	8-bit register
R	16-bit register
$b.(\ )_M$	A content of bit b in the memory address
b.gr	A content of bit b in the register gr
d or j	8-bit signed displacement
S	Source
D	Destination
•	AND operation
+	OR operation
⊕	EXCLUSIVE OR operation
**	Added new instructions to Z80

Instruction Summary

** : Added new instructions to Z80

MNEMONICS	Bytes	Machine Cycles	States
ADC A,m	2	2	6
ADC A,g	1	2	4
ADC A, (HL)	1	2	6
ADC A, (IX+d)	3	6	14
ADC A, (IY+d)	3	6	14
ADD A,m	2	2	6
ADD A,g	1	2	4
ADD A, (HL)	1	2	6
ADD A, (IX+d)	3	6	14
ADD A, (IY+d)	3	6	14
ADC HL,ww	2	6	10
ADD HL,ww	1	5	7
ADD IX,xx	2	6	10
ADD IY,yy	2	6	10
AND m	2	2	6
AND g	1	2	4
AND (HL)	1	2	6
AND (IX+d)	3	6	14
AND (IY+d)	3	6	14
BIT b, HU	2	3	9
BIT b, (IX+d)	4	5	15
BIT b, (IY+d)	4	5	15
BIT b,g	2	2	6
CALL f,mn	3	2	6 (If condition is false)

Op Code Map

Table 48. 1st Op Code Map Instruction Format: XX

				ww (L0 = ALL)												L0 = 0~7				
				BC	DE	HL	SP									BC	DE	HL	AF	zz
				g (LO = 0~7)												NZ	NC	P0	P	f
				B	D	H	(HL)	B	D	H	(HL)					00H	10H	20H	30H	v
			HI	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
			LO	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
S (HI = ALL)	B	0000	0	N0P	DJNZj	JR NZ,j	JR NC,j				note 1)					RET f				0
	C	0001	1	LD ww, mn				LD g, s				ADD A,s	SUB s	AND s	OR s	POP zz				1
	D	0010	2	LD (ww), A		LD (mn) ,HL	LD (mn), A									JP f, mn				2
	E	0011	3	INC ww												JP mn	OUT (m),A	EX(SP), HL	DI	3
	H	0100	4	INC g			note1									CALL f, mn				4
	L	0101	5	DEC g			note1									PUSH zz				5
	(HL)	0110	6	LD g,m			note1	note2			HALT	note2	note2	note2	note2	ADD A,m	SUB m	AND m	OR m	6
	A	0111	7	RLCA	RLA	DAA	SCF									RST v				7
	B	1000	8	EXAF,A F'	JR j	JR Z,j	JR C,j									RET f				8
	C	1001	9	ADD HL, ww				LD g, s				ADC A,s	SBC A,s	XOR s	CP s	RET	EXX	JP(HL)	LD SP, HL	9
	D	1010	A	LD A,(ww)		LD HL, (mn)	LD A, (mn)									JP f, mn				A
	E	1011	B	DEC ww												Table2	IN A(m)	EXDE,H L	EI	B
	H	1100	C	INC g												CALL f, mn				C
	L	1101	D	DEC g												CALL mn	note3	Table3	note3	D
	(HL)	1110	E	LD g,m				note2				note2	note2	note2	note2	ADC A,m	SBC A,m	XOR m	CP m	E
	A	1111	F	RRCA	RRA	CPL	CCF									RST v				F
				0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
				C	E	L	A	C	E	L	A					Z	C	PE	M	f
				g(L0 = 8~F)												08H	18H	28H	3BH	v
																LO = 8~F				

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{MREQ}}$	$\overline{\text{IORQ}}$	$\overline{\text{M1}}$	$\overline{\text{HALT}}$	ST
LD (mn),IX LD (mn),IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	Ti	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	mn	IXL IYL	1	0	0	1	1	1	1
	MC7	T1T2T3	mn+1	IXH IYH	1	0	0	1	1	1	1
LD SP, HL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
LD SP,IX LD SP,IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
LDI LDD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1

- $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ = 1
  memory to/from (memory mapped)
  I/O DMA transfer
- BCR0, BCR1 = `0000H` (all DMA transfers)
- $\overline{\text{NMI}}$ = 0 (all DMA transfers)

OTHER OPERATION MODE TRANSITIONS

The following operation mode transitions are also possible.

1. HALT $\rightleftarrows$ $\left\{ \begin{array}{l} \text{DMA} \\ \text{REFRESH} \\ \text{BUS RELEASE} \end{array} \right\}$

   IOSTOP $\rightleftarrows$ $\left\{ \begin{array}{l} \text{DMA} \\ \text{REFRESH} \\ \text{BUS RELEASE} \end{array} \right\}$

2. SLEEP $\rightleftarrows$ BUS RELEASE

   SYSTEM STOP $\rightleftarrows$ BUS RELEASE

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)

Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
	CKA0 (External Clock Mode)	Z	IN (A)	IN (N)	IN (N)
	$\overline{\text{DREQ0}}$	Z	IN (N)	IN (A)	IN (N)
TXA1	—	1	OUT	H	H
RXA1	—	IN (N)	IN (A)	IN (N)	IN (N)
CKA1/$\overline{\text{TEND0}}$	CKA1 (Internal Clock Mode)	Z	OUT	Z	Z
	CKA1 (External Clock Mode)	Z	IN (A)	IN (N)	IN (N)
	$\overline{\text{TEND0}}$	Z	1	OUT	1
TXS	—	1	OUT	H	H
RXS/$\overline{\text{CTS}}_1$	RXS	IN (N)	IN (A)	IN (N)	IN (N)
	$\overline{\text{CTS1}}$	IN (N)	IN (A)	IN (N)	IN (N)
CKS	CKS (Internal Clock Mode)	Z	OUT	1	1
	CKS (External Clock Mode)	Z	IN (A)	Z	Z
$\overline{\text{DREQ}}_1$	—	IN (N)	IN (N)	IN (A)	IN (N)
$\overline{\text{TEND}}_1$	—	1	1	OUT	1
$\overline{\text{HALT}}$	—	1	0	OUT	0
$\overline{\text{RFSH}}$	—	1	1	OUT	1
$\overline{\text{IORQ}}$	—	1	1	OUT	1

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)

Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
$\overline{MREQ}$	—	1	1	OUT	1
E	—	0	E Clock Output	←	←
$\overline{M1}$	—	1	1	OUT	1
$\overline{WR}$	—	1	1	OUT	1
$\overline{RD}$	—	1	1	OUT	1
Phi	—	Phi Clock Output	←	←	←

- 1: HIGH 0: LOW A: Programmable Z: High Impedance
- IN (A): Input (Active) IN (N): Input (Not active) OUT: Output
- H: Holds the previous state
- ←: same as the left