Zilog - Z8018006PSC Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006psc

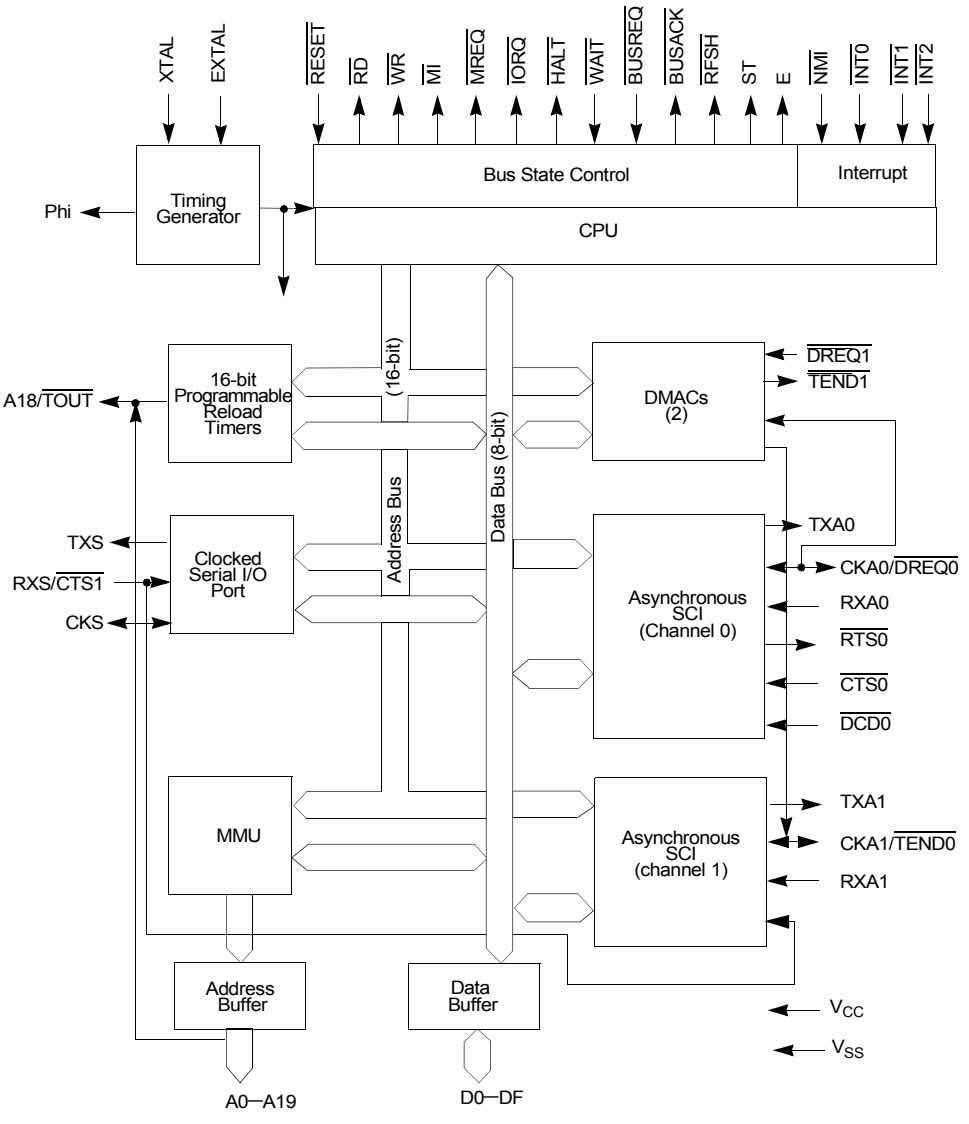

Figure 4. Z80180/Z8S180/Z8L180 Block Diagram

Table 2. Multiplexed Pin Descriptions

Multiplexed Pins	Descriptions
A18/TOUT	During RESET, this pin is initialized as A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, TOUT function is selected. If TOC1 and TOC0 bits are cleared to 0, A18 function is selected.
CKA0/$\overline{\text{DREQ0}}$	During RESET, this pin is initialized as CKA_0 pin. If either DM1 or SM1 in DMA Mode Register (DMODE) is set to 1, $\overline{\text{DREQ0}}$ function is always selected.
CKA1/$\overline{\text{TEND0}}$	During RESET, this pin is initialized as CKA1 pin. If CKA1D bit in ASCI control register ch 1 (CNTLA1) is set to 1, $\overline{\text{TEND0}}$ function is selected. If CKA1D bit is set to 0, CKA1 function is selected.
RXS/$\overline{\text{CTS1}}$	During RESET, this pin is initialized as RXS pin. If CTS1E bit in ASCI status register ch 1 (STAT1) is set to 1, $\overline{\text{CTS1}}$ function is selected. If CTS1E bit is 0, RXS function is selected.

ARCHITECTURE

The Z8X180 combines a high performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller (including dynamic memory refresh), interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks:

- Direct Memory Access (DMA) Control (2 channels)
- Asynchronous Serial Communications Interface (ASCI, 2 channels),

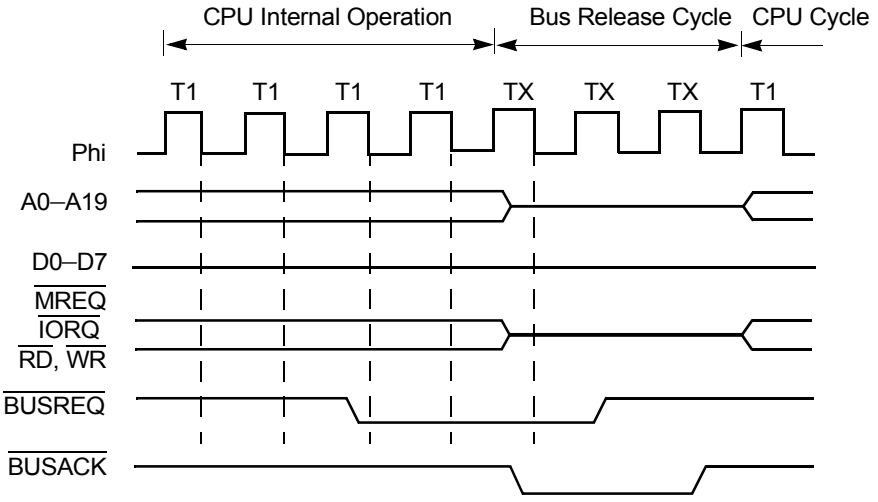

Figure 17. Bus Exchange Timing During CPU Internal Operation

Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z8X180 uses Wait States (TW) to extend bus cycle timing. A Wait State(s) is inserted based on the combined (logical OR) state of the external $\overline{\text{WAIT}}$ input and an internal programmable wait state (TW) generator. Wait States (TW) can be inserted in both CPU execution and DMA transfer cycles.

When the external $\overline{\text{WAIT}}$ input is asserted Low, Wait State(s) (TW) are inserted between T2 and T3 to extend the bus cycle duration. The $\overline{\text{WAIT}}$ input is sampled at the falling edge of the system clock in T2 or TW. If the $\overline{\text{WAIT}}$ input is asserted Low at the falling edge of the system clock in TW, another TW is inserted into the bus cycle.

Note: $\overline{\text{WAIT}}$ input transitions must meet specified setup and hold times. This specification can easily be accomplished by

Low Power Modes (Z8S180/Z8L180 only)

The following section is a detailed description of the enhancements to the Z8S180/L180 from the standard Z80180 in the areas of STANDBY, IDLE and STANDBY QUICK RECOVERY modes.

Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce current consumption. The Z8S180 features two additional power-down modes, STANDBY and IDLE, to reduce current consumption even further. The differences in these power-down modes are summarized in Table 5.

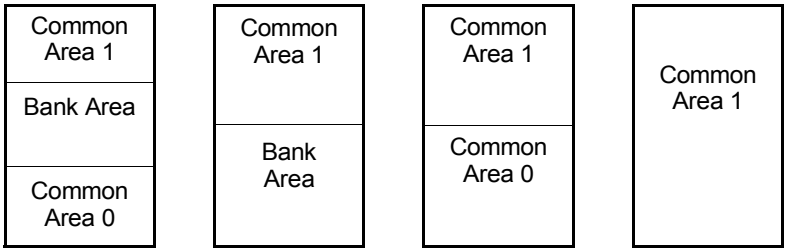

Figure 23. Logical Address Mapping Examples

Logical to Physical Address Translation

Figure 24 illustrates an example in which the three logical address space portions are mapped into a 1024KB physical address space. The important points to note are that Common and Bank Areas can overlap and that Common Area 1 and Bank Area can be freely relocated (on 4KB physical address boundaries). Common Area 0 (if it exists) is always based at physical address `00000H`.

individual I/O (PRT, DMAC, CSI/O, ASCI) control register. The lower vector of $\overline{INT1}$ $\overline{INT2}$ and internal interrupt are summarized in Table 9.

Table 9. Vector Table

Interrupt Source	Priority	IL			Fixed Code				
		b7	b6	b5	b4	b3	b2	b1	b0
$\overline{INT1}$	Highest	—	—	—	0	0	0	0	0
$\overline{INT2}$		—	—	—	0	0	0	1	0
PRT channel 0		—	—	—	0	0	1	0	0
PRT channel 1		—	—	—	0	0	1	1	0
DMA channel 0		—	—	—	0	1	0	0	0
DMA channel 1		—	—	—	0	1	0	1	0
CSI/O		—	—	—	0	1	1	0	0
ASCI channel 0	Lowest	—	—	—	0	1	1	1	0
ASCI channel 1		—	—	—	1	0	0	0	0

Interrupt Acknowledge Cycle Timings

Figure 43 illustrates $\overline{INT1}$, $\overline{INT2}$, and internal interrupts timing. $\overline{INT1}$ and $\overline{INT2}$ are sampled at the falling edge of the clock state prior to T2 or T1 in the last machine cycle. If $\overline{INT1}$ or $\overline{INT2}$ is asserted Low at the falling edge of clock state prior to T3 or T1 in the last machine cycle, the interrupt request is accepted.

Refresh Control Register (RCR)

The RCR specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

Refresh Control Register (RCR: 36H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	REFE	REFW	?				CYC1	CYC0
R/W	R/W	R/W	?				R/W	R/W
Reset	1	1	?				0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	REFE	R/W		**REFE: Refresh Enable**
			0	Disables the refresh controller
			1	Enables refresh cycle insertion.
6	REFW	R/W		**Refresh Wait** (bit 6)
			0	Causes the refresh cycle to be two clocks in duration.
			1	Causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW).
1–0	CYC1–0	R/W		**Cycle Interval** — CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. In the case of dynamic RAMs requiring 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET. Refer to Table 11.

DMA/WAIT Control Register (DCNTL: 32H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–6	MWI1–0	R/W		**Memory Wait Insertion** —Specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET. See section on Wait State Generator for details.
5–4	IWI1–0	R/W		**Wait Insertion** — Specifies the number of Wait States introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET. See section on Wait State Generator for details.
3–2	DMS1–0	R/W		**DMA Request Sense** — Specifies the DMA request sense for channel 0 ($\overline{\text{DREQ0}}$) and channel 1 ($\overline{\text{DREQ1}}$) respectively. When reset to 0, the input is level-sense. When set to 1, the input is edge-sense.
1–0	DIM1–0	R/W		**DMA Channel 1 I/O and Memory Mode** — Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. Reference Table 15.

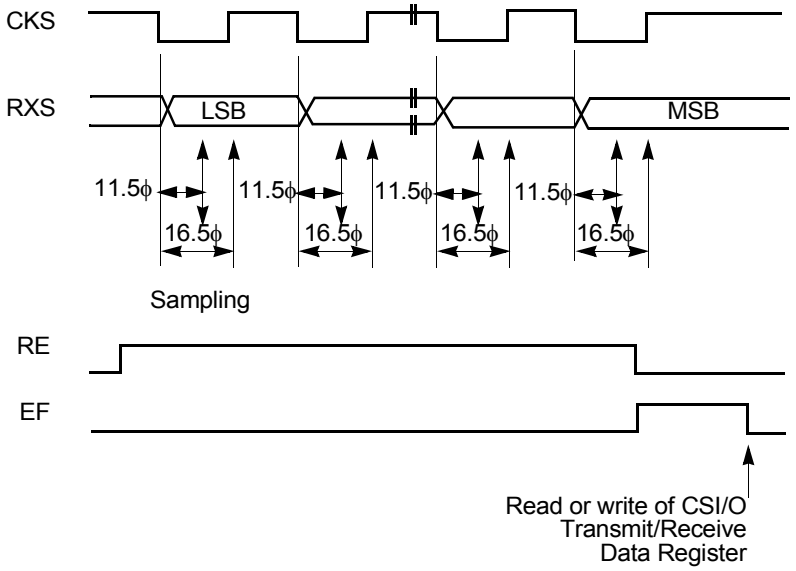

Figure 62. CSI/O Receive Timing–External Clock

Programmable Reload Timer (PRT)

The Z8X180 contains a two channel 16-bit Programmable Reload Timer. Each PRT channel contains a 16-bit down counter and a 16-bit reload register. The down counter is directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. Also, PRT channel 1 features a TOUT output pin (multiplexed with A18) which can be set High, Low, or toggled. Thus, PRT1 can perform programmable output waveform generation.

PRT Block Diagram

The PRT block diagram is depicted in Figure 63. The two channels feature separate timer data and reload registers and a common status/

MLT- Multiply

The MLT performs unsigned multiplication on two 8-bit numbers yielding a 16-bit result. MLT may specify BC, DE, HL, or SP registers. The 8-bit operands are loaded into each half of the 16-bit register and the 16-bit result is returned in that register.

OTIM, OTIMR, OTDM, OTDMR - Block I/O

The contents of memory pointed to by HL is output to the I/O address in (C). The memory address (HL) and I/O address (C) are incremented in OTIM and OTIMR and decremented in OTDM and OTDMR, respectively. The B register is decremented. The OTIMR and OTDMR variants repeat the above sequence until register B is decremented to 0. Since the I/O address (C) is automatically incremented or decremented, these instructions are useful for block I/O (such as Z80180 on-chip I/O) initialization. When I/O is accessed, 00H is output in high-order bits of address automatically.

TSTIO m - Test I/O Port

The contents of the I/O port addressed by C are ANDed with immediately specified 8-bit data and the status flags are updated. The I/O port contents are not written (non-destructive AND). When I/O is accessed, `00H` is output in higher bits of address automatically.

TST g - Test Register

Perform an `AND` instruction on the contents of the specified register with the accumulator (A) and the status flags are updated. The accumulator and specified register are not changed (non-destructive `AND`).

TST m - Test Immediate

Perform an `AND` instruction on the contents of the immediately specified 8-bit data with the accumulator (A) and the status flags are updated. The accumulator is not changed (non-destructive `AND`).

8-bit Register

g or g field '	Register
0	B
0 0 1	C
0 1 0	D
0 1 1	E
1 0 0	H
1 0 1	L
1 1 0	—
1 1 1	A

ww field	Register
0 0	B C
0 1	D E
1 0	H L
1 1	S P

xx field	Register
0 0	B C
0 1	D E
1 0	I X
1 1	S P

16-bit Register

zz field	Register
0 0	B C
0 1	D E
1 0	H L
1 1	A F

yy field	Register
0 0	B C
0 1	D E
1 0	I Y
1 1	S P

Suffixed H and L ww,xx,yy,zz (ex. wwH,IXL) indicate upper and lower 8-bit of the 16-bit register respectively.

Figure 75. Register Direct — Bit Field Definitions

Register Indirect (REG)

The memory operand address is contained in one of the 16-bit General Purpose Registers (BC, DE, and HL) as illustrated in Figure 76.

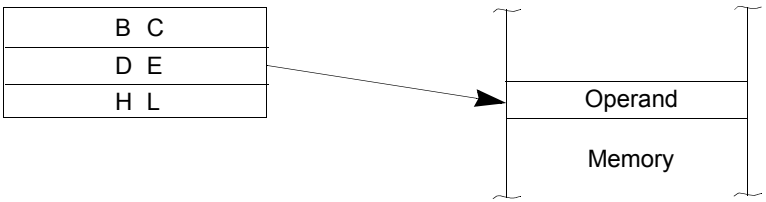

Figure 76. Register Indirect Addressing

Indexed (INDX)

The memory operand address is calculated using the contents of an Index Register (IX or IY) and an 8-bit signed displacement specified in the instruction. Refer to Figure 77

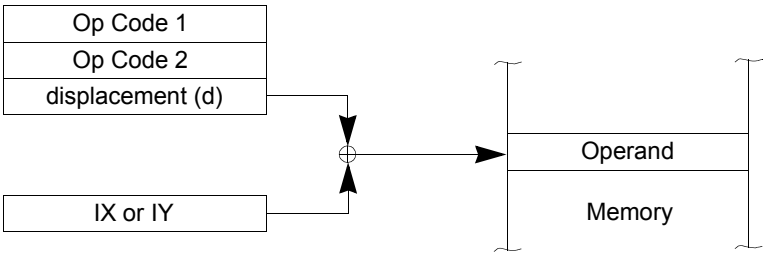

Figure 77. Indexed Addressing

Extended (EXT)

The memory operand address is specified by two bytes contained in the instruction, as depicted in Figure 78.

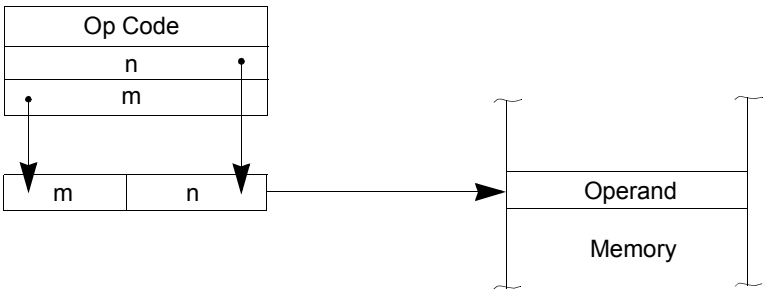

Figure 78. Extended Addressing

STANDARD TEST CONDITIONS

The previous DC Characteristics and Capacitance sections apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows in to the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

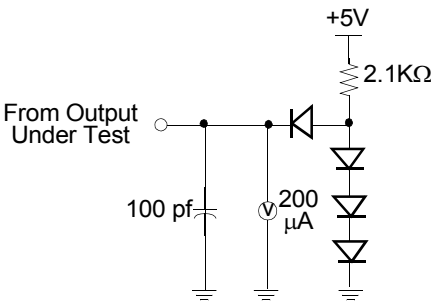

Figure 93. Test Setup

MISCELLANEOUS

Table 37 lists the operations mnemonics.

Table 37. Operations Mnemonics

$( )_M$	Data in the memory address
$( )_I$	Data in the I/O address
m or n	8-bit data
mn	16-bit data
r	8-bit register
R	16-bit register
$b.( )_M$	A content of bit b in the memory address
b.gr	A content of bit b in the register gr
d or j	8-bit signed displacement
S	Source
D	Destination
•	AND operation
+	OR operation
⊕	EXCLUSIVE OR operation
**	Added new instructions to Z80

MNEMONICS	Bytes	Machine Cycles	States
	2	3	7 (if Br = 0)
EI	1	1	3
EX AF,AF'	1	2	4
EX DE,HL	1	1	3
EX (SP),HL	1	6	16
EX (SP)I,IX	2	7	19
EX (SP),IY	2	7	19
EXX	1	1	3
HALT	1	1	3
IM 0	2	2	6
IM 1	2	2	6
IM 2	2	2	6
INC g	1	2	4
INC (HL)	1	4	10
INC (IX+d)	3	8	18
INC (IY+d)	3	8	18
INC ww	1	2	4
INC IX	2	3	7
INC IY	2	3	7
IN A,(m)	2	3	9
IN g,(C)	2	3	9
INI	2	4	12
INIR	2	6	14 (if Br ≠ 0)
	2	4	12 (If Br = 0)
IND	2	4	12
INDR	2	6	14 (If Br ≠ 0)
INDR	2	4	12 (If Br = 0)
IN0 g,(m)**	3	4	12
JP f,mn	3	2	6 (If f is false)

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (IX+d),m LD (IY+d),m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	T1T2T3	IX+ d IY+d	DATA	1	0	0	1	1	1	1
LD A, (BC) LD A, (DE)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	BC DE	DATA	0	1	0	1	1	1	1
LD A,(mn)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	T1T2T3	mn	DATA	0	1	0	1	1	1	1
LD (BC),A LD (DE),A	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	BC DE	A	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (mn),HL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	mn	L	1	0	0	1	1	1	1
	MC6	T1T2T3	mn+1	H	1	0	0	1	1	1	1
LD (mn),ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	Ti	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	mn	wwL	1	0	0	1	1	1	1
	MC7	T1T2T3	mn+1	wwH	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
PUSH IX PUSH IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3~MC4	TiTi	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP-1	IXH IYH	1	0	0	1	1	1	1
	MC6	T1T2T3	SP-2	IXL IYL	1	0	0	1	1	1	1
RET	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC3	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
RET f (If condition is false)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2~MC3	TiTi	*	Z	1	1	1	1	1	1	1
RET f (If condition is true)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
RETI (R0, R1) RETN	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	SP	DATA	0	1	0	1	1	0	1
	MC4	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1

Table 52. Interrupts (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
$\overline{INT0}$ Mode 2	MC1	T1T2TW TWT3	Next Op Code Address (PC)	Vector	1	1	1	0	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP-1	PCH	1	0	0	1	1		1
	MC4	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC5	T1T2T3	I, Vector	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3 T1T2,TW	I, Vector+1	DATA	0	1	0	1	1	1	1
$\overline{INT1}$ $\overline{INT2}$ Internal Interrupts	MC1	T1T2,TW TWT3	Next Op Code Address (PC)		1	1	1	1	1	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC4	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC5	T1T2T3	I, Vector	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3	I, Vector+1	DATA	0	1	0	1	1	1	1

Note: If Bus Request and Refresh Request occur simultaneously, Bus Request is accepted but Refresh Request is cleared.

OPERATION MODE TRANSITION