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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006psg

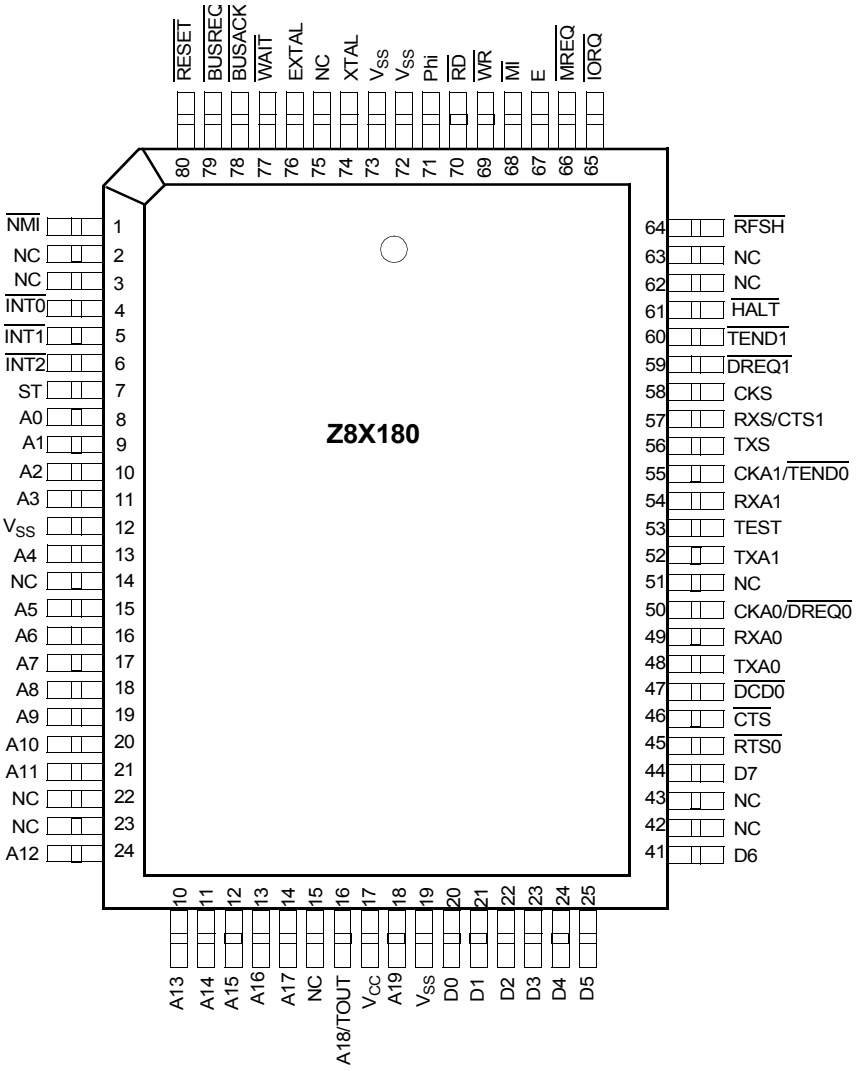

Figure 3. 80-Pin QFP

Wait States (TW) are inserted as previously described for Op Code fetch cycles. Figure 11 illustrates the read/write timing without Wait States (Tw), while Figure 12 illustrates read/write timing with Wait States (TW).

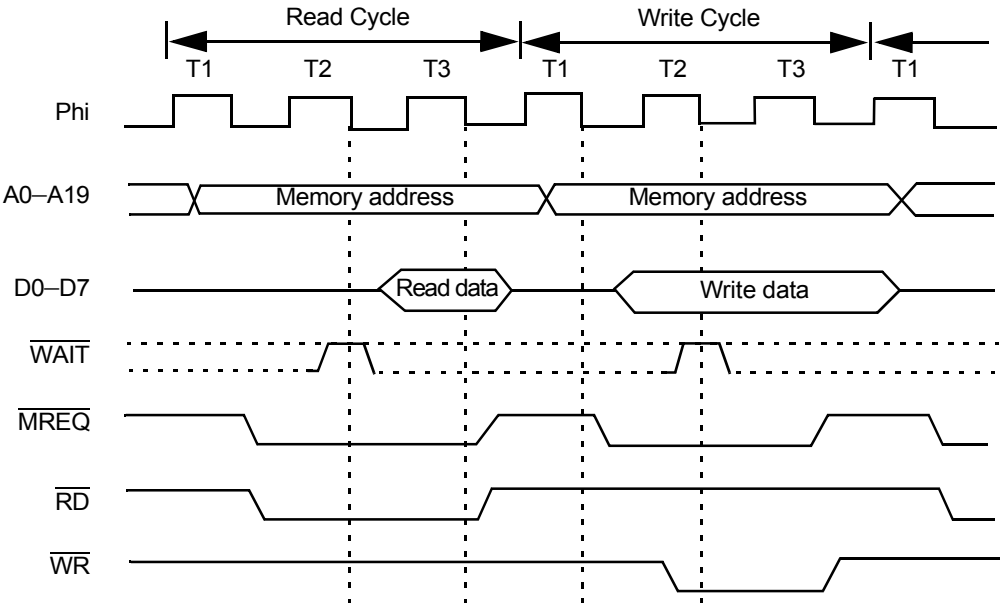

Figure 11. Memory Read/Write (without Wait State) Timing Diagram

When the bus is released, the address (A0–A19), data (D0–D7), and control ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$) signals are placed in the high impedance state.

Dynamic RAM refresh is not performed when the Z8X180 has released the bus. The alternate bus master must provide dynamic memory refreshing if the bus is released for long periods of time.

Figure 16 illustrates $\overline{BUSREQ}$/$\overline{BUSACK}$ bus exchange during a memory read cycle. Figure 17 illustrates bus exchange when the bus release is requested during a Z8X180 CPU internal operation. $\overline{BUSREQ}$ is sampled at the falling edge of the system clock prior to T3, T1 and Tx (BUS RELEASE state). If $\overline{BUSREQ}$ is asserted Low at the falling edge of the clock state prior to Tx, another Tx is executed.

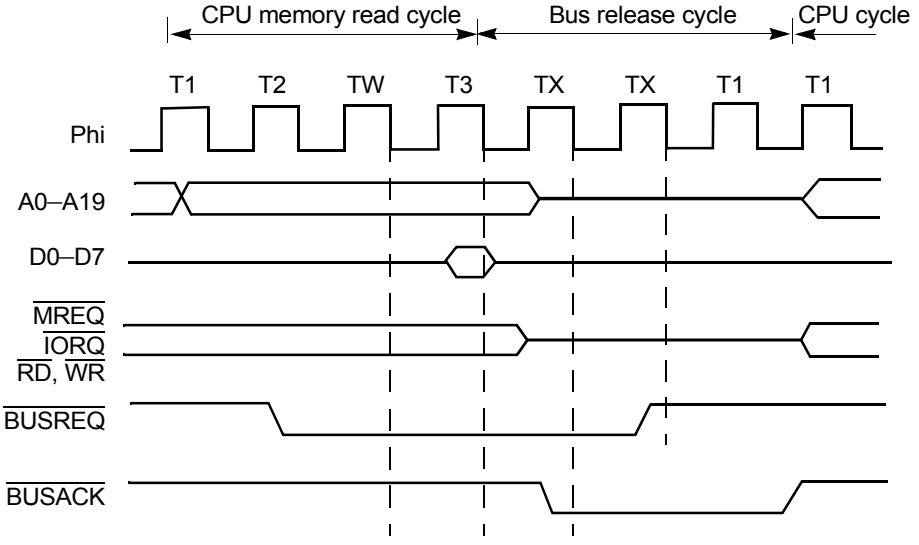

Figure 16. Bus Exchange Timing During Memory Read

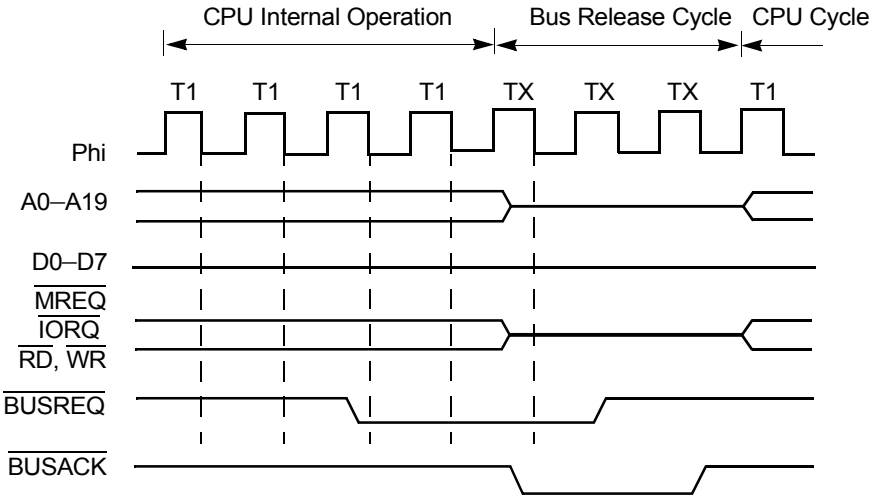

Figure 17. Bus Exchange Timing During CPU Internal Operation

Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z8X180 uses Wait States (TW) to extend bus cycle timing. A Wait State(s) is inserted based on the combined (logical OR) state of the external $\overline{\text{WAIT}}$ input and an internal programmable wait state (TW) generator. Wait States (TW) can be inserted in both CPU execution and DMA transfer cycles.

When the external $\overline{\text{WAIT}}$ input is asserted Low, Wait State(s) (TW) are inserted between T2 and T3 to extend the bus cycle duration. The $\overline{\text{WAIT}}$ input is sampled at the falling edge of the system clock in T2 or TW. If the $\overline{\text{WAIT}}$ input is asserted Low at the falling edge of the system clock in TW, another TW is inserted into the bus cycle.

Note: $\overline{\text{WAIT}}$ input transitions must meet specified setup and hold times. This specification can easily be accomplished by

- The HALT output pin is asserted Low
- The external bus activity consists of repeated dummy fetches of the Op Code following the HALT instruction.

Essentially, the Z80180 operates normally in HALT mode, except that instruction execution is stopped.

HALT mode can be exited in the following two ways:

- $\overline{\text{RESET}}$ Exit from HALT Mode

  If the $\overline{\text{RESET}}$ input is asserted Low for at least six clock cycles, HALT mode is exited and the normal $\overline{\text{RESET}}$ sequence (restart at address `00000H`) is initiated.

- Interrupt Exit from HALT mode

  When an internal or external interrupt is generated, HALT mode is exited and the normal interrupt response sequence is initiated.

If the interrupt source is masked (individually by enable bit, or globally by IEF1 state), the Z80180 remains in HALT mode. However, $\overline{\text{NMI}}$ interrupt initiates the normal $\overline{\text{NMI}}$ interrupt response sequence independent of the state of IEF1.

HALT timing is illustrated in Figure 20.

MMU Register Description

MMU Common/Bank Area Register (CBAR)

CBAR specifies boundaries within the Z8X180 64KB logical address space for up to three areas; Common Area 0, Bank Area and Common Area 1.

MMU Common/Bank Area Register (CBAR: 3AH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–4	CA7–4	R/W		CA specifies the start (low) address (on 4KB boundaries) for the Common Area 1. This also determines the last address of the Bank Area.
3–0	BA3–0	R/W		BA specifies the start (low) address (on 4KB boundaries) for the Bank Area. This also determines the last address of the Common Area 0.

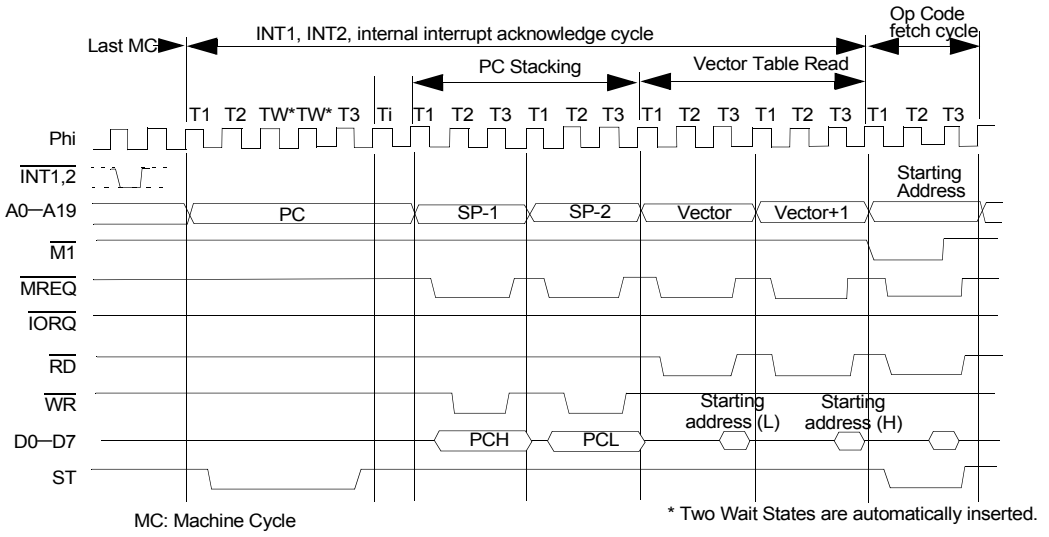

Figure 43. INT1, INT2 and Internal Interrupts Timing Diagram

Dynamic RAM Refresh Control

The Z8X180 incorporates a dynamic RAM refresh control circuit including 8-bit refresh address generation and programmable refresh timing. This circuit generates asynchronous refresh cycles inserted at the programmable interval independent of CPU program execution. For systems which do not use dynamic RAM, the refresh function can be disabled.

When the internal refresh controller determines that a refresh cycle should occur, the current instruction is interrupted at the first breakpoint between machine cycles. The refresh cycle is inserted by placing the refresh address on A0–A7 and the $\overline{\text{RFSH}}$ output is driven Low.

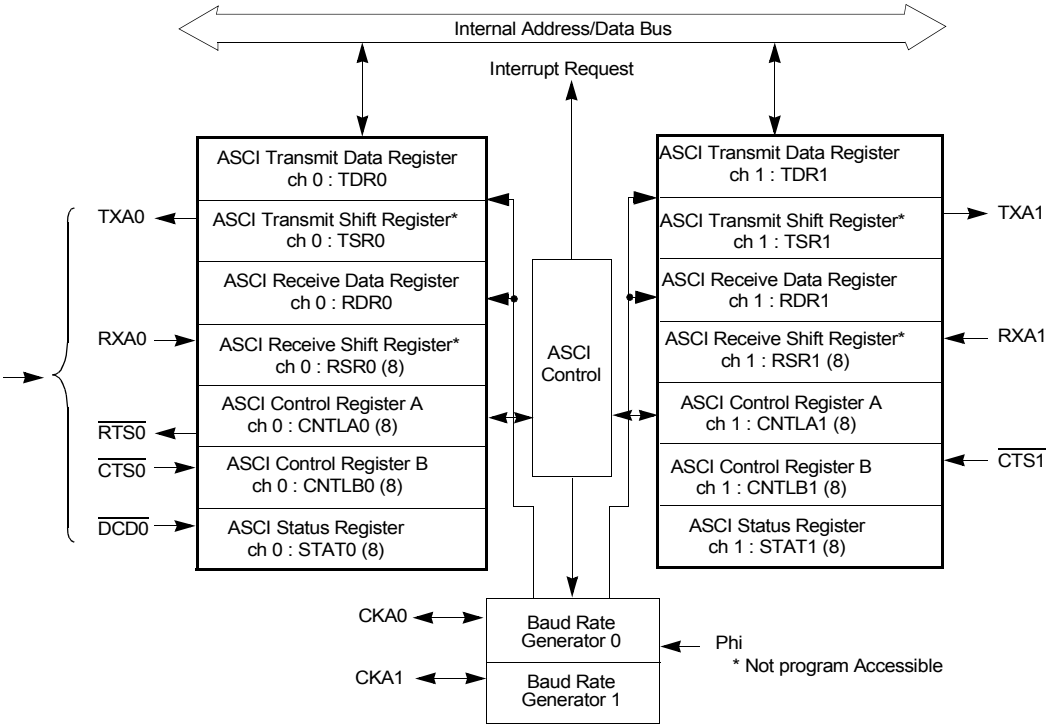

Figure 52. ASCI Block Diagram

ASCI Register Description

The following subparagraphs explain the various functions of the ASCI registers.

ASCI Transmit Shift Register 0, 1 (TSR0, 1)

When the ASCI Transmit Shift Register receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin.

Bit Position	Bit/Field	R/W	Value	Description
2	Break Feature Enable	R/W	0 1	Break Feature Enable On Break Feature Enable Off
1	Break Detect (RO)	R/W	0 1	Break Detect On Break Detect Off
0	Send Break	R/W	0 1	Normal Xmit Drive TXA Low

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

ASCI0 Time Constant Low Register (I/O Address: 1AH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

ASCI0 Time Constant High Register (I/O Address: 1BH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

c. Poll the RE bit in CNTR until RE = 0.

d. Read the receive data from TRDR.

e. Repeat steps 2 to 4 for each receive data byte.

- Receive–Interrupts

a. Poll the RE bit in CNTR until RE is 0.

b. Set the RE and EIE bits in CNTR to 1.

c. When the receive interrupt occurs read the receive data from TRDR.

d. Set the RE bit in CNTR to 1.

e. Repeat steps 3 and 4 for each receive data byte.

CSI/O Operation Timing Notes

- Transmitter clocking and receiver sampling timings are different from internal and external clocking modes. Figure 59 to Figure 62 illustrate CSI/O Transmit/Receive Timing.
- The transmitter and receiver is disabled TE and RE = 0) when initializing or changing the baud rate.

CSI/O Operation Notes

- Disable the transmitter and receiver (TE and RE = 0) before initializing or changing the baud rate. When changing the baud rate after completion of transmission or reception, a delay of at least one bit time is required before baud rate modification.
- When RE or TE is cleared to 0 by software, a corresponding receive or transmit operation is immediately terminated. Normally, TE or RE is only cleared to 0 when EF is 1.
- Simultaneous transmission and reception is not possible. Thus, TE and RE are not both 1 at the same time.

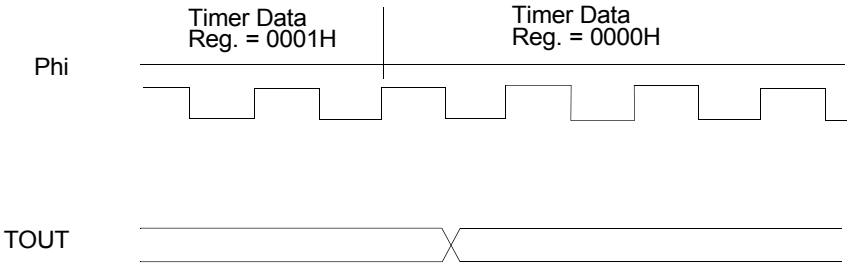

Figure 65. Timer Output Timing Diagram

PRT Interrupts

The PRT interrupt request circuit is illustrated in Figure 66.

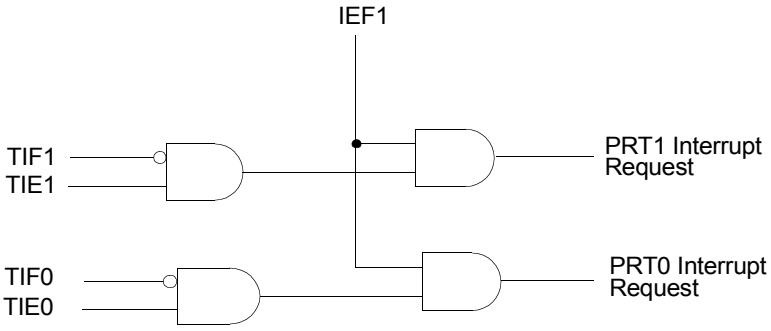

Figure 66. PRT Interrupt Request Generation

PRT and RESET

During RESET, the bits in TCR are initialized as defined in the TCR register description. Down counting is stopped and the TMDR and RLDR registers are initialized to FFFFH. The A18/TOUT pin reverts to the address output function.

Figure 74 depicts CPU register configurations.

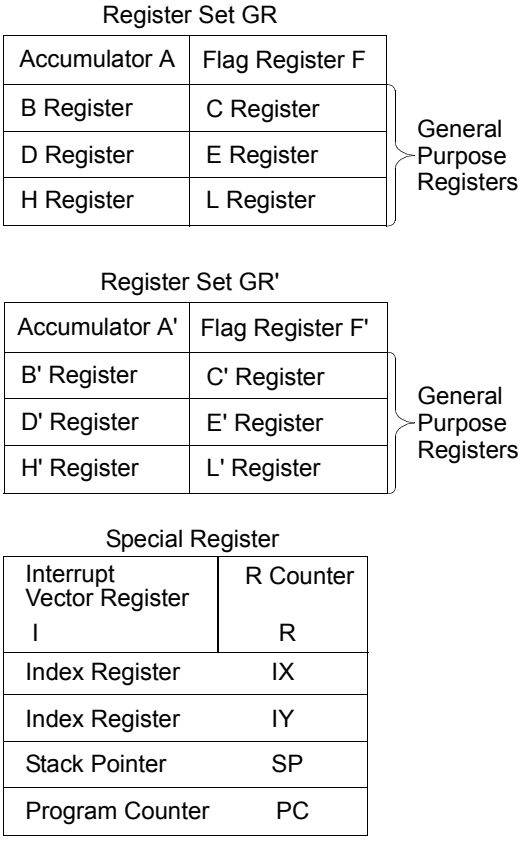

Figure 74. CPU Register Configurations

Accumulator (A, A')

The Accumulator (A) is the primary register used for many arithmetic, logical, and I/O instructions.

Z8L180 DC CHARACTERISTICS

(V_{CC} = 3.3V ± 10%, V_{SS} = OV, Ta = 0° to +70°C, unless otherwise noted.)

Table 30. Z8L180 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VIH1	Input High Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		V_{CC} –0.6	–	V_{CC} +0.3	V
VIH2	Input High Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		2.0		V_{CC} +0.3	V
VIL1	Input Low Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.8	V
VIL2	Input Low Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.8	V
VOH1	Output High Voltage all outputs	IOH = –200 µA	2.4			V
VOH2	Output High Voltage Output High Phi	IOH = –200 µA	V_{CC} –0.6			V
VOL	Output Low Voltage all outputs	IOL = 4 mA	–	–	0.4	V
VOL2	Output Low Voltage Output Low Phi	IOL = 4 mA	–	–	0.4	V
IIL	Input Leakage Current all inputs except XTAL, EXTAL	VIN = 0.5 ~ VCC –0.5	–	–	1.0	µA
ITL	Three-State Leakage Current	VIN = 0.5 ~ VCC –0.5	–	–	1.0	µA

Instruction Set

This section explains the symbols in the instruction set.

REGISTER

g, g', ww, xx, yy, and zz specify a register to be used. g and g' specify an 8-bit register. ww, xx, yy, and zz specify a pair of 8-bit registers. Table 32 describes the correspondence between symbols and registers.

Table 32. Register Values

g,g'	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

ww	Reg.
00	BC
01	DE
10	HL
11	SP

xx	Reg.
00	BC
01	DE
10	IX
11	SP

yy	Reg.
00	BC
01	DE
10	IY
11	SP

zz	Reg.
00	BC
01	DE
10	HL
11	AF

Note: Suffixed H and L to ww, xx, yy, zz (ex. wwH, IXL) indicate upper and lower 8-bit of the 16-bit register respectively.

BIT

b specifies a bit to be manipulated in the bit manipulation instruction. Table 33 indicates the correspondence between **b** and bits.

Table 39. Rotate and Shift Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Bit Reset	RES b,(IY + d)	11 011 101 11 001 01l <d> 10 b 110			S/D					4	19	$0 \rightarrow b \bullet (IY + d)_M$	•	•	•	•	•	•
Bit Test	BIT b, g	11 001 011 01bg				S				2	6	$\overline{b} \bullet \overline{g} r \rightarrow z$	X	↑	S	X	R	•
	BIT b,(HL)	11 001 011 01 b 110					S			2	9	$\overline{b} \bullet \overline{(HL)}_M \rightarrow z$	X	↑	S	X	R	•
	BIT b,(IX + d)	11 011 101 11 001 011 <d> 01 b 110			S					4	15	$\overline{b} \bullet \overline{(IX + d)}_M \rightarrow z$	X	↑	S	X	R	•
	BIT b,(IY + d)	11 111 101 11 001 011 <d> 01 b 110			S					4	15	$\overline{b} \bullet \overline{(IY + d)}_M \rightarrow z$	X	↑	S	X	R	•

MNEMONICS	Bytes	Machine Cycles	States
LD g,g'	1	2	4
LD SP,HL	1	2	4
LD SP,IX	2	3	7
LD SP,IY	2	3	7
MLT ww"	2	13	17
NEG	2	2	6
NOP	1	1	3
OR (HL)	1	2	6
OR (IX+d)	3	6	14
OR (IY+d)	3	6	14
OR m	2	2	6
OR g	1	2	4
OTDM**	2	6	14
OTDMR**	2	8	16 (If Br ≠ 0)
	2	6	14 (If Br = 0)
OTDR	2	6	14 (If Br ≠ 0)
	2	4	12 (If Br = 0
OTIM**	2	6	14
OTIMR**	2	8	16 (If Br ≠ 0)
	2	6	14 (If Br = 0)
OTIR	2	6	14 (If Br ≠ 0)
	2	4	12 (If Br = 0)
OUTD	2	4	12
OUTI	2	4	12
OUT (m),A	2	4	10
OUT (C),g	2	4	10
OUT0 (m),g **	3	5	13
POP IX	2	4	12
POP IY	2	4	12
POP zz	1	3	9

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
CPI CPD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4 ~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
CPIR CPDR (If $BC_R \neq 0$ and $Ar = (HL)_M$)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC8	TiTiTi TiTi	*	Z	1	1	1	1	1	1	1
CPIR CPDR (If $BC_R=0$ or $Ar=(HL)_M$)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
CPL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
DAA	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
DI*1	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
* 1 Interrupt request is not sampled.											

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
INIR INDR (If Br=0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	BC	DATA	0	1	1	0	1	1	1
	MC4	T1T2T3	HL	DATA	1	0	0	1	1	1	1
JP mn	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
JP f,mn (if is false)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
JP f,mn (If f is true)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
JP (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
JP (IX) JP (IY)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
JR j	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	j-2	0	1	0	1	1	1	1
	MC3~MC4	TiTi	*	Z	1	1	1	1	1	1	1
JR C,j JR NC,j JR Z,j JR NZ,j (if condition is false)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	j-2	0	1	0	1	1	1	1
JR C,j JR NC,j JR Z,j JR NZ,j (if condition is true)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	j-2	0	1	0	1	1	1	1
	MC3~MC4	TiTi	*	Z	1	1	1	1	1	1	1
LD g,g'	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
LD g,m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
LD g, (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	HL	DATA	0	1	0	1	1	1	1

Status Signals

PIN OUTPUTS IN EACH OPERATING MODE

Table 55 describes pin outputs in each operating mode.

Table 55. Pin Outputs in Each Operating Mode

Mode		$\overline{M1}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{RD}$	$\overline{WR}$	$\overline{RFSH}$	$\overline{HALT}$	$\overline{BUSACK}$	ST	Address BUS	Data BUS
CPU Operation	Op Code Fetch (1st Op Code)	0	0	1	0	1	1	1	1	0	A	IN
	Op Code Fetch (except 1 st Op Code)	0	0	1	0	1	1	1	1	1	A	IN
	MemRead	1	0	1	0	1	1	1	1	1	A	IN
	Memory Write	1	0	1	1	0	1	1	1	1	A	OUT
	I/O Read	1	1	0	0	1	1	1	1	1	A	IN
	I/O Write	1	1	0	1	0	1	1	1	1	A	OUT
	Internal Operation	1	1	1	1	1	1	1	1	1	A	IN
Refresh		1	0	1	1	1	0	1	1	*	A	IN
Interrupt Acknowledge Cycle (1st Machine Cycle)	$\overline{NMI}$	0	0	1	0	1	1	1	1	0	A	IN
	$\overline{INT0}$	0	1	0	1	1	1	1	1	0	A	IN
	$\overline{INT1}$, $\overline{INT2}$ & Internal Interrupts	1	1	1	1	1	1	1	1	0	A	IN
BUS RELEASE		1	Z	Z	Z	Z	1	1	0	*	Z	IN
HALT		0	0	1	0	1	1	0	1	0	A	IN
SLEEP		1	1	1	1	1	1	0	1	1	1	IN