Zilog - Z8018006VEC Datasheet

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006vec

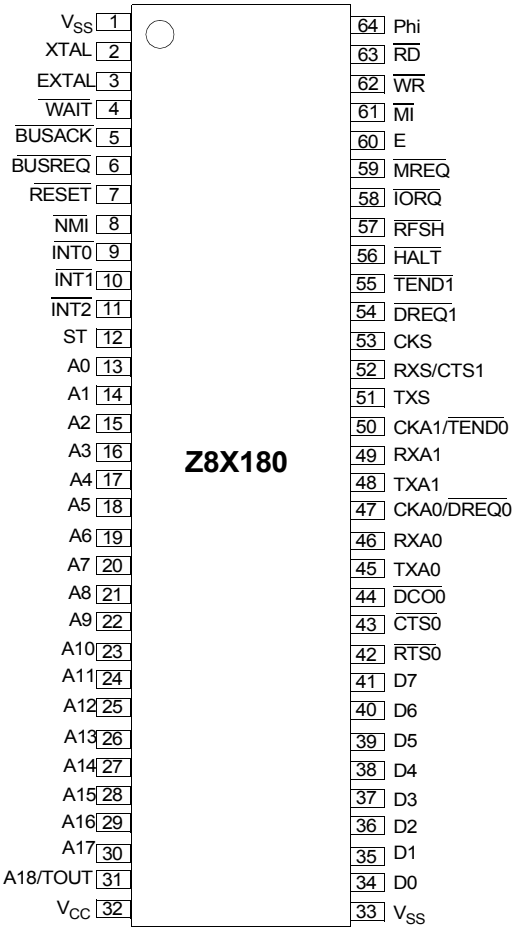

Figure 1. 64-Pin DIP

OPERATION MODES

The Z8X180 can be configured to operate like the Hitachi HD64180. This functionality is accomplished by allowing user control over the $\overline{M1}$, $\overline{IORQ}$, $\overline{WR}$, and $\overline{RD}$ signals. The Operation Mode Control Register (OMCR), illustrated in Figure 5, determines the $\overline{M1}$ options, the timing of the $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ signals, and the RETI operation.

Operation Mode Control Register

Bit	7	6	5	4	0
Bit/Field	M1E	$\overline{M1TE}$	IOC	Reserved	
R/W	R/W	W	R/W	–	
Reset	1	1	1	–	

Note: R = Read W = Write X = Indeterminate? = Not Applicable

Figure 5. Operation Mode Control Register

M1E (M1_Enable): This bit controls the $\overline{M1}$ output and is set to a 1 during RESET.

When M1E is 1, the $\overline{M1}$ output is asserted Low during the Op Code fetch cycle, the INT0 acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge. This action also causes the M1 signal to be Active during both fetches of the RETI instruction sequence, and may cause corruption of the external interrupt daisy chain. Therefore, this bit must be 0 for the Z8X180. When M1E is 0 the $\overline{M1}$ output is normally inactive and asserted Low only during the refetch of the RETI instruction sequence and the $\overline{INT0}$ acknowledge cycle (Figure 6).

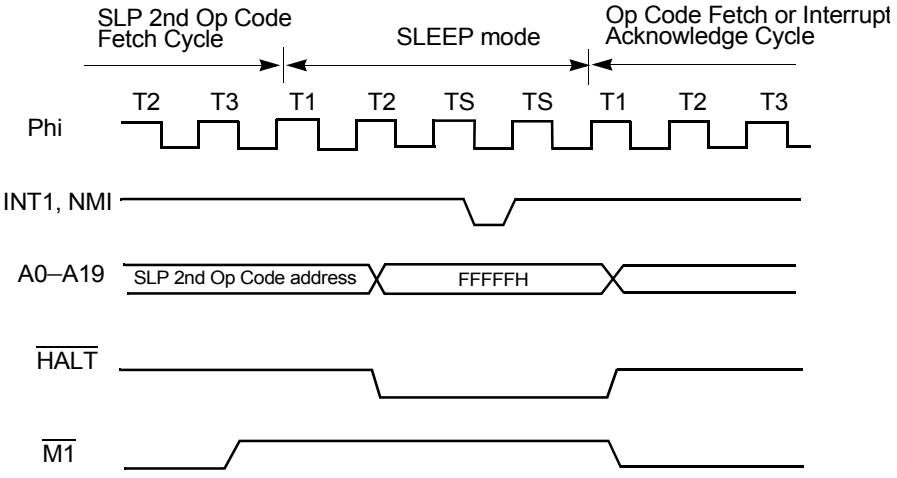

Figure 21. SLEEP Timing Diagram

IOSTOP Mode

IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode

SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode, noting that internal I/O sources, (disabled by IOSTOP) cannot generate a recovery interrupt.

CPU Control Register (CCR: 1FH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Clock Divide	STAND BY/ IDLE Enable	BREXT	LNPHI	STAND BY/ IDLE Enable	LNIO	LNCPU CTL	LNAD/ DATA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	Clock Divide	R/W	0 1	XTAL/2 XTAL/1
6	STANDBY /IDLE Mode	R/W	 00 01 10 11	In conjunction with Bit 3 No STANDBY IDLE after SLEEP STANDBY after SLEEP STANDBY after SLEEP 64 Cycle Exit (Quick Recovery)
5	BREXT	R/W	0 1	Ignore BUSREQ in STANDBY/IDLE STANDBY/IDLE exit on BUSREQ
4	LNPHI	R/W	0 1	Standard Drive 33% Drive on EXTPHI Clock
3	STANDBY /IDLE Mode	R/W	 00 01 10 11	In conjunction with Bit 6 No STANDBY IDLE after SLEEP STANDBY after SLEEP STANDBY after SLEEP 64 Cycle Exit (Quick Recovery)

Figure 35. $\overline{\text{NMI}}$ Timing

INT0 - Maskable Interrupt Level 0

The next highest priority external interrupt after $\overline{\text{NMI}}$ is $\overline{\text{INT0}}$. $\overline{\text{INT0}}$ is sampled at the falling edge of the clock state prior to T3 or T1 in the last machine cycle. If $\overline{\text{INT0}}$ is asserted LOW at the falling edge of the clock state prior to T3 or T1 in the last machine cycle, $\overline{\text{INT0}}$ is accepted. The interrupt is masked if either the IEF1 flag or the ITEO (Interrupt Enable 0) bit in ITC are reset to `0`. After $\overline{\text{RESET}}$ the state is as follows:

1. IEF1 is `0`, so $\overline{\text{INT0}}$ is masked
2. ITE0 is `1`, so $\overline{\text{INT0}}$ is enabled by execution of the El (Enable Interrupts) instruction

The $\overline{\text{INT0}}$ interrupt is unique in that 3 programmable interrupt response modes are available - Mode 0, Mode 1 and Mode 2. The specific mode is selected with the IM 0, IM 1 and IM 2 (Set Interrupt Mode) instructions. During $\overline{\text{RESET}}$, the Z8X180 is initialized to use Mode 0 for $\overline{\text{INT0}}$. The 3 interrupt response modes for $\overline{\text{INT0}}$ are:

- Mode 0–Instruction fetch from data bus
- Mode 1–Restart at logical address `0038H`
- Mode 2–Low-byte vector table address fetch from data bus

INT0 Mode 0

During the interrupt acknowledge cycle, an instruction is fetched from the data bus (DO–D7) at the rising edge of T3. Often, this instruction is one of the eight single byte RST (RESTART) instructions which stack the PC and restart execution at a fixed logical address. However, multibyte instructions can be processed if the interrupt acknowledging device can provide a multibyte response. Unlike all other interrupts, the PC is not automatically stacked:

disabling all maskable interrupts. The interrupt service routine normally terminates with the EI (Enable Interrupts) instruction followed by the RETI (Return from Interrupt) instruction, to reenable the interrupts. Figure 37 depicts the use of $\overline{\text{INT0}}$ (Mode 1) and RETI for the Mode 1 interrupt sequence.

Figure 37. INT0 Mode 1 Interrupt Sequence

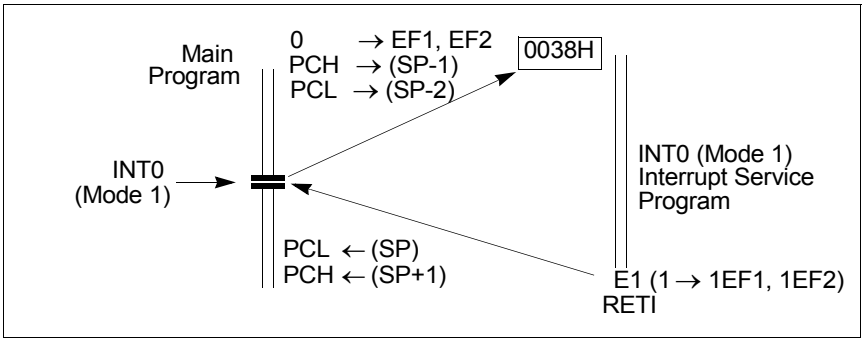

Figure 38 illustrates $\overline{\text{INT0}}$ Mode 1 Timing.

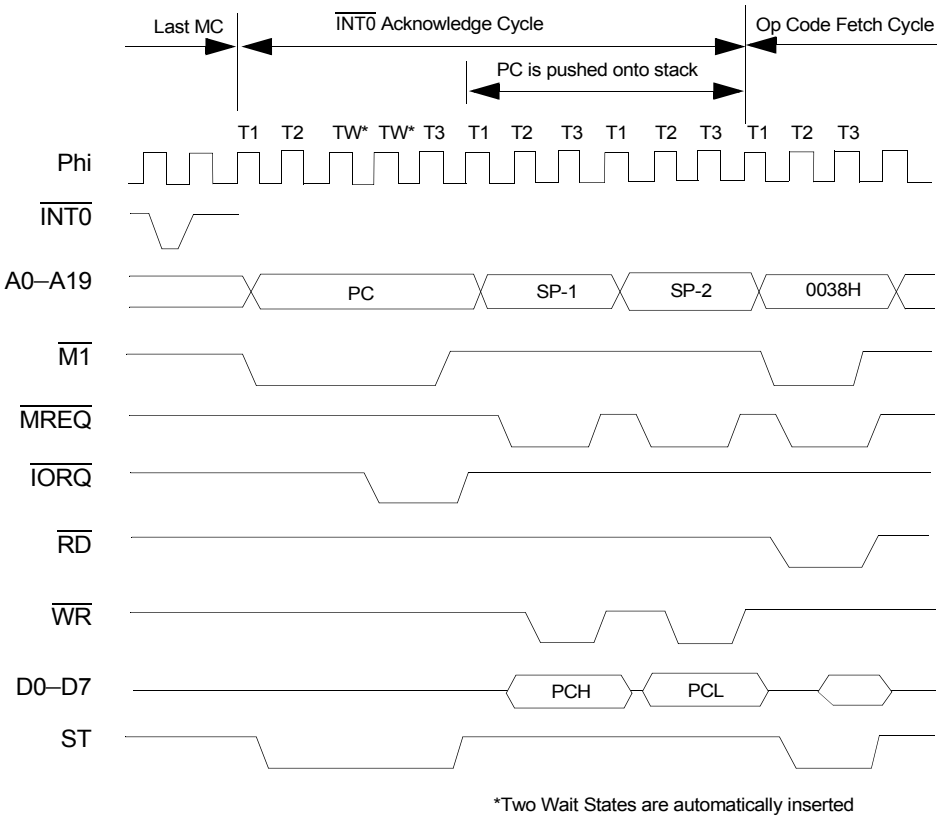

Figure 38. INT0 Mode 1 Timing

INT0 Mode 2

This method determines the restart address by reading the contents of a table residing in memory. The vector table consists of up to 128 two-byte restart addresses stored in low byte, high byte order.

$\overline{\text{DREQ0}}$ for ASCI transmission and reception respectively. To initiate memory to/from ASCI DMA transfer, perform the following operations:

1. Load the source and destination addresses into SAR0 and DAR0 Specify the I/O (ASCI) address as follows:
   a. Bits A0–A7 must contain the address of the ASCI channel transmitter or receiver (I/O addresses 6H-9H).
   b. Bits A8–A15 must equal 0.
   c. Bits SAR17–SAR16 must be set according to Table 16 to enable use of the appropriate ASCI status bit as an internal DMA request.

Table 16. DMA Transfer Request

SAR18	SAR17	SAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	RDRF (ASCI channel 0)
X	1	0	RDRF (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

DAR18	DAR17	DAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	TDRE (ASCI channel O)
X	1	0	TDRE (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

Miscellaneous

Free Running Counter (I/O Address = 18H)

If data is written into the free running counter, the interval of DRAM refresh cycle and baud rates for the ASCI and CSI/O are not guaranteed.

In IOSTOP mode, the free running counter continues counting down. It is initialized to FFH during RESET.

Free Running counter (FRC: 18H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Counting Data							
R/W	R							
Reset	?							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
31	t_{INTS}	$\overline{INT}$ Set-up Time to PHI Fall	20	—	15	—	ns
32	t_{INTH}	$\overline{INT}$ Hold Time from PHI Fall	10	—	10	—	ns
33	t_{NMIW}	$\overline{NMI}$ Pulse Width	35	—	25	—	ns
34	t_{BRS}	$\overline{BUSREQ}$ Set-up Time to PHI Fall	10	—	10	—	ns
35	t_{BRH}	$\overline{BUSREQ}$ Hold Time from PHI Fall	10	—	10		ns
36	t_{BAD1}	PHI Rise to $\overline{BUSACK}$ Fall Delay	—	25	—	15	ns
37	t_{BAD2}	PHI Fall to $\overline{BUSACK}$ Rise Delay	—	25	—	15	ns
38	t_{BZD}	PHI Rise to Bus Floating Delay Time	—	40	—	30	ns
39	t_{MEWH}	$\overline{MREQ}$ Pulse Width (High)	35	—	25	—	ns
40	t_{MEWL}	$\overline{MREQ}$ Pulse Width (Low)	35	—	25	—	ns
41	t_{RFD1}	PHI Rise to $\overline{RFSH}$ Fall Delay	—	20	—	15	ns
42	t_{RFD2}	PHI Rise to $\overline{RFSH}$ Rise Delay	—	20	—	15	ns
43	t_{HAD1}	PHI Rise to $\overline{HALT}$ Fall Delay	—	15	—	15	ns
44	t_{HAD2}	PHI Rise to $\overline{HALT}$ Rise Delay	—	15	—	15	ns
45	t_{DRQS}	$\overline{DREQ1}$ Set-up Time to PHI Rise	20	—	15	—	ns
46	t_{DRQH}	$\overline{DREQ1}$ Hold Time from PHI Rise	20	—	15	—	ns
47	t_{TED1}	PHI Fall to $\overline{TENDi}$ Fall Delay	—	25	—	15	ns
48	t_{TED2}	PHI Fall to $\overline{TENDi}$ Rise Delay	—	25	—	15	ns
49	t_{ED1}	PHI Rise to E Rise Delay	—	30	—	15	ns
50	t_{ED2}	PHI Fall or Rise to E Fall Delay	—	30	—	15	ns
51	P_{WEH}	E Pulse Width (High)	25	—	20	—	ns
52	P_{WEL}	E Pulse Width (Low)	50	—	40	—	ns
53	t_{Er}	Enable Rise Time	—	10	—	10	ns

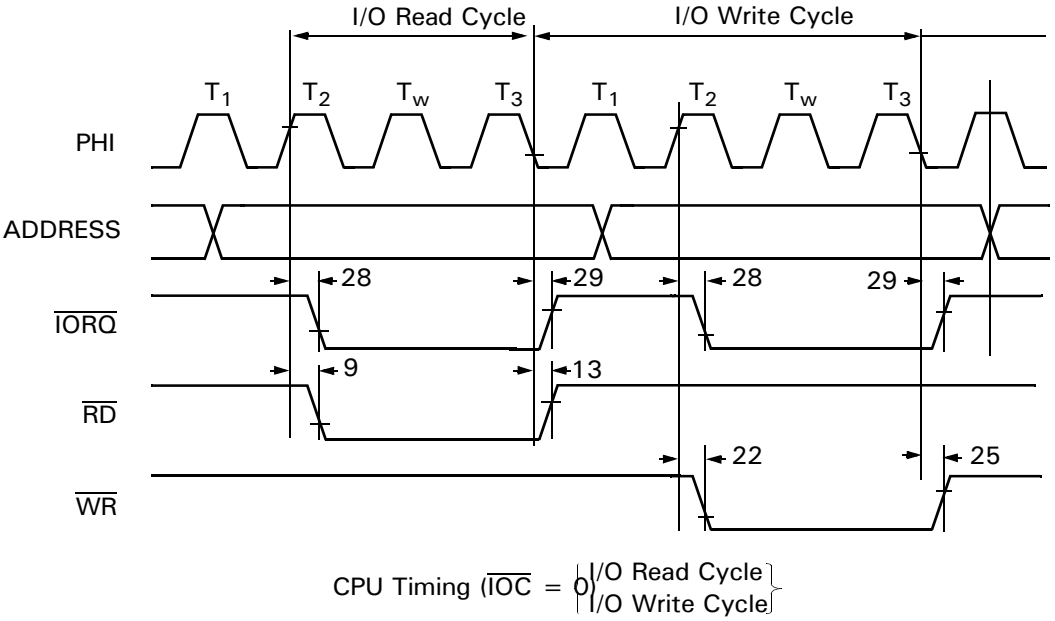

Figure 83. CPU Timing ($\overline{IOC}$ = 0) (I/O Read Cycle, I/O Write Cycle)

Table 46. I/O Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
INPUT	INIR	11 101 101 10 110 010					D		S	2	14 (Br ≠ 0) 12 (Br = 0)	Q (BC)$_I$→(HL)$_M$ HL$_R$ + 1→HL$_R$ Br-f→Br Repeat Q until Br = 0 Cr→A0~A7 Br→A8→A16	X	S	X	X	↑	X
OUTPUT	OUT (m)A	11 010 011 <m>						S	D	2	10	Ar→(Am)1 m→A0~A7 Ar→A8~A16	•	•	•	•	•	•
	OUT (C),g	11 101 101 01 g 001				S			D	2	10	gr→(BC)1 Cr→A0~A7 Br→A8~A16	•	•	•	•	•	•
	OUT0(m),g**	11 101 101 00 g 001 <m>				S			D	3	13	gr→(00m)1 m→A0~A7 00→A8~A16	•	• (5)	•	•	• (6)	•
	OTDM**	11 101 101 10 001 011					S		D	2	14	(HL)$_M$→(00C)1 HL$_R$-1→HL$_R$ Cr-1→Cr Br-1→Br Cr→A0~A7 00→A8~A16	↑	↑	↑	P	↑ (6)	↑
	OTDMR**	11 101 101 10 011 011					S		D	2	16 (Br ≠ 0) 14 (Br = 0)	Q (HL)$_M$→(00C)1 HL$_R$-1-HL$_R$ Cr-1→Cr Br-1→Br Repeat Q until Br = 0 Cr→A0~A7 00→A8~A16	R	S	R	S	↑ (6)	R

Special Control Instructions

Table 47. Special Control Instructions

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Special Function	DAA	00 100 111						S/D		1	4	Decimal Adjust Accumulator	↑	↑	↑	P	•	↑
Carry Control	CCF	00 111 111								1	3	$\overline{C}$→C	•	•	R	•	R	↑
	SCF	00 110 111								1	3	1→C	•	•	R	•	R	S
CPU Control	DI	11 110 011								1	3	0→IEF1,0→IEF2 (7)	•	•	•	•	•	•
	EI	11 111 011								1	3	1→IEF1,1→IEF2 (7)	•	•	•	•	•	•
	HALT	01 110 110								1	3	CPU halted	•	•	•	•	•	•
	IM0	11 101 101								2	6	Interrupt	•	•	•	•	•	•
		01 000 110										Mode 0						
	IM1	11 101 101								2	6	Interrupt	•	•	•	•	•	•
		01 010 110										Mode 1						
	IM2	11 101 101								2	6	Interrupt	•	•	•	•	•	•
		01 011 110										Mode 2						
	NOP	00 000 000								1	3	No operation	•	•	•	•	•	•
	SLP**	11 101 101								2	8	Sleep	•	•	•	•	•	•
		01 110 110																

7) Interrupts are not sampled at the end of DI or EI.

MNEMONICS	Bytes	Machine Cycles	States
	2	3	7 (if Br = 0)
EI	1	1	3
EX AF,AF'	1	2	4
EX DE,HL	1	1	3
EX (SP),HL	1	6	16
EX (SP)I,IX	2	7	19
EX (SP),IY	2	7	19
EXX	1	1	3
HALT	1	1	3
IM 0	2	2	6
IM 1	2	2	6
IM 2	2	2	6
INC g	1	2	4
INC (HL)	1	4	10
INC (IX+d)	3	8	18
INC (IY+d)	3	8	18
INC ww	1	2	4
INC IX	2	3	7
INC IY	2	3	7
IN A,(m)	2	3	9
IN g,(C)	2	3	9
INI	2	4	12
INIR	2	6	14 (if Br ≠ 0)
	2	4	12 (If Br = 0)
IND	2	4	12
INDR	2	6	14 (If Br ≠ 0)
INDR	2	4	12 (If Br = 0)
IN0 g,(m)**	3	4	12
JP f,mn	3	2	6 (If f is false)

Note 1: (HL) replaces g.

Note 2: (HL) replaces s.

Note 3: If DDH is supplemented as first Op Code for the instructions which have HL or (HL) as an operand in Table 48, the instructions are executed replacing HL with IX and (HL) with (IX+d).

```
ex. 22H : LD (mn), HL
```

```
DDH 22H : LD (mn), IX
```

If FDH is supplemented as 1st Op Code for the instructions which have HL or (HL) as an operand in Table 48, the instructions are executed replacing HL with IY and (HL) with (IY+d).

```
ex. 34H : INC (HL)
```

```
FDH 34H : INC (IY+d)
```

However, JP (HL) and EX DE, HL are exceptions and note the following.

- If DDH is supplemented as 1st Op Code for JP (HL), (IX) replaces (HL) as operand and JP (IX) is executed
- If FDH is supplemented as 1st Op Code for JP (HL), (IY) replaces (HL) as operand and JP (IY) is executed
- Even if DDH or FDH is supplemented as 1st Op Code for EX DE, HL, HL is not replaced and the instruction is regarded as illegal instruction.

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
CPI CPD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4 ~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
CPIR CPDR (If $BC_R \neq 0$ and $Ar = (HL)_M$)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC8	TiTiTi TiTi	*	Z	1	1	1	1	1	1	1
CPIR CPDR (If $BC_R=0$ or $Ar=(HL)_M$)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
CPL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
DAA	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
DI*1	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
* 1 Interrupt request is not sampled.											

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (IX+d),m LD (IY+d),m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	T1T2T3	IX+ d IY+d	DATA	1	0	0	1	1	1	1
LD A, (BC) LD A, (DE)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	BC DE	DATA	0	1	0	1	1	1	1
LD A,(mn)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	T1T2T3	mn	DATA	0	1	0	1	1	1	1
LD (BC),A LD (DE),A	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	BC DE	A	1	0	0	1	1	1	1