Zilog - Z8018006VEC00TR Datasheet

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006vec00tr

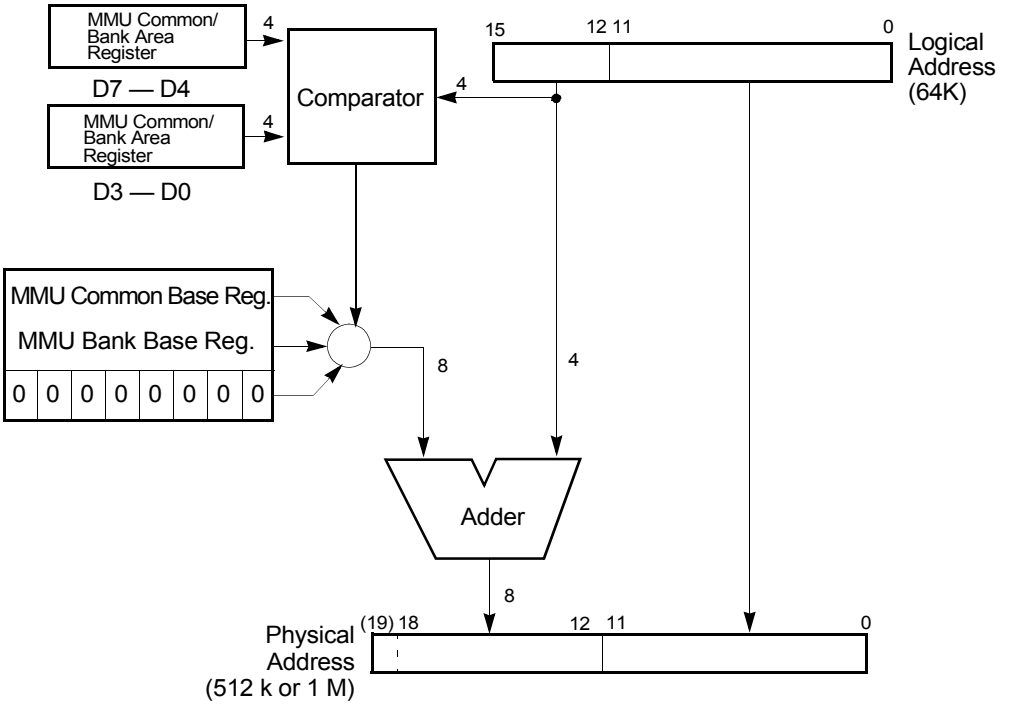


Figure 29. Physical Address Generation

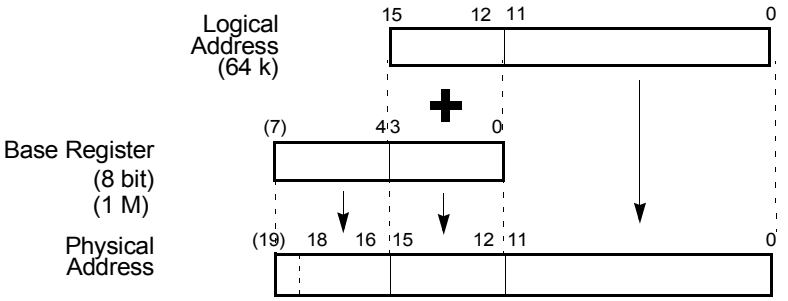


Figure 30. Physical Address Generation 2

Note: Packages not containing an A19 pin or situations using TOUT instead of A18 yield an address capable of only addressing 512K of physical space.

Interrupts

The Z8X180 CPU has twelve interrupt sources, 4 external and 8 internal, with fixed priority. (Reference Figure 31.)

This section explains the CPU registers associated with interrupt processing, the TRAP interrupt, interrupt response modes, and the external interrupts. The detailed discussion of internal interrupt generation (except TRAP) is presented in the appropriate hardware section (that is, PRT, DMAC, ASCI, and CSI/O).

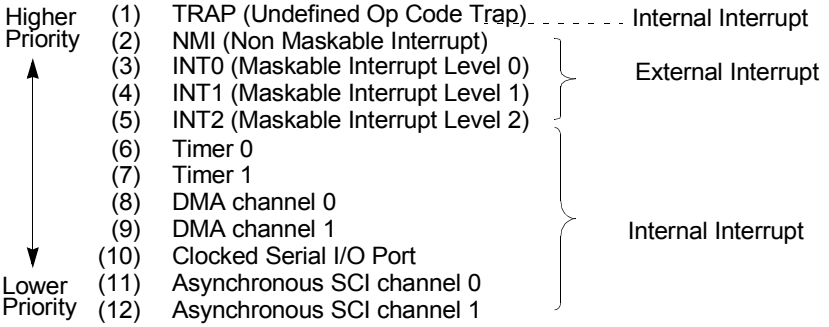


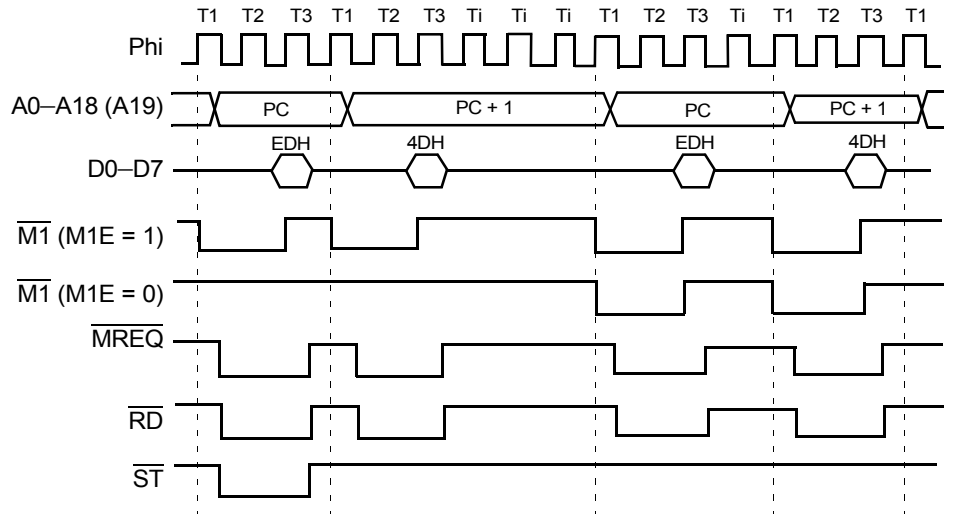
Figure 31. Interrupt Sources

Interrupt Control Registers and Flags. The Z8X180 has three registers and two flags which are associated with interrupt processing.

Return from Subroutine (RETI) Instruction Sequence

When the EDH/4DH sequence is fetched by the Z8X180, it is recognized as the RETI instruction sequence. The Z8X180 then refetches the RETI instruction with four T-states in the EDH cycle allowing the Z80 peripherals time to decode that cycle (See Figure 42). This procedure allows the internal interrupt structure of the peripheral to properly decode the instruction and behave accordingly.

The M1E bit of the Operation Mode Control Register (OMCR) must be set to 0 so that $\overline{M1}$ signal is active only during the refetch of the RETI instruction sequence. This condition is the desired operation when Z80 peripherals are connected to the Z8018X.



Note: RETI machine cycles 9 and 10 not shown.

Figure 42. RETI Instruction Sequence

The RETI instruction takes 22 T-states and 10 machine cycles. Table 10 lists the conditions of all the control signals during this sequence for the

Refresh Control Register (RCR)

The RCR specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

Refresh Control Register (RCR: 36H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	REFE	REFW	?				CYC1	CYC0
R/W	R/W	R/W	?				R/W	R/W
Reset	1	1	?				0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	REFE	R/W		**REFE: Refresh Enable**
			0	Disables the refresh controller
			1	Enables refresh cycle insertion.
6	REFW	R/W		**Refresh Wait** (bit 6)
			0	Causes the refresh cycle to be two clocks in duration.
			1	Causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW).
1–0	CYC1–0	R/W		**Cycle Interval** — CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. In the case of dynamic RAMs requiring 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET. Refer to Table 11.

Bit Position	Bit/Field	R/W	Value	Description
6	DE0	R/W		**Enable Channel 0** — When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates BCR0 = 0), DE0: is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU. To perform a software write to DE0, DWE0 must be written with 0 during the same register write access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DME (DMA Main Enable) to 1. DE0 is cleared to 0 during RESET.
5	$\overline{\text{DWE1}}$	W		**Bit Write Enable 1** — When performing any software write to DEI, $\overline{\text{DWE1}}$ must be written with 0 during the same access. $\overline{\text{DWE1}}$ write value of 0 is not held and DWE1 is always read as 1.
4	$\overline{\text{DWE0}}$	W		**Bit Write Enable 0** — When performing any software write to DE0, $\overline{\text{DWE0}}$ must be written with 0 during the same access. $\overline{\text{DWE0}}$ write value of 0 is not held and DWE0 is always read as 1.
3	DIE1	R/W		**DMA Interrupt Enable Channel 1** — When DIE1 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 is 0) causes a CPU interrupt request to be generated. When DIE1 is 0, the channel 1 DMA termination interrupt is disabled. DIE1 is cleared to 0 during RESET.
2	DIE0			**DMA Interrupt Enable Channel 0** — When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 is 0) causes a CPU interrupt request to be generated. When DIE0 is 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

Table 13. Channel 0 Source

SM1	SM0	Memory/I/O	Address Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	-1
1	0	Memory	fixed
1	1	I/O	fixed

Table 14 describes all DMA TRANSFER mode combinations of DM0 DM1, SM0 SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 14. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Increment/Decrement
0	0	0	0	Memory to Memory	SAR0+1, DAR0+1
0	0	0	1	Memory to Memory	SAR0-1, DAR0+1
0	0	1	0	Memory* to Memory	SAR0 fixed, DAR0+ 1
0	0	1	1	I/O to Memory	SAR0 fixed DAR0+1
0	1	0	0	Memory to Memory	SAR0+1, DAR0-1
0	1	0	1	Memory to Memory	SAR0-1,DAR0-1
0	1	1	0	Memory to Memory	SAR0 fixed, DAR0-1
0	1	1	1	I/O to Memory	SAR0 fixed. DAR0-1
1	0	0	0	Memory to Memory*	SAR0+ 1, DAR0 fixed
1	0	0	1	Memory to Memory*	SAR0-1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	

Bit Position	Bit/Field	R/W	Value	Description
4	FE	R		**Framing Error** — If a receive data byte frame is delimited by an invalid stop bit (that is, 0, should be 1), FE is set to 1. FE is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.
3	RIE	R/W		**Receive Interrupt Enable** — RIE must be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, if any of the flags RDRF, OVRN, PE, or FE become set to 1, an interrupt request is generated. For channel 0, an interrupt is also generated by the transition of the external $\overline{\text{DCD0}}$ input from Low to High.
2	CTS1E	R/W		**Channel 1 $\overline{\text{CTS}}$ Enable** — Channel 1 has an external $\overline{\text{CTS1}}$ input which is multiplexed with the receive data pin (RXS) for the CSI/O (Clocked Serial I/O Port). Setting CTS1E to 1 selects the $\overline{\text{CTS1}}$ function and clearing CTS1E to 0 selects the RXS function.
1	TDRE	R		**Transmit Data Register Empty** — TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. When the external $\overline{\text{CTS}}$ input is High, TDRE is reset to 0.
0	TIE	R/W		**Transmit Interrupt Enable** — TIE must be set to 1 to enable ASCI transmit interrupt requests. If TIE is 1, an interrupt is requested when TDRE is 1. TIE is cleared to 0 during RESET.

ASCI Control Register B 0 (CNTLB0: 02H)
ASCI Control Register B 1 (CNTLB1: 03H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	MPBT	MP	$\overline{\text{CTS}}$/PS	PE0	DR	SS2	SS1	SS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	0	0	0	0	1	1	1

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	MPBT	R/W		**Multiprocessor Bit Transmit** — When multiprocessor communication format is selected (MP bit is 1), MPBT is used to specify the MPB data bit for transmission. If MPBT is 1, then MPB = 1 is transmitted. If MPBT is 0, then MPBT = 0 is transmitted. MPBT state is undefined during and after RESET.
6	MP	R/W		**Multiprocessor Mode** — When MP is set to 1, the data format is configured for multiprocessor mode based on the MOD2 (number of data bits) and MOD0 (number of stop bits) bits in CNTLA. The format is as follows. Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits Multiprocessor (MP = 1) format has no provision for parity. If MP is 0, the data format is based on MOD0 MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

CSI/O Transmit/Receive Register (TRDR: 0BH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	CSI/O Transmit/Receive Data							
R/W	R/W							
Reset	0							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Table 22. CSI/O Baud Rate Selection

SS2	SS1	SS0	Divide Ratio	Baud Rate
0	0	0	÷ 20	(200000)
0	0	1	÷ 40	(100000)
0	1	0	÷ 80	(50000)
0	1	1	÷ 160	(25000)
1	0	0	÷ 320	(12500)
1	0	1	÷ 640	(6250)
1	1	0	÷ 1280	(3125)
1	1	1	External Clock input (less than ÷ 20)	

Note: ( ) indicates the baud rate (BPS) at Phi = 4 MHz.

After RESET, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSI/O Interrupts

The CSI/O interrupt request circuit is shown in Figure 58.

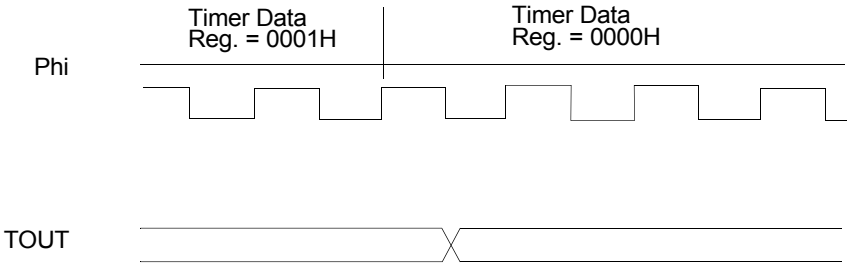


Figure 65. Timer Output Timing Diagram

PRT Interrupts

The PRT interrupt request circuit is illustrated in Figure 66.

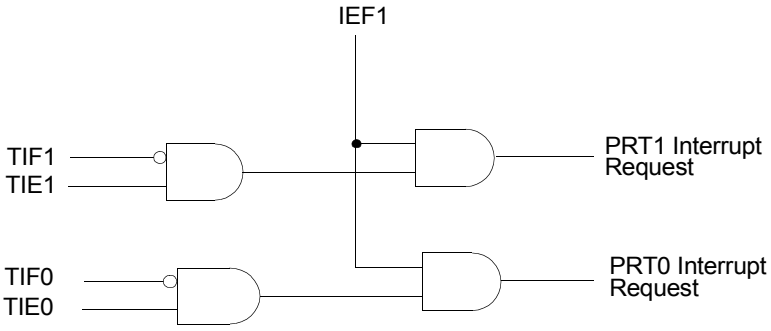


Figure 66. PRT Interrupt Request Generation

PRT and RESET

During RESET, the bits in TCR are initialized as defined in the TCR register description. Down counting is stopped and the TMDR and RLDR registers are initialized to FFFFH. The A18/TOUT pin reverts to the address output function.

Figure 74 depicts CPU register configurations.

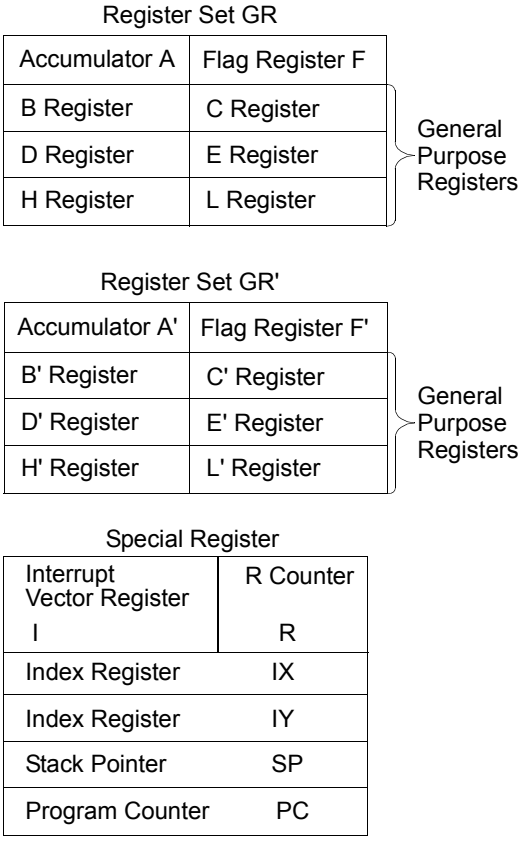


Figure 74. CPU Register Configurations

Accumulator (A, A')

The Accumulator (A) is the primary register used for many arithmetic, logical, and I/O instructions.

Indexed (INDX)

The memory operand address is calculated using the contents of an Index Register (IX or IY) and an 8-bit signed displacement specified in the instruction. Refer to Figure 77

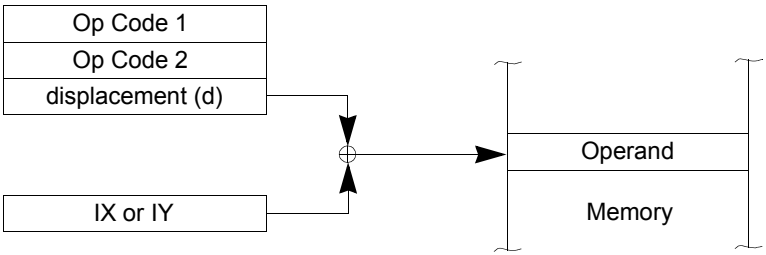


Figure 77. Indexed Addressing

Extended (EXT)

The memory operand address is specified by two bytes contained in the instruction, as depicted in Figure 78.

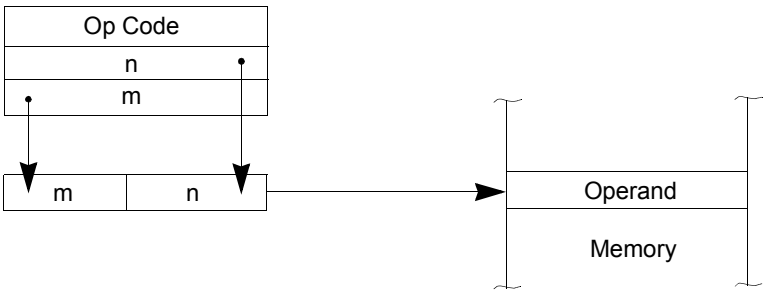


Figure 78. Extended Addressing

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
69	t_{IR}	Input Rise Time (except EXTAL, $\overline{\text{RESET}}$)	—	50	—	50	ns
70	t_{IF}	Input Fall Time (except EXTAL, $\overline{\text{RESET}}$)	—	50	—	50	ns

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
CALL mn	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC6	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
CALL f,mn (If condition is false)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
CALL f,mn if condition is true)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC6	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
CCF	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
INC (IX+ d) INC (IY+d) DEC (IX+d) DEC (IY+d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4~MC5	TiTi	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	X+ d IY+ d	DATA	0	1	0	1	1	1	1
	MC7	T1	*	Z	1	1	1	1	1	1	1
	MC8	T1T2T3	IX+ d IY+d	DATA	1	0	0	1	1	1	1
INC ww DEC ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	t	1	1	1	1
INC IX INC IY DEC IX DEC IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
IN A,(m)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC3	T1T2T3	m to A0~A7 A to A8~A15	DATA	0	1	1	0	1	1	1

Table 53. Request Acceptances in Each Operating Mode

Request / Current Status		Normal Operation (CPU mode and IOSTOP Mode)	WAIT State	Refresh Cycle	Interrupt Acknowledge Cycle	DMA Cycle	BUS RELEASE Mode	SLEEP Mode	SYSTEM STOP Mode
	Internal I/O Interrupt	↑	↑	↑	↑	↑	↑	↑	Not acceptable
	$\overline{NMI}$	↑	↑	↑	Not acceptable Interrupt acknowledge cycle precedes. $\overline{NMI}$ is accepted after executing	Acceptable DMA cycle stops			Acceptable Return from SYSTEM STOP mode to normal operation
Note: * Not acceptable when DMA Request is in level-sense. ↑: Same as above. MC: Machine Cycle									

REQUEST PRIORITY

The Z80180 features three types of requests.

Table 54. The Z80180 Types of Requests

Type 1	Accepted in specified state	WAIT
Type 2	Accepted in each machine cycle	Refresh Request, DMA Request, and Bus Request.
Type 3	Accepted in each instruction	Interrupt Request

Type 1, Type 2, and Type 3 requests priority as follows.

- Highest priority Type 1 > Type 2 > Type 3 lowest priority
- Each request priority in Type 2 is shown as follows. highest priority Bus Req. > Refresh Req. > DMA Request lowest priority

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes

Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
$\overline{WAIT}$	—	IN (N)	IN (N)	IN (A)	IN (N)
$\overline{BUSACK}$	—	1	OUT	OUT	OUT
$\overline{BUSREQ}$	—	IN (N)	IN (A)	IN (A)	IN (A)
$\overline{RESET}$	—	0	IN (A)	IN (A)	IN (A)
$\overline{NMI}$	—	IN (N)	IN (A)	IN (A)	IN (A)
$\overline{INT}_0$	—	IN (N)	IN (A)	IN (A)	IN (A)
$\overline{INT}_1$	—	IN (N)	IN (A)	IN (A)	IN (A)
$\overline{INT}_2$	—	IN (N)	IN (A)	IN (A)	IN (A)
ST	—	1	1	OUT	1
A0–A17, A19	—	Z	1	A	1
A18/TOUT	A18	Z	1	A	1
	TOUT	Z	OUT	H	H
D0–D7	—	Z	Z	A	Z
$\overline{RTS}$0	—	1	H	OUT	H
$\overline{CTS}$0	—	IN (N)	IN (A)	IN (N)	N (N)
$\overline{DCD}$0	—	IN (N)	IN (A)	IN (N)	IN (N)
TXA0	—	1	OUT	H	H
RXA0	—	IN (N)	IN (A)	IN (N)	IN (N)
CKA0/$\overline{DREQ}$0	CKA0 (Internal Clock Mode)	Z	OUT	Z	Z

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
Timer Data Register Channel 1L:	TMDR1L	1	4	
Timer Data Register Channel 1H:	TMDR1H	1	5	
Timer Reload Register Channel 1L	RLDR1L	1	6	
Timer Reload Register Channel 1H:	RLDR1H	1	7	
Free Running Counter:	FRC	1	8	Read only
DMA Source Address Register Channel 0L:	SAR0L	2	0	
DMA Source Address Register Channel 0H:	SAR0H	2	1	
DMA Source Address Register Channel 0B:	SAR0B	2	2	Bits 0-2 (3) are used for SAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — RDR0 (ASCI0) X X 1 0 — RDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Destination Address Register Channel 0L:	DAR0L	2	3	
DMA Destination Address Register Channel 0H:	DAR0H	2	4	
DMA Destination Address Register Channel 0B:	DAR0B	2	5	Bits 0-2 (3) are used for DAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — TDR0 (ASCI0) X X 1 0 — TDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Byte Count Register Channel 0L:	BCROL	2	6	
DMA Byte Count Register Channel 0H:	BCROH	2	7	
DMA Memory Address Register Channel 1L:	MAR1L	2	8	
DMA Memory Address Register Channel 1H:	MAR1H	2	9	

* In the R1 and Z mask, these DMAC registers are expanded from 4 bits to 3 bits in the package version of CP-68.

A

B

C

U

V

W