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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018006vsg

Table 5. Power-Down Modes (Z8S180/Z8L180-Class Processors Only)

Power-Down Modes	CPU Core	On-Chip I/O	Osc.	CLKOUT	Recovery Source	Recovery Time (Minimum)
SLEEP	Stop	Running	Running	Running	RESET, Interrupts	1.5 Clock
I/O STOP	Running	Stop	Running	Running	By Programming	–
SYSTEM STOP	Stop	Stop	Running	Running	RESET, Interrupts	1.5 Clock
IDLE †	Stop	Stop	Running	Stop	RESET, Interrupts, BUSREQ	8 + 1.5 Clock
STANDBY †	Stop	Stop	Stop	Stop	RESET, Interrupts, BUSREQ	2^{17} + 1.5 Clock (Normal Recovery) 2^{6} + 1.5 Clock (Quick Recovery)

† IDLE and STANDBY modes are only offered in the Z8S180. The minimum recovery time can be achieved if INTERRUPT is used as the Recovery Source.

STANDBY Mode

The Z8S180/Z8L180 is designed to save power. Two low-power programmable power-down modes have been added:

- STANDBY mode
- IDLE mode

The STANDBY/IDLE mode is selected by multiplexing bits 1 and 3 of the CPU Control Register (CCR, I/O Address = 1FH).

To enter STANDBY mode:

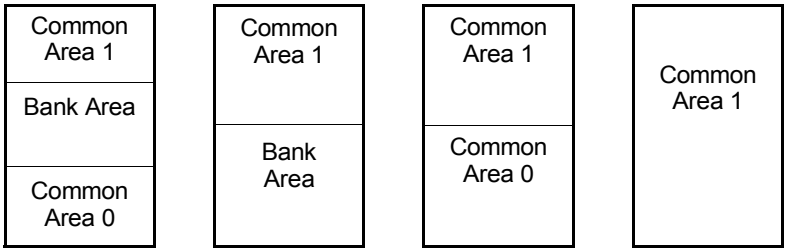


Figure 23. Logical Address Mapping Examples

Logical to Physical Address Translation

Figure 24 illustrates an example in which the three logical address space portions are mapped into a 1024KB physical address space. The important points to note are that Common and Bank Areas can overlap and that Common Area 1 and Bank Area can be freely relocated (on 4KB physical address boundaries). Common Area 0 (if it exists) is always based at physical address `00000H`.

MMU Common Base Register (CBR)

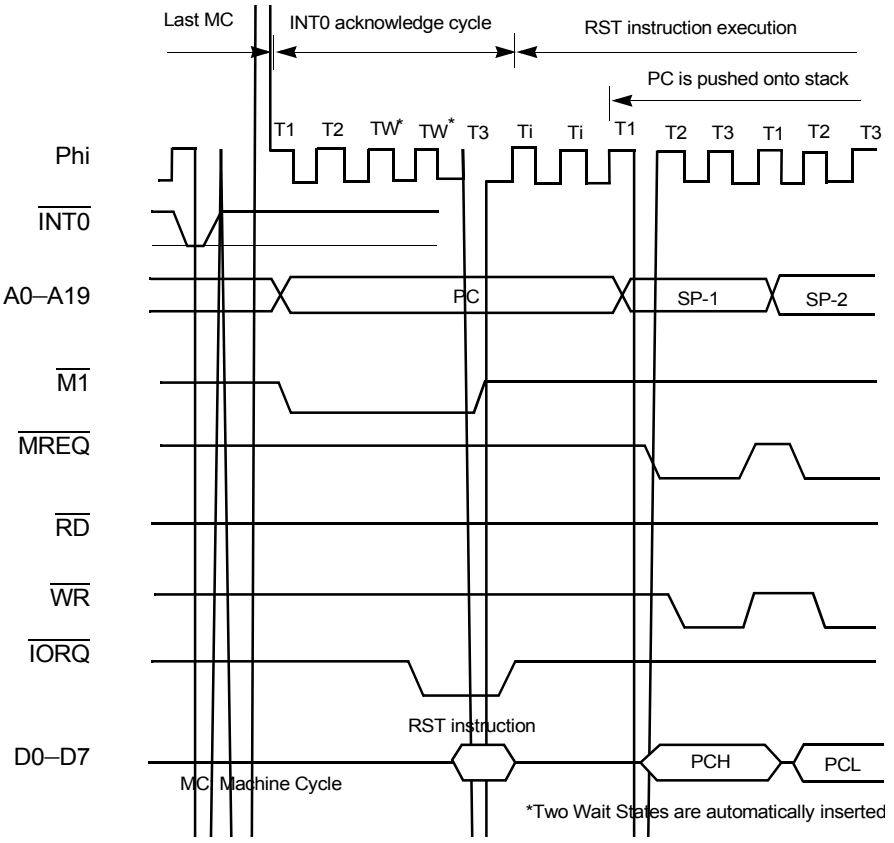
CBR specifies the base address (on 4K boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register (CBR: 38H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–0	CB7–0	R/W		CBR specifies the base address (on 4KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses.



Note: The TRAP interrupt occurs if an invalid instruction is fetched during Mode 0 interrupt acknowledge. (Reference Figure 36.)

Figure 36. $\overline{\text{INT0}}$ Mode 0 Timing Diagram

INT0 Mode 1

When $\overline{\text{INT0}}$ is received, the PC is stacked and instruction execution restarts at logical address `0038H`. Both IEF1 and IEF2 flags are reset to `0`,

ASCI to/from DMAC Operation

Operation of the ASCI with the on-chip DMAC channel 0 requires that the DMAC be correctly configured to use the ASCI flags as DMA request signals.

ASCI and RESET

During RESET, the ASCI status and control registers are initialized as defined in the individual register descriptions.

Receive and Transmit operations are stopped during RESET. However, the contents of the transmit and receive data registers (TDR and RDR) are not changed by RESET.

ASCI Clock

When in external clock input mode, the external clock is directly input to the sampling rate (÷16/÷64) as depicted in Figure 56.

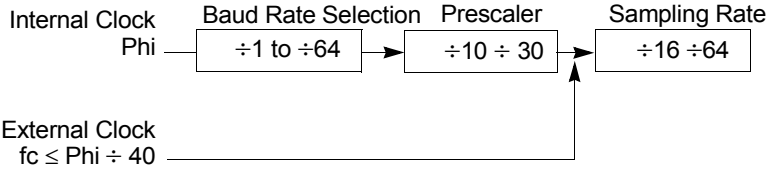


Figure 56. ASCI Clock

causes for an ASCI Receive interrupt (PE, FE, OVRN, and for ASCI0, DCD) continue to request RX interrupt if the RIE bit is 1. The Rx DMA request is inhibited if PE or FE or OVRN is set, so that software can detect where an error occurred. When the RIE bit is 0, as it is after a Reset, RDRF causes an ASCI interrupt if RIE is 1.

Clocked Serial I/O Port (CSI/O)

The Z8X180 includes a simple, high-speed clock, synchronous serial I/O port. The CSI/O includes transmit/receive (half-duplex), fixed 8-bit data, and internal or external data clock selection. High-speed operation (baud rate 200Kbps at fC = 4 MHz) is provided. The CSI/O is ideal for implementing a multiprocessor communication link between multiple Z8X180s. These secondary devices may typically perform a portion of the system I/O processing, (that is, keyboard scan/decode, LDC interface, for instance).

CSI/O Block Diagram

The CSI/O block diagram is illustrated in Figure 57. The CSI/O consists of two registers–the Transmit/Receive Data Register (TRDR) and Control Register (CNTR).

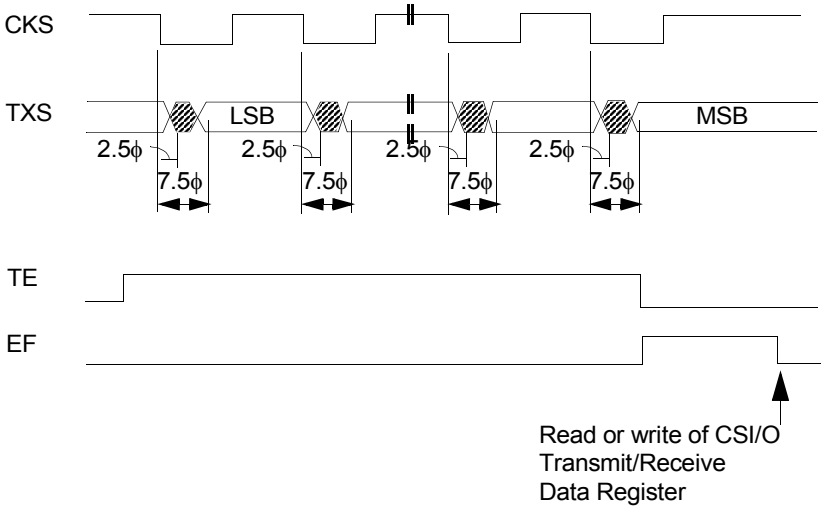


Figure 60. Transmit Timing–External Clock

Timer Data Register 0L (TMDR0L: 0CH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Data							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Timer Data Register 0H (TMDR0H: 0DH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Data							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Timer Reload Register (RLDR: I/O Address = CH0: 0EH, 0FH, CHI, 16H, 17H)

PRT0 and PRT1 each contain 16-bit Timer Reload Registers (RLDR). RLDR0 and RLDR1 are each accessed as low and high byte registers (RLDR0H, RLDR0L and RLDR1H, RLDR1L). During RESET, RLDR0 and RLDR1 are set to FFFFH

When the TMDR counts down to 0, it is automatically reloaded with the contents of RLDR.

TST (HL) - Test Memory

The contents of memory pointed to by HL are ANDed with the accumulator (A) and the status flags are updated. The memory contents and accumulator are not changed (non-destructive AND).

INO g, (m) - Input, Immediate I/O address

The contents of immediately specified 8-bit I/O address are input into the specified register. When I/O is accessed, `00H` is output in high-order bits of the address automatically.

OUTO (m), g - Output, Immediate I/O address

The contents of the specified register are output to the immediately specified 8-bit I/O address. When I/O is accessed, 00H is output in high-order bits of the address automatically.

CPU REGISTERS

The Z80180 CPU registers consist of Register Set GR, Register Set GR' and Special Registers.

The Register Set GR consists of 8-bit Accumulator (A), 8-bit Flag Register (F), and three General Purpose Registers (BC, DE, and HL) which may be treated as 16-bit registers (BC, DE, and HL) or as individual 8-bit registers (B, C, D, E, H, and L) depending on the instruction to be executed. The Register Set GR' is alternate register set of Register Set GR and also contains Accumulator (A'), Flag Register (F') and three General Purpose Registers (BC', DE', and HL'). While the alternate Register Set GR' contents are not directly accessible, the contents can be programmably exchanged at high speed with those of Register Set GR.

The Special Registers consist of 8-bit Interrupt Vector Register (I), 8-bit R Counter (R), two 16-bit Index Registers (IX and IY), 16-bit Stack Pointer (SP), and 16-bit Program Counter (PC)

Immediate (IMMED)

The memory operands are contained within one or two bytes of the instruction, as depicted in Figure 79.

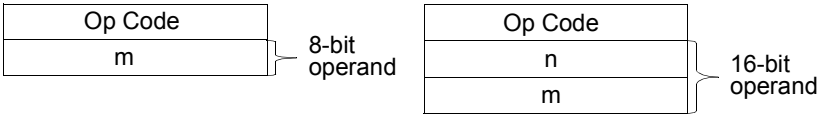


Figure 79. Immediate Addressing

Relative (REL)

Relative addressing mode is only used by the conditional and unconditional branch instructions (refer to Figure 80). The branch displacement (relative to the contents of the program counter) is contained in the instruction.

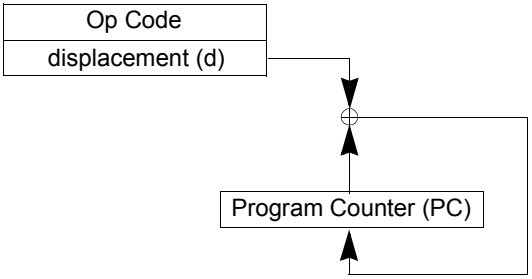


Figure 80. Relative Addressing

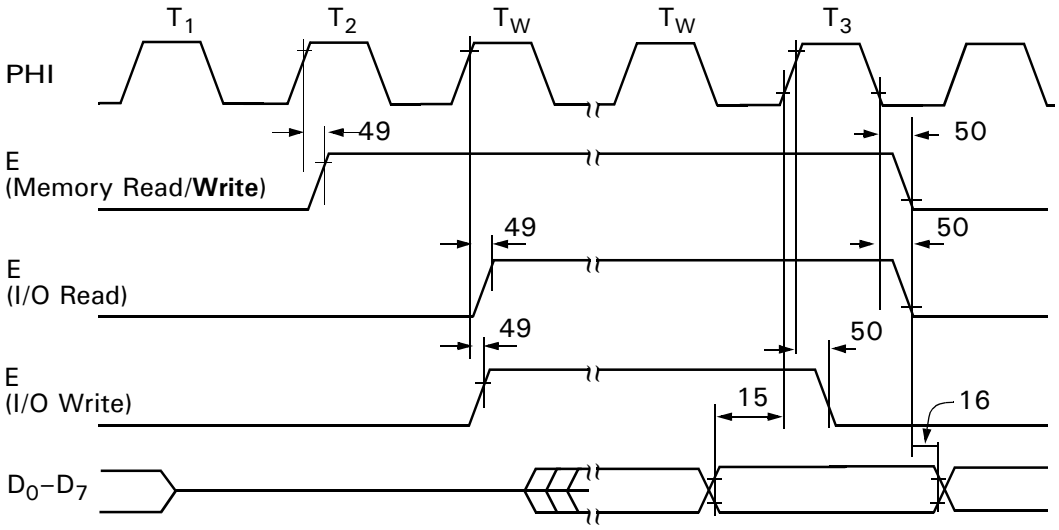


Figure 85. E Clock Timing (Memory R/W Cycle) (I/O R/W Cycle)

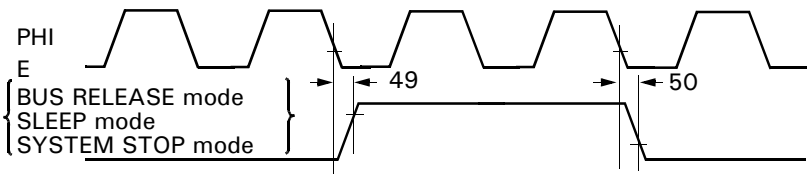


Figure 86. E Clock Timing (BUS RELEASE Mode, SLEEP Mode, and SYSTEM STOP Mode

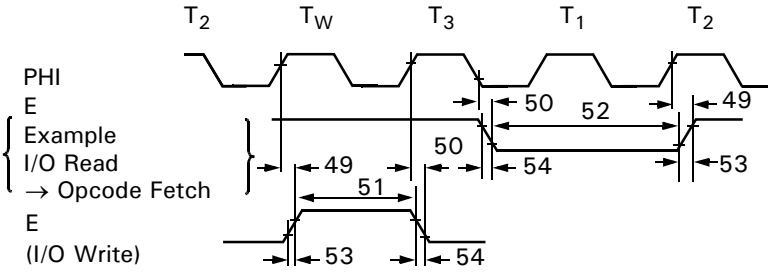


Figure 87. E Clock Timing (Minimum Timing Example of PWEL and PWEH)

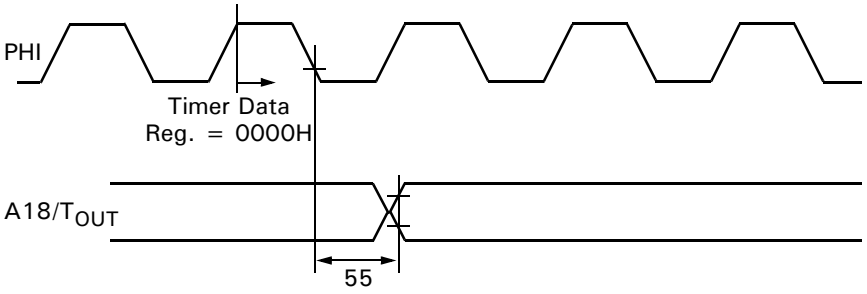


Figure 88. Timer Output Timing

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
AND	AND g	10 100 g				S		D		1	4	Ar*gr→Ar	↑	↑	S	P	R	R
	AND (HL)	10 100 110					S	D		1	6	Ar*$(HL)_M$→Ar	↑	↑	S	P	R	R
	AND m	11 100 110	S					D		2	6	Ar*m→Ar	↑	↑	S	P	R	R
		<m>																
	AND (IX + d)	11 011 101			S			D		3	14	Ar*$(1X + d))_M$→Ar	↑	↑	S	P	R	R
		10 100 110																
		<d>																
	AND (IY + d)	11 111 101			S			D		3	14	Ar*(1Y + d)v→Ar	↑	↑	S	P	R	R
		10 100 110																
		<d>																
Compare	CP g	10 111 g				S		D		1	4	Ar-gr	↑	↑	↑	V	S	↑
	CP (HL)	10 111 110					S	D		1	6	Ar-$(HL)_M$	↑	↑	↑	V	S	↑
	CP m	11 111 110	S					D		2	6	Ar-m	↑	↑	↑	V	S	↑
		<m>																
	CP (IX + d)	11 011 101		S				D		3	14	Ar-$(IX + d))_M$	↑	↑	↑	V	S	↑
		10 111 110																
		<d>																
	CP (IY + d)	11 111 101		S				D		3	14	Ar-$(IY + d))_M$	↑	↑	↑	V	S	↑
		10 111 110																
		<d>																
Complement	CPL	00 101 111						S/D		1	3	$\overline{Ar}$→Ar	•	•	S	•	S	•

Special Control Instructions

Table 47. Special Control Instructions

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Special Function	DAA	00 100 111						S/D		1	4	Decimal Adjust Accumulator	↑	↑	↑	P	•	↑
Carry Control	CCF	00 111 111								1	3	$\overline{C}$→C	•	•	R	•	R	↑
	SCF	00 110 111								1	3	1→C	•	•	R	•	R	S
CPU Control	DI	11 110 011								1	3	0→IEF1,0→IEF2 (7)	•	•	•	•	•	•
	EI	11 111 011								1	3	1→IEF1,1→IEF2 (7)	•	•	•	•	•	•
	HALT	01 110 110								1	3	CPU halted	•	•	•	•	•	•
	IM0	11 101 101								2	6	Interrupt	•	•	•	•	•	•
		01 000 110										Mode 0						
	IM1	11 101 101								2	6	Interrupt	•	•	•	•	•	•
		01 010 110										Mode 1						
	IM2	11 101 101								2	6	Interrupt	•	•	•	•	•	•
		01 011 110										Mode 2						
	NOP	00 000 000								1	3	No operation	•	•	•	•	•	•
	SLP**	11 101 101								2	8	Sleep	•	•	•	•	•	•
		01 110 110																

7) Interrupts are not sampled at the end of DI or EI.

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (IX+d),m LD (IY+d),m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	T1T2T3	IX+ d IY+d	DATA	1	0	0	1	1	1	1
LD A, (BC) LD A, (DE)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	BC DE	DATA	0	1	0	1	1	1	1
LD A,(mn)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	T1T2T3	mn	DATA	0	1	0	1	1	1	1
LD (BC),A LD (DE),A	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	BC DE	A	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LDIR LDDR (If BCR≠0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1
	MC5~MC6	TiTi	*	Z	1	1	1	1	1	1	1
LDIR LDDR (If BCR=0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1
MLT ww**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC13	TiTiTTi TiTiTiTi TiTiTi	*	Z	1	1	1	1	1	1	1
NEG	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
NOP	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0

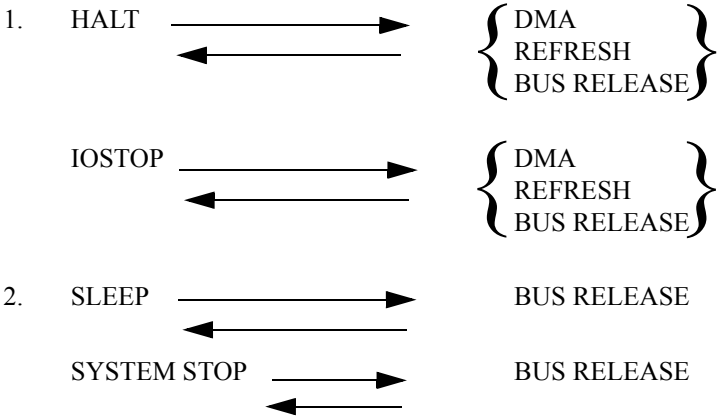
Table 52. Interrupts (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
$\overline{INT0}$ Mode 2	MC1	T1T2TW TWT3	Next Op Code Address (PC)	Vector	1	1	1	0	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP-1	PCH	1	0	0	1	1		1
	MC4	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC5	T1T2T3	I, Vector	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3 T1T2,TW	I, Vector+1	DATA	0	1	0	1	1	1	1
$\overline{INT1}$ $\overline{INT2}$ Internal Interrupts	MC1	T1T2,TW TWT3	Next Op Code Address (PC)		1	1	1	1	1	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC4	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC5	T1T2T3	I, Vector	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3	I, Vector+1	DATA	0	1	0	1	1	1	1

- $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ = 1
  memory to/from (memory mapped)
  I/O DMA transfer
- BCR0, BCR1 = `0000H` (all DMA transfers)
- $\overline{\text{NMI}}$ = 0 (all DMA transfers)

OTHER OPERATION MODE TRANSITIONS

The following operation mode transitions are also possible.



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