Zilog - Z8018008FSC Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008fsc

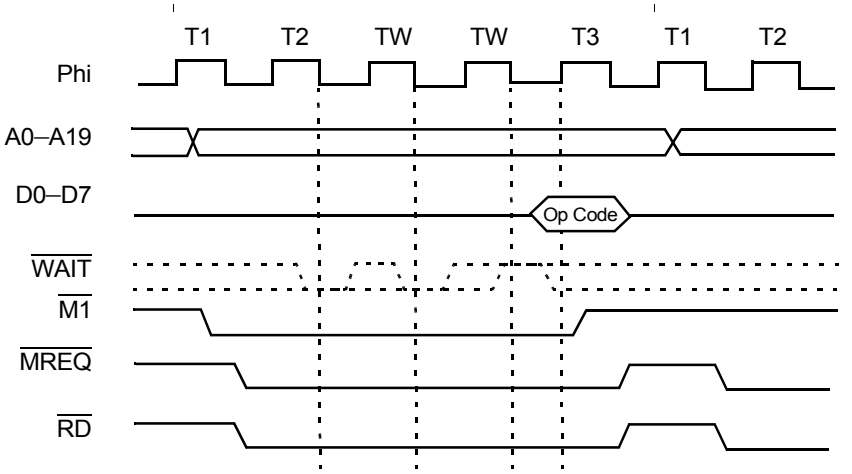

Figure 10. Op Code Fetch (with Wait State) Timing Diagram

Operand and Data Read/Write Timing

The instruction operand and data read/write timing differs from Op Code fetch timing in two ways:

- The $\overline{M1}$ output is held inactive
- The read cycle timing is relaxed by one-half clock cycle because data is latched at the falling edge of T3

Instruction operands include immediate data, displacement, and extended addresses, and contain the same timing as memory data reads.

During memory write cycles the $\overline{MREQ}$ signal goes active in the second half of T1. At the end of T1, the data bus is driven with the write data.

At the start of T2, the $\overline{WR}$ signal is asserted Low enabling the memory. $\overline{MREQ}$ and $\overline{WR}$ go inactive in the second half of T3 followed by disabling of the write data on the data bus.

- Data Bus, 3-state

SLEEP mode is exited in one of two ways as described below.

- RESET Exit from SLEEP mode. If the $\overline{\text{RESET}}$ input is held Low for at least six clock cycles, it exits SLEEP mode and begins the normal RESET sequence with execution starting at address (logical and physical) 00000H.

- Interrupt Exit from SLEEP mode. The SLEEP mode is exited by detection of an external ($\overline{\text{NMI}}$, $\overline{\text{INT0}}$, $\overline{\text{INT2}}$) or internal (ASCI, CSI/O, PRT) interrupt.

In case of $\overline{\text{NMI}}$, SLEEP mode is exited and the CPU begins the normal $\overline{\text{NMI}}$ interrupt response sequence.

In the case of all other interrupts, the interrupt response depends on the state of the global interrupt enable flag IEF1 and the individual interrupt source enable bit.

If the individual interrupt condition is disabled by the corresponding enable bit, occurrence of that interrupt is ignored and the CPU remains in the SLEEP mode.

Assuming the individual interrupt condition is enabled, the response to that interrupt depends on the global interrupt enable flag (IEF1). If interrupts are globally enabled (IEF1 is 1) and an individually enabled interrupt occurs, SLEEP mode is exited and the appropriate normal interrupt response sequence is executed.

If interrupts are globally disabled (IEF1 is 0) and an individually enabled interrupt occurs, SLEEP mode is exited and instruction execution begins with the instruction following the SLP instruction. This feature provides a technique for synchronization with high speed external events without incurring the latency imposed by an interrupt response sequence.

Figure 21 depicts SLEEP timing.

Table 6. I/O Address Map for Z80180-Class Processors Only (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
DMA	DMA Source Address Register Ch 0L	SAR0L	XX100000	20H	93
	DMA Source Address Register Ch 0H	SAR0H	XX100001	21H	93
	DMA Source Address Register Ch 0B	SAR0B	XX100010	22H	93
	DMA Destination Address Register Ch 0L	DAR0L	XX100011	23H	94
	DMA Destination Address Register Ch 0H	DAR0H	XX100100	24H	94
	DMA Destination Address Register Ch 0B	DAR0B	XX100101	25H	94
	DMA Byte Count Register Ch 0L	BCR0L	XX100110	26H	94
	DMA Byte Count Register Ch 0H	BCR0H	XX100111	27H	94
	DMA Memory Address Register Ch 1L	MAR1L	XX101000	28H	94
	DMA Memory Address Register Ch 1H	MAR1H	XX101001	29H	94
	DMA Memory Address Register Ch 1B	MAR1B	XX101010	2AH	94
	DMA I/0 Address Register Ch 1L	IAR1L	XX101011	2BH	102
	DMA I/0 Address Register Ch 1H	IAR1H	XX101100	2CH	102
	Reserved		XX101101	2DH	
	DMA Byte Count Register Ch 1L	BCR1L	XX101110	2EH	94
	DMA Byte Count Register Ch 1H	BCR1H	XX101111	2FH	94
	DMA Status Register	DSTAT	XX110000	30H	95
	DMA Mode Register	DMODE	XX110001	31H	97
	DMA/WAIT Control Register	DCNTL	XX110010	32H	101

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only)

	Register	Mnemonic	Address		
			Binary	Hex	Page
ASCI	ASCI Control Register A Ch 0	CNTLA0	XX000000	00H	125
	ASCI Control Register A Ch 1	CNTLA1	XX000001	01H	128
	ASCI Control Register B Ch 0	CNTLB0	XX000010	02H	132
	ASCI Control Register B Ch 1	CNTLB1	XX000011	03H	132
	ASCI Status Register Ch 0	STAT0	XX000100	04H	120
	ASCI Status Register Ch 1	STAT1	XX000101	05H	123
	ASCI Transmit Data Register Ch 0	TDR0	XX000110	06H	118
	ASCI Transmit Data Register Ch 1	TDR1	XX000111	07H	118
	ASCI Receive Data Register Ch 0	RDR0	XX001000	08H	119
	ASCI Receive Data Register Ch 1	RDR1	XX001001	09H	119
	ASCI0 Extension Control Register 0	ASEXT0	XX010010	12H	135
	ASCI1 Extension Control Register 1	ASEXT1	XX010011	13H	136
	ASCI0 Time Constant Low	ASTC0L	XX011010	1AH	137
	ASCI0 Time Constant High	ASTC0H	XX001011	1BH	137
	ASCI1 Time Constant Low	ASCT1L	XX001100	1CH	138
	ASCI1 Time Constant High	ASCT1H	XX001101	1DH	138
CSI0	CSI0 Control Register	CNTR	XX001010	0AH	147
	CSI0 Transmit/Receive Data Register	TRD	XX1011	0BH	149

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
DMA	DMA Source Address Register Ch 0L	SAR0L	XX100000	20H	93
	DMA Source Address Register Ch 0H	SAR0H	XX100001	21H	93
	DMA Source Address Register Ch 0B	SAR0B	XX100010	22H	93
	DMA Destination Address Register Ch 0L	DAR0L	XX100011	23H	94
	DMA Destination Address Register Ch 0H	DAR0H	XX100100	24H	94
	DMA Destination Address Register Ch 0B	DAR0B	XX100101	25H	94
	DMA Byte Count Register Ch 0L	BCR0L	XX100110	26H	94
	DMA Byte Count Register Ch 0H	BCR0H	XX100111	27H	94
	DMA Memory Address Register Ch 1L	MAR1L	XX101000	28H	94
	DMA Memory Address Register Ch 1H	MAR1H	XX101001	29H	94
	DMA Memory Address Register Ch 1B	MAR1B	XX101010	2AH	94
	DMA I/O Address Register Ch 1L	IAR1L	XX101011	2BH	102
	DMA I/O Address Register Ch 1H	IAR1H	XX101100	2CH	102
	DMA I/O Address Register Ch 1	IAR1B	XX101101	2DH	94
	DMA Byte Count Register Ch 1L	BCR1L	XX101110	2EH	94
	DMA Byte Count Register Ch 1H	BCR1H	XX101111	2FH	94
	DMA Status Register	DSTAT	XX110000	30H	95
	DMA Mode Register	DMODE	XX110001	31H	97
	DMA/WAIT Control Register	DCNTL	XX110010	32H	101

Clock Multiplier Register (CMR: 1EH) (Z8S180/L180-Class Processors Only)

Bit	7	6						0
Bit/Field	X2	Reserved						
R/W	R/W	?						
Reset	0	1						

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	X2 Clock Multiplier Mode	R/W		X2 Clock Multiplier Mode
			0	Disable
			1	Enable
6–0	Reserved	?	?	Reserved

CPU Control Register (CCR: 1FH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Clock Divide	STAND BY/ IDLE Enable	BREXT	LNPHI	STAND BY/ IDLE Enable	LNIO	LNCPU CTL	LNAD/ DATA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	Clock Divide	R/W	0 1	XTAL/2 XTAL/1
6	STANDBY /IDLE Mode	R/W	 00 01 10 11	In conjunction with Bit 3 No STANDBY IDLE after SLEEP STANDBY after SLEEP STANDBY after SLEEP 64 Cycle Exit (Quick Recovery)
5	BREXT	R/W	0 1	Ignore BUSREQ in STANDBY/IDLE STANDBY/IDLE exit on BUSREQ
4	LNPHI	R/W	0 1	Standard Drive 33% Drive on EXTPHI Clock
3	STANDBY /IDLE Mode	R/W	 00 01 10 11	In conjunction with Bit 6 No STANDBY IDLE after SLEEP STANDBY after SLEEP STANDBY after SLEEP 64 Cycle Exit (Quick Recovery)

Table 8. State of IEF1 and IEF2 (Continued)

CPU Operation	IEF1	IEF2	REMARKS
DI	0	0	
LD A, I	not affected	not affected	Transfers the contents of IEF1 to P/V
LID A, R	not affected	not affected	Transfers the contents of IEF1 to P/V

TRAP Interrupt

The Z8X180 generates a non-maskable (not affected by the state of IEF1) TRAP interrupt when an undefined Op Code fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during Op Code fetch cycles and also if an undefined Op Code is fetched during the interrupt acknowledge cycle for $\overline{\text{INT0}}$ when Mode 0 is used.

When a TRAP interrupt occurs the Z8X180 operates as follows:

1. The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to `1`.
2. The current PC (Program Counter) value, reflecting location of the undefined Op Code, is saved on the stack.
3. The Z8X180 vectors to logical address 0. Note that if logical address `0000H` is mapped to physical address `00000H`. the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address `00000H` was caused by RESET or TRAP.

The state of the UFO (Undefined Fetch Object) bit in ITC allows TRAP manipulation software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the Op Code generated the TRAP. If UFO is `0`, the starting address of the invalid instruction is equal to the

DMA Destination Address Register Channel 0 (DAR0 I/O Address = 23H to 25H)

Specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024KB memory addresses or up to 64KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O.

DMA Byte Count Register Channel 0 (BCR0 I/O Address = 26H to 27H)

Specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64KB transfers. When one byte is transferred, the register is decremented by one. If *n* bytes are transferred, *n* is stored before the DMA operation.

DMA Memory Address Register Channel 1 (MAR1: I/O Address = 28H to 2AH)

Specifies the physical memory address for channel 1 transfers. This address may be a destination or source memory address. The register contains 20 bits and may specify up to 1024KB memory address.

DMA I/O Address Register Channel 1 (IAR1: I/O Address = 2BH to 2CH)

Specifies the I/O address for channel 1 transfers. This address may be a destination or source I/O address. The register contains 16 bits and may specify up to 64KB I/O addresses.

DMA Byte Count Register Channel 1 (BCR1: I/O Address = 2EH to 2FH)

Specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64KB transfers. When one byte is transferred, the register is decremented by one.

DMAC Internal Interrupts

Figure 50 illustrates the internal DMA interrupt request generation circuit.

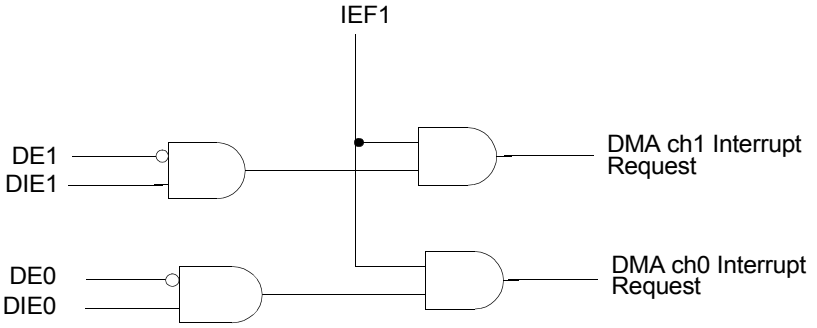

Figure 50. DMA Interrupt Request Generation

DE0 and DE1 are automatically cleared to 0 by the Z8X180 at the completion (byte count is 0) of a DMA operation for channel 0 and channel 1, respectively. They remain 0 until a 1 is written. Because DE0: and DE1 use level sense, an interrupt occurs if the CPU IEF1 flag is set to 1. Therefore, the DMA termination interrupt service routine disables further DMA interrupts (by programming the channel DIE bit is 0) before enabling CPU interrupts (for example, IEF1 is set to 1). After reloading the DMAC address and count registers, the DIE bit can be set to 1 to reenable the channel interrupt, and at the same time DMA can resume by programming the channel DE bit = 1.

DMAC and $\overline{\text{NMI}}$

$\overline{\text{NMI}}$, unlike all other interrupts, automatically disables DMAC operation by clearing the DME bit of DSTAT. Thus, the $\overline{\text{NMI}}$ interrupt service routine responds to time-critical events without delay due to DMAC bus usage. Also, $\overline{\text{NMI}}$ can be effectively used as an external DMA abort input, recognizing that both channels are suspended by the clearing of DME.

Table 19. ASCI Baud Rate Selection

Prescaler		Sampling Rate		Baud Rate				General Divide Ratio	Baud Rate (Example) (BPS)			CKA	
PS	Divide Ratio	DR	Rate	SS2	SS1	SS0	Divide Ratio		ϕ = 6.144 MHz	ϕ = 4.608 MHz	ϕ = 3.072 MHz	I/O	Clock Frequency
0	$\phi \div 10$	0	16	0	0	0	÷1	$\phi \div 160$	38400		19200		$\phi \div 10$
				0	0	1	2	320	19200		9600		20
				0	1	0	4	640	9600		4800		40
				0	1	1	8	1280	4800		2400	0	80
				1	0	0	16	2560	2400		1200		160
				1	0	1	32	5120	1200		600		320
				1	1	0	64	10240	600		300		640
				1	1	1	—	fc ÷ 16	—	—	—	I	fc
		1	64	0	0	0	÷1	0÷640	9600		4800		$\phi \div 10$
				0	0	1	2	1280	4800		2400		20
				0	1	0	4	2560	2400		1200		40
				0	1	1	8	5120	1200		600	0	80
				1	0	0	16	10240	600		300		160
				1	0	1	32	20480	300		150		320
				1	1	0	64	40960	150		75		640
				1	1	1	—	fc ÷ 64	—	—	—	I	fc

Immediate (IMMED)

The memory operands are contained within one or two bytes of the instruction, as depicted in Figure 79.

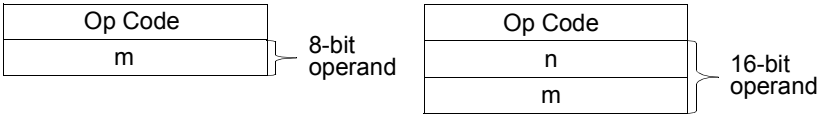

Figure 79. Immediate Addressing

Relative (REL)

Relative addressing mode is only used by the conditional and unconditional branch instructions (refer to Figure 80). The branch displacement (relative to the contents of the program counter) is contained in the instruction.

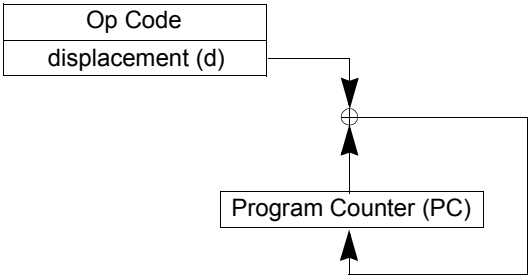

Figure 80. Relative Addressing

Table 39. Rotate and Shift Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	SRL (HL)	11 001 011				S/D				2	3		↑	↑	R	P	R	↑
		00 111 110																
	SRL (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 111 110																
	SRL (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 111 110																
Bit Set	SET b,g	11 001 011				S/D				2	7	1→b•gr	•	•	•	•	•	•
		11 b g																
	SET b,(HL)	11 001 011					S/D			2	13	$1 \rightarrow b \bullet (HL)_M$	•	•	•	•	•	•
		11 b 110																
	SET b,(IX + d)	11 011 101			S/D					4	19	$1 \rightarrow b \bullet (IX + d)_M$	•	•	•	•	•	•
		11 001 011																
		<d>																
		11 b 110																
	SET b,(IY + d)	11 111 101			S/D					4	19	$I \rightarrow b \bullet (IY + d)_M$	•	•	•	•	•	•
		11 001 011																
		<d>																
		11 b 110																
Bit Reset	RES b,g	11 001 011				S/D				2	7	0 →b•gr	•	•	•	•	•	•
		10 b g																
	RES b,(HL)	11 001 011					S/D			2	13	$0 \rightarrow 6 * b \bullet (HL)_M$	•	•	•	•	•	•
		10 b 110																
	RES b,(IX + d)	11 011 101			S/D					4	19	$0 \rightarrow \bullet b \bullet (IX + d)_M$	•	•	•	•	•	•
		11 001 011																
		<d>																
		10 b 110																

Table 40. Arithmetic Instructions (16-bit)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
ADD	ADD HL,ww	00 ww1 001				S		D		1	7	$HL_R + ww_R \rightarrow HL_R$	•	•	X	•	R	↑
	ADD IX,xx	11 011 101 00 xx1 001				S		D		2	10	$IX_R + xx_R \rightarrow {}^*IX_R$	•	•	X	•	R	↑
	ADD IY,yy	11 111 101 00 yy1 001				S		D		2	10	$IY_R + yy_R \rightarrow IY_R$	•	•	X	•	R	↑
ADC	ADC HL,ww	11 101 101 01 ww1 010				S		D		2	10	$HL_R + ww_R + c \rightarrow HL_R$	↑	↑	X	V	R	↑
DEC	DEC ww	00 ww1 011				S/D				1	4	$ww_R - 1 \rightarrow \bullet ww_R$	•	•	•	•	•	•
	DEC IX	11 011 101 00 101 011						S/D		2	7	$1X_R - 1 \rightarrow IX_R$	•	•	•	•	•	•
	DEC IY	11 111 101 00 101 011						S/D		2	7	$1Y_R - 1 \rightarrow IY_R$	•	•	•	•	•	•
INC	INC ww	00 ww 0011				S/D				1	4	$ww_R + 1 \rightarrow ww_R$	•	•	•	•	•	•
	INC IX	11 011 101 00 100 011						S/D		2	7	$1X_R + 1 \rightarrow IX_R$	•	•	•	•	•	•
	INC IY	11 111 101 00 100 011						S/D		2	7	$1Y_R + 1 \rightarrow IY_R$	•	•	•	•	•	•
SBC	SBC HL ww	11 101 101 01 ww0 010				S		D		2	10	$HL_R - ww_R - c \rightarrow HL_R$	↑	↑	X	V	S	↑

PROGRAM AND CONTROL INSTRUCTIONS

Table 45. Program Control Instructions

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Call	CALL mn	11 001 101		D						3	16	$PCHr \rightarrow (SP-1)_M$	•	•	•	•	•	•
		<n>										$PCLr \rightarrow (SP-2)_M$						
		<m>										$mn \rightarrow PC_R$						
												$SP_R-2 \rightarrow SP_R$						
	CALL f,mn	11 f 100		D						3	6 (f : false)	continue : f is false	•	•	•	•	•	•
		<n>									16 (f: true)	CALL mn: f is true						
		<m>																
Jump	DJNZj	00 010 000						D		2	9 (Br ≠ 0)	Br-1→Br	•	•	•	•	•	•
		<j-2>								2	7 (Br = 0)	continue: Br = 0						
												$PC_R + j \rightarrow PC_R$: Br ≠ 0						
	JP f,mn	11 f 010		D						3	6 (f: false)	$mn \rightarrow PC_R$: f is true	•	•	•	•	•	•
		<n>								3	9 (f: true)	continue: f is false						
		<m>																
	JP mn	11 000 011		D						3	9	$mn \rightarrow PC_R$	•	•	•	•	•	•
		<n>																
		<m>																
	JP (HL)	11 101 001					D			1	3	$HL_R \rightarrow PC_R$	•	•	•	•	•	•
	JP (IX)	11 011 101					D			2	6	$IX_R \rightarrow PC_R$	•	•	•	•	•	•
		11 101 001																
	JP (IY)	11 111 101					D			2	6	$IY_R \rightarrow PC_R$	•	•	•	•	•	•
		11 101 001																
	JR j	00 011 000							D	2	8	$PC_R + j \rightarrow PC_R$	•	•	•	•	•	•
		<j-2>																
	JR Cj	00 111 000							D	2	6	continue: C = 0	•	•	•	•	•	•
		<j-2>								2	8	$PC_R + j \rightarrow PC_R$: C = 1						
	JR NCj	00 110 000							D	2	6	continue : C = 1	•	•	•	•	•	•
		<j-2>								2	8	$PC_R + j \rightarrow PC_R$: C = 0						

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
RETI (Z)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0*5 1	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0*5 1	1	1
	MC3 ~MC5	TiTiTi	*	Z	1	1	1	1	1*5 1	1	1
	MC6	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0*5 0	1	1
	MC7	Ti	*	Z	1	1	1	1	1*5 1	1	1
	MC8	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0*5 0	1	1
	MC9	T1T2T3	SP	data	0	1	0	1	1*5 1	1	1
	MC10	T1T2T3	SP+1	data	0	1	0	1	1*5 1	1	1
RLCA RLA RRCA RRA	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
RLC g RL g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
RRC g RR g SLA g SRA g SRL g	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
*5 The upper and lower data show the state of $\overline{M1}$ when $\overline{IOC}$ = 1 and $\overline{IOC}$ = 0 respectively.											

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
RLC (HL) RL (HL) RRC (HL) RR (HL) SLA (HL) SRA (HL) SRL (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	HL	DATA	1	0	0	1	1	1	1
RLC (IX + d) RLC (IY + d) RL (IX + d) RL (IY + d) RRC (IX + d) RRC (IY + d) RR (IX + d) RR (IY + d) SLA (IX + d) SLA (IY + d) SRA (IX + d) SRA (IY + d) SRL (IX + d) SRL (IY + d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2ndOp Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4	T1T2T3	3rd Op Code Address	3rd Op Code	0	1	0	1	0	1	1
	MC5	T1T2T3	IX+d IY+d	DATA	0	1	0	1	1	1	1
	MC6	Ti	*	Z	1	1	1	1	1	1	1
	MC7	T1T2T3	IX+d IY+d	DATA	1	0	0	1	1	1	1
RLD RRD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC7	TiTiTiTi *		Z	1	1	1	1	1	1	1
	MC8	T1T2T3	HL	DATA	1	0	0	1	1	1	1

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)

Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
	CKA0 (External Clock Mode)	Z	IN (A)	IN (N)	IN (N)
	$\overline{\text{DREQ0}}$	Z	IN (N)	IN (A)	IN (N)
TXA1	—	1	OUT	H	H
RXA1	—	IN (N)	IN (A)	IN (N)	IN (N)
CKA1/$\overline{\text{TEND0}}$	CKA1 (Internal Clock Mode)	Z	OUT	Z	Z
	CKA1 (External Clock Mode)	Z	IN (A)	IN (N)	IN (N)
	$\overline{\text{TEND0}}$	Z	1	OUT	1
TXS	—	1	OUT	H	H
RXS/$\overline{\text{CTS}}_1$	RXS	IN (N)	IN (A)	IN (N)	IN (N)
	$\overline{\text{CTS1}}$	IN (N)	IN (A)	IN (N)	IN (N)
CKS	CKS (Internal Clock Mode)	Z	OUT	1	1
	CKS (External Clock Mode)	Z	IN (A)	Z	Z
$\overline{\text{DREQ}}_1$	—	IN (N)	IN (N)	IN (A)	IN (N)
$\overline{\text{TEND}}_1$	—	1	1	OUT	1
$\overline{\text{HALT}}$	—	1	0	OUT	0
$\overline{\text{RFSH}}$	—	1	1	OUT	1
$\overline{\text{IORQ}}$	—	1	1	OUT	1

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
Timer Data Register Channel 1L:	TMDR1L	1	4	
Timer Data Register Channel 1H:	TMDR1H	1	5	
Timer Reload Register Channel 1L	RLDR1L	1	6	
Timer Reload Register Channel 1H:	RLDR1H	1	7	
Free Running Counter:	FRC	1	8	Read only
DMA Source Address Register Channel 0L:	SAR0L	2	0	
DMA Source Address Register Channel 0H:	SAR0H	2	1	
DMA Source Address Register Channel 0B:	SAR0B	2	2	Bits 0-2 (3) are used for SAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — RDR0 (ASCI0) X X 1 0 — RDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Destination Address Register Channel 0L:	DAR0L	2	3	
DMA Destination Address Register Channel 0H:	DAR0H	2	4	
DMA Destination Address Register Channel 0B:	DAR0B	2	5	Bits 0-2 (3) are used for DAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — TDR0 (ASCI0) X X 1 0 — TDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Byte Count Register Channel 0L:	BCROL	2	6	
DMA Byte Count Register Channel 0H:	BCROH	2	7	
DMA Memory Address Register Channel 1L:	MAR1L	2	8	
DMA Memory Address Register Channel 1H:	MAR1H	2	9	

* In the R1 and Z mask, these DMAC registers are expanded from 4 bits to 3 bits in the package version of CP-68.