Zilog - Z8018008FSC00TR Datasheet

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008fsc00tr

Z8018x
Family MPU User Manual

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UM005003-0703

Table 6. I/O Address Map for Z80180-Class Processors Only (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
Timer	Data Register Ch 0 L	TMDR0L	XX001100	0CH	159
	Data Register Ch 0 H	TMDR0H	XX001101	0DH	159
	Reload Register Ch 0 L	RLDR0L	XX001110	0EH	159
	Reload Register Ch 0 H	RLDR0H	XX001111	0FH	159
	Timer Control Register	TCR	XX010000	10H	161
	Reserved		XX010001	11H	
			↕	↕	
			XX010011	13H	
	Data Register Ch 1 L	TMDR1L	XX010100	14H	160
	Data Register Ch 1 H	TMDR1H	XX010101	15H	160
	Reload Register Ch 1 L	RLDR1L	XX010110	16H	159
	Reload Register Ch 1 H	RLDR1H	XX010111	17H	159
Others	Free Running Counter	FRC	XX011000	18H	172
	Reserved		XX011001	19H	
			↕	↕	
			XX011111	1FH	

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only)

	Register	Mnemonic	Address		
			Binary	Hex	Page
ASCI	ASCI Control Register A Ch 0	CNTLA0	XX000000	00H	125
	ASCI Control Register A Ch 1	CNTLA1	XX000001	01H	128
	ASCI Control Register B Ch 0	CNTLB0	XX000010	02H	132
	ASCI Control Register B Ch 1	CNTLB1	XX000011	03H	132
	ASCI Status Register Ch 0	STAT0	XX000100	04H	120
	ASCI Status Register Ch 1	STAT1	XX000101	05H	123
	ASCI Transmit Data Register Ch 0	TDR0	XX000110	06H	118
	ASCI Transmit Data Register Ch 1	TDR1	XX000111	07H	118
	ASCI Receive Data Register Ch 0	RDR0	XX001000	08H	119
	ASCI Receive Data Register Ch 1	RDR1	XX001001	09H	119
	ASCI0 Extension Control Register 0	ASEXT0	XX010010	12H	135
	ASCI1 Extension Control Register 1	ASEXT1	XX010011	13H	136
	ASCI0 Time Constant Low	ASTC0L	XX011010	1AH	137
	ASCI0 Time Constant High	ASTC0H	XX001011	1BH	137
	ASCI1 Time Constant Low	ASCT1L	XX001100	1CH	138
	ASCI1 Time Constant High	ASCT1H	XX001101	1DH	138
CSI0	CSI0 Control Register	CNTR	XX001010	0AH	147
	CSI0 Transmit/Receive Data Register	TRD	XX1011	0BH	149

1. DMAC operation is suspended by the clearing of the DME (DMA Main Enable) bit in DCNTL.

2. The PC is pushed onto the stack.

3. The contents of IEF1 are copied to IEF2. This saves the interrupt reception state that existed prior to $\overline{\text{NMI}}$.

4. IEF1 is cleared to 0. This disables all external and internal maskable interrupts (that is, all interrupts except $\overline{\text{NMI}}$ and TRAP).

5. Execution commences at logical address 0066H.

The last instruction of an $\overline{\text{NMI}}$ service routine must be RETN (Return from Non-maskable Interrupt). This restores the stacked PC, allowing the interrupted program to continue. Furthermore, RETN causes IEF2 to be copied to IEF1, restoring the interrupt reception state that existed prior to $\overline{\text{NMI}}$.

Note: $\overline{\text{NMI}}$, because it can be accepted during Z8X180 on-chip DMAC operation, can be used to externally interrupt DMA transfer. The $\overline{\text{NMI}}$ service routine can reactivate or abort the DMAC operation as required by the application.

For $\overline{\text{NMI}}$, take special care to insure that interrupt inputs do not *overrun* the $\overline{\text{NMI}}$ service routine. Unlimited $\overline{\text{NMI}}$ inputs without a corresponding number of RETN instructions eventually cause stack overflow.

Figure 34 depicts the use of $\overline{\text{NMI}}$ and RETN while Figure 35 details $\overline{\text{NMI}}$ response timing. $\overline{\text{NMI}}$ is edge sensitive and the internally latched $\overline{\text{NMI}}$ falling edge is held until it is sampled. If the falling edge of $\overline{\text{NMI}}$ is latched before the falling edge of the clock state prior to T3 or T1 in the last machine cycle, the internally latched $\overline{\text{NMI}}$ is sampled at the falling edge of the clock state prior to T3 or T1 in the last machine cycle and $\overline{\text{NMI}}$ acknowledge cycle begins at the end of the current machine cycle.

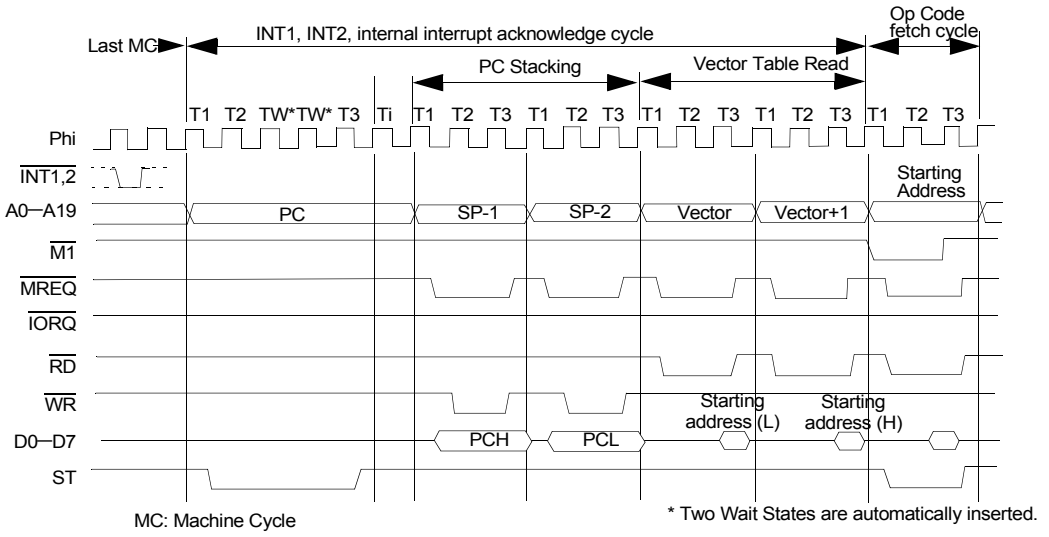

Figure 43. INT1, INT2 and Internal Interrupts Timing Diagram

Dynamic RAM Refresh Control

The Z8X180 incorporates a dynamic RAM refresh control circuit including 8-bit refresh address generation and programmable refresh timing. This circuit generates asynchronous refresh cycles inserted at the programmable interval independent of CPU program execution. For systems which do not use dynamic RAM, the refresh function can be disabled.

When the internal refresh controller determines that a refresh cycle should occur, the current instruction is interrupted at the first breakpoint between machine cycles. The refresh cycle is inserted by placing the refresh address on A0–A7 and the $\overline{\text{RFSH}}$ output is driven Low.

Refresh Control Register (RCR)

The RCR specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

Refresh Control Register (RCR: 36H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	REFE	REFW	?				CYC1	CYC0
R/W	R/W	R/W	?				R/W	R/W
Reset	1	1	?				0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	REFE	R/W		**REFE: Refresh Enable**
			0	Disables the refresh controller
			1	Enables refresh cycle insertion.
6	REFW	R/W		**Refresh Wait** (bit 6)
			0	Causes the refresh cycle to be two clocks in duration.
			1	Causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW).
1–0	CYC1–0	R/W		**Cycle Interval** — CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. In the case of dynamic RAMs requiring 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET. Refer to Table 11.

DMA Destination Address Register Channel 0 (DAR0 I/O Address = 23H to 25H)

Specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024KB memory addresses or up to 64KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O.

DMA Byte Count Register Channel 0 (BCR0 I/O Address = 26H to 27H)

Specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64KB transfers. When one byte is transferred, the register is decremented by one. If *n* bytes are transferred, *n* is stored before the DMA operation.

DMA Memory Address Register Channel 1 (MAR1: I/O Address = 28H to 2AH)

Specifies the physical memory address for channel 1 transfers. This address may be a destination or source memory address. The register contains 20 bits and may specify up to 1024KB memory address.

DMA I/O Address Register Channel 1 (IAR1: I/O Address = 2BH to 2CH)

Specifies the I/O address for channel 1 transfers. This address may be a destination or source I/O address. The register contains 16 bits and may specify up to 64KB I/O addresses.

DMA Byte Count Register Channel 1 (BCR1: I/O Address = 2EH to 2FH)

Specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64KB transfers. When one byte is transferred, the register is decremented by one.

$\overline{\text{DREQ0}}$ for ASCI transmission and reception respectively. To initiate memory to/from ASCI DMA transfer, perform the following operations:

1. Load the source and destination addresses into SAR0 and DAR0 Specify the I/O (ASCI) address as follows:
   a. Bits A0–A7 must contain the address of the ASCI channel transmitter or receiver (I/O addresses 6H-9H).
   b. Bits A8–A15 must equal 0.
   c. Bits SAR17–SAR16 must be set according to Table 16 to enable use of the appropriate ASCI status bit as an internal DMA request.

Table 16. DMA Transfer Request

SAR18	SAR17	SAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	RDRF (ASCI channel 0)
X	1	0	RDRF (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

DAR18	DAR17	DAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	TDRE (ASCI channel O)
X	1	0	TDRE (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

Bit Position	Bit/Field	R/W	Value	Description
7	EF	R		**End Flag** — EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If EIE (End Interrupt Enable) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF is 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.
6	EIE	R/W		**End Interrupt Enable** — EIE is set to 1 to enable EF = 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.
5	RE	R/W		**Receive Enable** — A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external dock mode, the dock is input on the CKS pin. In either case, data is shifted in on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and ISTOP mode. RXS is multiplexed with $\overline{\text{CTS1}}$ modem control input of ASCI channel 1. In order to enable the RXS function, the CTS1E bit in CNTA1 must be reset to 0.

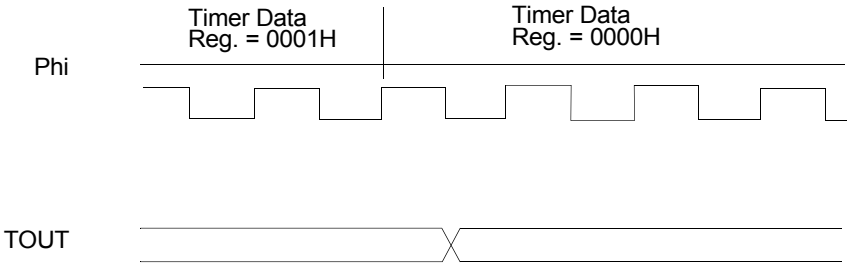

Figure 65. Timer Output Timing Diagram

PRT Interrupts

The PRT interrupt request circuit is illustrated in Figure 66.

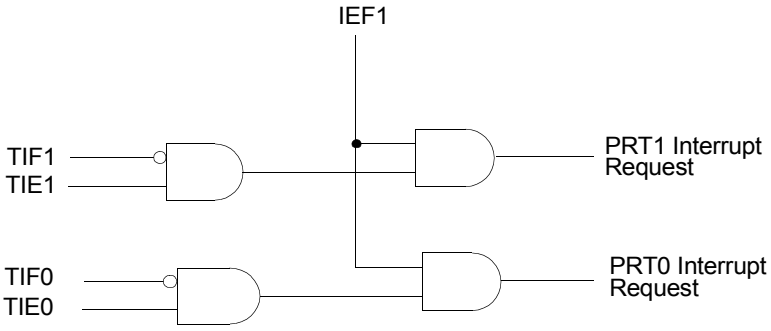

Figure 66. PRT Interrupt Request Generation

PRT and RESET

During RESET, the bits in TCR are initialized as defined in the TCR register description. Down counting is stopped and the TMDR and RLDR registers are initialized to FFFFH. The A18/TOUT pin reverts to the address output function.

Flag Registers (F, F')

The flag registers store status bits (described in the next section) resulting from executed instructions.

General Purpose Registers (BC, BC', DE, DE', HL, HL')

The General Purpose Registers are used for both address and data operation. Depending on the instruction, each half (8 bits) of these registers (B, C, D, E, H, and I) may also be used.

Interrupt Vector Register (I)

For interrupts that require a vector table address to be calculated ($\overline{\text{INT0}}$ Mode 2, $\overline{\text{INT1}}$, $\overline{\text{INT2}}$, and internal interrupts), the Interrupt Vector Register (I) provides the most significant byte of the vector table address. I is cleared to 00H during reset.

R Counter (R)

The least significant seven bits of the R counter (R) count the number of instructions executed by the Z80180. R increments for each CPU Op Code fetch cycle (each $\overline{\text{M1}}$ cycle). R is cleared to 00H during reset.

Index Registers (IX, and IY)

The Index Registers are used for both address and data operations. For addressing, the contents of a displacement specified in the instruction are added to or subtracted from the Index Register to determine an effective operand address.

Z80180 DC CHARACTERISTICS

V_{CC} = 5V ± 10%, V_{SS} = OV, Ta = 0° to +70°C, unless otherwise noted.)

Table 28. Z80180 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VIH1	Input High Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		V_{CC} –0.6	–	V_{CC} +0.3	V
VIH2	Input High Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		2.0		V_{CC} +0.3	V
VIL1	Input Low Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.6	V
VIL2	Input Low Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.8 Standard 7 TL_{VIL}	V
VOH	Output High Voltage all outputs	IOH = –200 µA IOH = –20 µA	2.4 V_{CC} –1.2	– –	– –	V V
VOL	Output Low Voltage all outputs	IOL = 2.2 mA	–	–	0.45	V
I_{IL}	Input Leakage Current all inputs except XTAL, EXTAL	V_{IN} = 0.5~ V_{CC} –0.5	–	–	1.0	µA
ITL	Three-State Leakage Current		–	–	1.0	µA
ICC	Power Dissipation* (Normal Operation)	f = 6 MHz f = 8 MHz f = 33 MHz	– – –	15 20 25	40 50 60	mA mA mA

Instruction Set

This section explains the symbols in the instruction set.

REGISTER

g, g', ww, xx, yy, and zz specify a register to be used. g and g' specify an 8-bit register. ww, xx, yy, and zz specify a pair of 8-bit registers. Table 32 describes the correspondence between symbols and registers.

Table 32. Register Values

g,g'	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

ww	Reg.
00	BC
01	DE
10	HL
11	SP

xx	Reg.
00	BC
01	DE
10	IX
11	SP

yy	Reg.
00	BC
01	DE
10	IY
11	SP

zz	Reg.
00	BC
01	DE
10	HL
11	AF

Note: Suffixed H and L to ww, xx, yy, zz (ex. wwH, IXL) indicate upper and lower 8-bit of the 16-bit register respectively.

BIT

b specifies a bit to be manipulated in the bit manipulation instruction. Table 33 indicates the correspondence between **b** and bits.

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
AND	AND g	10 100 g				S		D		1	4	Ar*gr→Ar	↑	↑	S	P	R	R
	AND (HL)	10 100 110					S	D		1	6	Ar*$(HL)_M$→Ar	↑	↑	S	P	R	R
	AND m	11 100 110	S					D		2	6	Ar*m→Ar	↑	↑	S	P	R	R
		<m>																
	AND (IX + d)	11 011 101			S			D		3	14	Ar*$(1X + d))_M$→Ar	↑	↑	S	P	R	R
		10 100 110																
		<d>																
	AND (IY + d)	11 111 101			S			D		3	14	Ar*(1Y + d)v→Ar	↑	↑	S	P	R	R
		10 100 110																
		<d>																
Compare	CP g	10 111 g				S		D		1	4	Ar-gr	↑	↑	↑	V	S	↑
	CP (HL)	10 111 110					S	D		1	6	Ar-$(HL)_M$	↑	↑	↑	V	S	↑
	CP m	11 111 110	S					D		2	6	Ar-m	↑	↑	↑	V	S	↑
		<m>																
	CP (IX + d)	11 011 101		S				D		3	14	Ar-$(IX + d))_M$	↑	↑	↑	V	S	↑
		10 111 110																
		<d>																
	CP (IY + d)	11 111 101		S				D		3	14	Ar-$(IY + d))_M$	↑	↑	↑	V	S	↑
		10 111 110																
		<d>																
Complement	CPL	00 101 111						S/D		1	3	$\overline{Ar}$→Ar	•	•	S	•	S	•

Table 39. Rotate and Shift Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	SRL (HL)	11 001 011				S/D				2	3		↑	↑	R	P	R	↑
		00 111 110																
	SRL (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 111 110																
	SRL (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 111 110																
Bit Set	SET b,g	11 001 011				S/D				2	7	1→b•gr	•	•	•	•	•	•
		11 b g																
	SET b,(HL)	11 001 011					S/D			2	13	$1 \rightarrow b \bullet (HL)_M$	•	•	•	•	•	•
		11 b 110																
	SET b,(IX + d)	11 011 101			S/D					4	19	$1 \rightarrow b \bullet (IX + d)_M$	•	•	•	•	•	•
		11 001 011																
		<d>																
		11 b 110																
	SET b,(IY + d)	11 111 101			S/D					4	19	$I \rightarrow b \bullet (IY + d)_M$	•	•	•	•	•	•
		11 001 011																
		<d>																
		11 b 110																
Bit Reset	RES b,g	11 001 011				S/D				2	7	0 →b•gr	•	•	•	•	•	•
		10 b g																
	RES b,(HL)	11 001 011					S/D			2	13	$0 \rightarrow 6 * b \bullet (HL)_M$	•	•	•	•	•	•
		10 b 110																
	RES b,(IX + d)	11 011 101			S/D					4	19	$0 \rightarrow \bullet b \bullet (IX + d)_M$	•	•	•	•	•	•
		11 001 011																
		<d>																
		10 b 110																

PROGRAM AND CONTROL INSTRUCTIONS

Table 45. Program Control Instructions

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Call	CALL mn	11 001 101		D						3	16	$PCHr \rightarrow (SP-1)_M$	•	•	•	•	•	•
		<n>										$PCLr \rightarrow (SP-2)_M$						
		<m>										$mn \rightarrow PC_R$						
												$SP_R-2 \rightarrow SP_R$						
	CALL f,mn	11 f 100		D						3	6 (f : false)	continue : f is false	•	•	•	•	•	•
		<n>									16 (f: true)	CALL mn: f is true						
		<m>																
Jump	DJNZj	00 010 000						D		2	9 (Br ≠ 0)	Br-1→Br	•	•	•	•	•	•
		<j-2>								2	7 (Br = 0)	continue: Br = 0						
												$PC_R + j \rightarrow PC_R$: Br ≠ 0						
	JP f,mn	11 f 010		D						3	6 (f: false)	$mn \rightarrow PC_R$: f is true	•	•	•	•	•	•
		<n>								3	9 (f: true)	continue: f is false						
		<m>																
	JP mn	11 000 011		D						3	9	$mn \rightarrow PC_R$	•	•	•	•	•	•
		<n>																
		<m>																
	JP (HL)	11 101 001					D			1	3	$HL_R \rightarrow PC_R$	•	•	•	•	•	•
	JP (IX)	11 011 101					D			2	6	$IX_R \rightarrow PC_R$	•	•	•	•	•	•
		11 101 001																
	JP (IY)	11 111 101					D			2	6	$IY_R \rightarrow PC_R$	•	•	•	•	•	•
		11 101 001																
	JR j	00 011 000							D	2	8	$PC_R + j \rightarrow PC_R$	•	•	•	•	•	•
		<j-2>																
	JR Cj	00 111 000							D	2	6	continue: C = 0	•	•	•	•	•	•
		<j-2>								2	8	$PC_R + j \rightarrow PC_R$: C = 1						
	JR NCj	00 110 000							D	2	6	continue : C = 1	•	•	•	•	•	•
		<j-2>								2	8	$PC_R + j \rightarrow PC_R$: C = 0						

MNEMONICS	Bytes	Machine Cycles	States
	3	6	16 (If condition is true)
CALL mn	3	6	16
CCF	1	1	3
CPD	2	6	12
CPDR	2	8	14 (If $BC_R \neq 0$ and $Ar \neq (HL)_M$
	2	6	12 (If $BC_R = 0$ or $Ar = (HL)_M$
CP (HL)	1	2	6
CPI	2	6	12
CPIR	2	8	14 (If $BC_R \neq 0$ and $Ar \neq (HL)_M$
	2	6	12 (If BCR = 0 or $Ar = (HL)_M$
CP (IX+d)	3	6	14
CP (IY+d)	3	6	14
CPL	1	1	3
CP m	2	2	6
CP g	1	2	4
DAA	1	2	4
DEC (HL)	1	4	10
DEC IX	2	3	7
DEC IY	2	3	7
DEC (IX+d)	3	8	18
DEC (IY+d)	3	8	18
DEC g	1	2	4
DEC ww	1	2	4
DI	1	1	3
DJNZ j	2	5	9 (if Br ≠ 0)

- $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ = 1
  memory to/from (memory mapped)
  I/O DMA transfer
- BCR0, BCR1 = `0000H` (all DMA transfers)
- $\overline{\text{NMI}}$ = 0 (all DMA transfers)

OTHER OPERATION MODE TRANSITIONS

The following operation mode transitions are also possible.

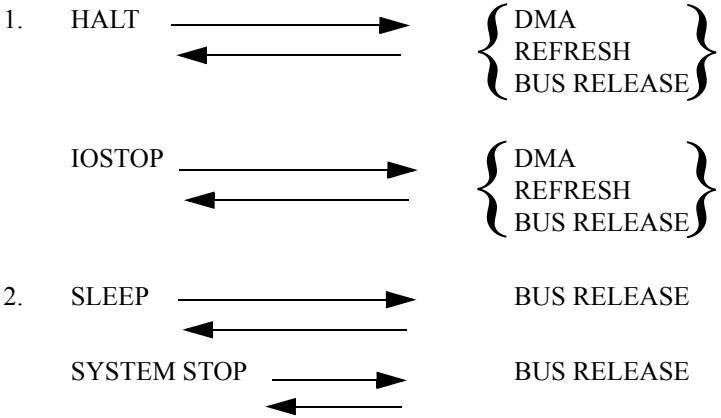

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)

Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
$\overline{\text{MREQ}}$	—	1	1	OUT	1
E	—	0	E Clock Output	←	←
$\overline{\text{M1}}$	—	1	1	OUT	1
$\overline{\text{WR}}$	—	1	1	OUT	1
$\overline{\text{RD}}$	—	1	1	OUT	1
Phi	—	Phi Clock Output	←	←	←

- 1: HIGH 0: LOW A: Programmable Z: High Impedance
- IN (A): Input (Active) IN (N): Input (Not active) OUT: Output
- H: Holds the previous state
- ←: same as the left