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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008pec

PIN DESCRIPTION

A0–A19. *Address Bus (Output, Active High, 3-state).* A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges, up to 1 MB, and I/O data bus exchanges, up to 64K. The address bus enters a high impedance state during RESET and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (TOUT, selected as address output on RESET) and address line A19 is not available in DIP versions of the Z8X180.

$\overline{\text{BUSACK}}$. *Bus Acknowledge (Output, Active Low).* $\overline{\text{BUSACK}}$ indicates that the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

$\overline{\text{BUSREQ}}$. *Bus Request (Input, Active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions and places the address and data buses, and other control signals, into the high impedance state.

CKA0, CKA1. *Asynchronous Clock 0 and 1 (Bidirectional, Active High).* These pins are the transmit and receive clocks for the ASCI channels. CKA0, is multiplexed with $\overline{\text{DREQ0}}$ and CKA1 is multiplexed with $\overline{\text{TEND0}}$.

CKS. *Serial Clock (Bidirectional, Active High).* This line is the clock for the CSIO channel.

CLOCK (PHI). *System Clock (Output, Active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency.

$\overline{\text{CTS0}}$, $\overline{\text{CTS1}}$. *Clear to Send 0 and 1 (Inputs, Active Low).* These lines are modem control signals for the ASCI channels. $\overline{\text{CTS1}}$ is multiplexed with RXS.

D0–D7. *Data Bus (Bidirectional, Active High, 3-state).* D0-D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during RESET and external bus acknowledge cycles.

$\overline{\text{DCD0}}$. *Data Carrier Detect 0 (Input, Active Low).* This input is a programmable modem control signal for ASCI channel 0.

$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$. *DMA Request 0 and 1 (Input, Active Low).* DREQ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a read or write operation. These inputs can be programmed to be either level- or edge-sensed. $\overline{\text{DREQ0}}$ is multiplexed with CKA0.

E. *Enable Clock (Output, Active High).* Synchronous machine cycle clock output during bus transactions.

EXTAL. *External Clock/Crystal (Input, Active High).* Crystal oscillator connection. An external clock can be input to the Z8X180 on this pin when a crystal is not used. This input is Schmitt-triggered.

$\overline{\text{HALT}}$. *Halt/Sleep Status (Output, Active Low).* This output is asserted after the CPU has executed either the $\overline{\text{HALT}}$ or SLP instruction, and is waiting for either non-maskable or maskable interrupt before operation can resume. $\overline{\text{HALT}}$ is also used with the $\overline{\text{M1}}$ and ST signals to decode status of the CPU machine cycle.

$\overline{\text{INT0}}$. *Maskable Interrupt Request 0 (Input, Active Low).* This signal is generated by external I/O devices. The CPU honors this request at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$ and $\overline{\text{BUSREQ}}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ signals become Active.

$\overline{\text{INT1}}$, $\overline{\text{INT2}}$. *Maskable Interrupt Requests 1 and 2 (Inputs, Active Low).* This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$,

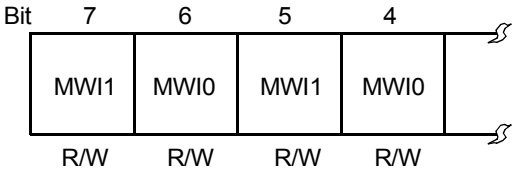


Figure 19. Memory and I/O Wait State Insertion (DCNTL – DMA/Wait Control Register)

The number of Wait States (TW) inserted in a specific cycle is the maximum of the number requested by the $\overline{\text{WAIT}}$ input, and the number automatically generated by the on-chip Wait State generator.

Bit 7, 6: MWI1 MWI0, (Memory Wait Insertion)

For CPU and DMAC cycles which access memory (including memory mapped I/O), zero to three Wait States may be automatically inserted depending on the programmed value in MWI1 and MWI0 as depicted in Table 3

Table 3. Memory Wait States

MW11	MWI0	The Number of Wait States
0	0	0
0	1	1
1	0	2
1	1	3

Bit 5, 4: IWI1, IWI0 (I/O Wait Insertion)

For CPU and DMA cycles which access external I/O (and interrupt acknowledge cycles), one to six Wait States (TW) may be automatically

address to 0. These instructions are IN0, OUT0, OTIM, OTIMR, OTDM, OTDMR and TSTIO (see Instruction Set).

When writing to an internal I/O register, the same I/O write occurs on the external bus. However, the duplicate external I/O write cycle exhibits internal I/O write cycle timing. For example, the $\overline{\text{WAIT}}$ input and programmable Wait State generator are ignored. Similarly, internal I/O read cycles also cause a duplicate external I/O read cycle. However, the external read data is ignored by the Z8X180.

Normally, external I/O addresses should be chosen to avoid overlap with internal I/O addresses and duplicate I/O accesses.

Table 6. I/O Address Map for Z80180-Class Processors Only

	Register	Mnemonic	Address		
			Binary	Hex	Page
ASCI	ASCI Control Register A Ch 0	CNTLA0	XX000000	00H	125
	ASCI Control Register A Ch 1	CNTLA1	XX000001	01H	128
	ASCI Control Register B Ch 0	CNTLB0	XX000010	02H	132
	ASCI Control Register B Ch 1	CNTLB1	XX000011	03H	132
	ASCI Status Register Ch 0	STAT0	XX000100	04H	120
	ASCI Status Register Ch 1	STAT1	XX000101	05H	123
	ASCI Transmit Data Register Ch 0	TDR0	XX000110	06H	118
	ASCI Transmit Data Register Ch 1	TDR1	XX000111	07H	118
	ASCI Receive Data Register Ch 0	RDR0	XX001000	08H	119
	ASCI Receive Data Register Ch 1	RDR1	XX001001	09H	119
CSI/O	CSI/O Control Register	CNTR	XX001010	0AH	147
	CSI/O Transmit/Receive Data Register	TRD	XX1011	0BH	149

The key functions for ASCI on Z80180, Z8S180 and Z8L180 class processors are listed below. Each channel is independently programmable.

- Full-duplex communication
- 7- or 8-bit data length
- Program controlled 9th data bit for multiprocessor communication
- 1 or 2 stop bits
- Odd, even, no parity
- Parity, overrun, framing error detection
- Programmable baud rate generator, /16 and /64 modes
- Modem control signals – Channel 0 contains $\overline{\text{DCD0}}$, $\overline{\text{CTS0}}$ and $\overline{\text{RTS0}}$; Channel 1 contains $\overline{\text{CTS1}}$
- Programmable interrupt condition enable and disable
- Operation with on-chip DMAC

ASCI Block Diagram for the Z8S180/Z8L180-Class Processors

Figure 52 illustrates the ASCI block diagram.

Bit Position	Bit/Field	R/W	Value	Description
4	FE	R		**Framing Error** — If a receive data byte frame is delimited by an invalid stop bit (that is, 0, should be 1), FE is set to 1. FE is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.
3	RIE	R/W		**Receive Interrupt Enable** — RIE must be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, if any of the flags RDRF, OVRN, PE, or FE become set to 1, an interrupt request is generated. For channel 0, an interrupt is also generated by the transition of the external $\overline{\text{DCD0}}$ input from Low to High.
2	CTS1E	R/W		**Channel 1 $\overline{\text{CTS}}$ Enable** — Channel 1 has an external $\overline{\text{CTS1}}$ input which is multiplexed with the receive data pin (RXS) for the CSI/O (Clocked Serial I/O Port). Setting CTS1E to 1 selects the $\overline{\text{CTS1}}$ function and clearing CTS1E to 0 selects the RXS function.
1	TDRE	R		**Transmit Data Register Empty** — TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. When the external $\overline{\text{CTS}}$ input is High, TDRE is reset to 0.
0	TIE	R/W		**Transmit Interrupt Enable** — TIE must be set to 1 to enable ASCI transmit interrupt requests. If TIE is 1, an interrupt is requested when TDRE is 1. TIE is cleared to 0 during RESET.

ASCI0 Extension Control Register (I/O Address: 12H) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
Bit/Field	RDRF Int Inhibit	DCD0 Disable	CTS0 Disable	X1 Bit Clk ASCI0	BRG0 Mode	Break Feature Enable	Break Detect (RO)	Send Break
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	RDRF Interrupt Inhibit	R/W	0 1	RDRF Interrupt Inhibit On RDRF Interrupt Inhibit Off
6	DCD0 Disable	R/W	0 1	DCD0 Auto-enables Rx DCD0 advisory to SW
5	CTS0 Disable	R/W	0 1	CTS0 Auto-enable Tx CTS0 advisory to SW
4	X1 Bit Clk ASCI0	R/W	0 1	CKA0 /16 or /64 CKA0 is bit clock
3	BRG0 Mode	R/W	0 1	As S180 Enable 16-bit BRG counter
2	Break Feature Enable	R/W	0 1	Break Feature Enable On Break Feature Enable Off
1	Break Detect (RO)	R/W	0 1	Break Detect On Break Detect Off

2^ss depends on the three least significant bits of the CNTLB register, as described in Table 21.

Table 21. 2^ss Values

ss2	ss1	ss0	2^ss
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	External Clock from CKA0

The ASCIs require a 50% duty cycle when CKA is used as an input. Minimum High and Low times on CKA0 are typical of most CMOS devices.

RDRF is set, and if enabled, an Rx Interrupt or DMA REquest is generated when the receiver transfers a character from the Rx Shift Register to the RX FIFO. The FIFO provides a margin against overruns. When the is more than one character in the FIFO, and software or a DMA channel reads a character, RDRF either remains set or is cleared and then immediately set again. For example, if a receive interrupt service routine does not real all the characters in the RxFIFO, RDRF and the interrupt request remain asserted.

The Rx DMA request is disabled when any of the error flags PE or FE or OVRN are set, so that software can identify with which character the problem is associated.

If Bit 7, RDRF Interrupt Inhibit, is set to 1, the ASCI does not request a Receive interrupt when its RDRF flag is 1. Set this bit when programming a DMA channel to handle the receive data from an ASCI. The other

causes for an ASCI Receive interrupt (PE, FE, OVRN, and for ASCI0, DCD) continue to request RX interrupt if the RIE bit is 1. The Rx DMA request is inhibited if PE or FE or OVRN is set, so that software can detect where an error occurred. When the RIE bit is 0, as it is after a Reset, RDRF causes an ASCI interrupt if RIE is 1.

Clocked Serial I/O Port (CSI/O)

The Z8X180 includes a simple, high-speed clock, synchronous serial I/O port. The CSI/O includes transmit/receive (half-duplex), fixed 8-bit data, and internal or external data clock selection. High-speed operation (baud rate 200Kbps at fC = 4 MHz) is provided. The CSI/O is ideal for implementing a multiprocessor communication link between multiple Z8X180s. These secondary devices may typically perform a portion of the system I/O processing, (that is, keyboard scan/decode, LDC interface, for instance).

CSI/O Block Diagram

The CSI/O block diagram is illustrated in Figure 57. The CSI/O consists of two registers–the Transmit/Receive Data Register (TRDR) and Control Register (CNTR).

Bit Position	Bit/Field	R/W	Value	Description
7–6	TIF1–0	R		**TIF1: Timer Interrupt Flag** — When TMDR1 decrements to 0, TIF1 is set to 1. This generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0. When TMDR0 decrements to 0, TIF0 is set to 1. This generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.
5–4	TIE1–0	R/W		**Timer Interrupt Enable** — When TIE1 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE1 is reset to 0, the interrupt request is inhibited. During RESET, TIE1 is cleared to 0. When TIE0 is set to 1, TIF0 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.
3–2	TOC1–0	R/W		**Timer Output Control** — TOC1, and TOC0 control the output of PRT1 using the multiplexed A18/TOUT pin as shown in Table 23. During RESET, TOC1 and TOC0 are cleared to 0. This selects the address function for A18/TOUT. By programming TOC1 and TOC0 the A18/TOUT pin can be forced HIGH, LOW, or toggled when TMDR1 decrements to 0. Reference Table 23.
1–0	TDE1–0	R/W		**Timer Down Count Enable** — TDE1 and TDE0 enable and disable down counting for TMDR1 and TMDR0 respectively. When TDEn (n = 0, 1) is set to 1, down counting is executed for TMDRn. When TDEn is reset to 0, down counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

Table 23. Timer Output Control

TOC1	TOC0	OUTPUT	
0	0	Inhibited	(A18/TOUT pin is selected as an address output function.)
0	1	Toggled	
1	0	0	A18/TOUT pin is selected as a PRT1 output function!
1	1	1	

Figure 64 illustrates timer initialization, count down, and reload timing. Figure 65 depicts timer output (A18/TOUT) timing.

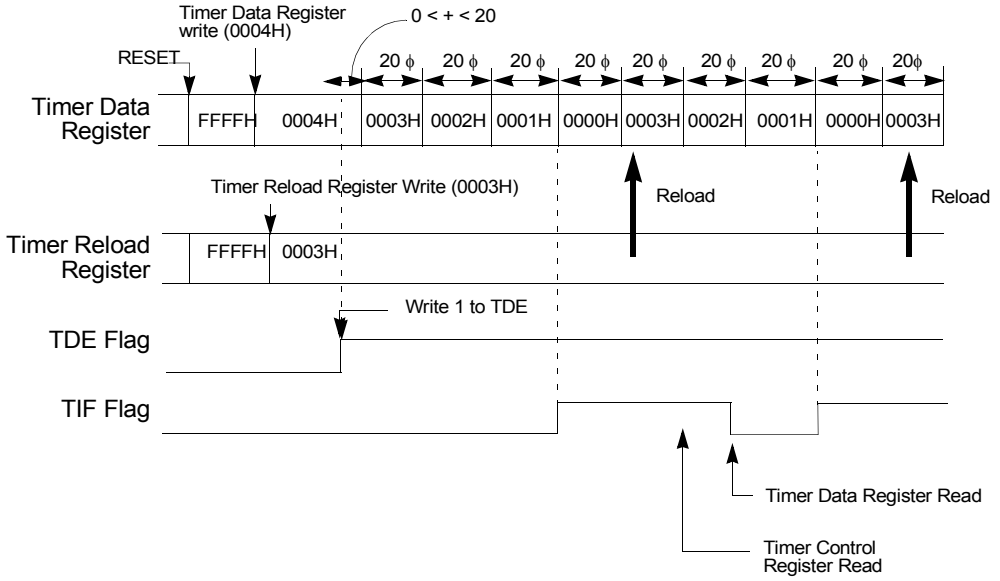


Figure 64. Timer Initialization, Count Down, and Reload Timing Diagram

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
31	t_{INTS}	$\overline{INT}$ Set-up Time to PHI Fall	20	—	15	—	ns
32	t_{INTH}	$\overline{INT}$ Hold Time from PHI Fall	10	—	10	—	ns
33	t_{NMIW}	$\overline{NMI}$ Pulse Width	35	—	25	—	ns
34	t_{BRS}	$\overline{BUSREQ}$ Set-up Time to PHI Fall	10	—	10	—	ns
35	t_{BRH}	$\overline{BUSREQ}$ Hold Time from PHI Fall	10	—	10		ns
36	t_{BAD1}	PHI Rise to $\overline{BUSACK}$ Fall Delay	—	25	—	15	ns
37	t_{BAD2}	PHI Fall to $\overline{BUSACK}$ Rise Delay	—	25	—	15	ns
38	t_{BZD}	PHI Rise to Bus Floating Delay Time	—	40	—	30	ns
39	t_{MEWH}	$\overline{MREQ}$ Pulse Width (High)	35	—	25	—	ns
40	t_{MEWL}	$\overline{MREQ}$ Pulse Width (Low)	35	—	25	—	ns
41	t_{RFD1}	PHI Rise to $\overline{RFSH}$ Fall Delay	—	20	—	15	ns
42	t_{RFD2}	PHI Rise to $\overline{RFSH}$ Rise Delay	—	20	—	15	ns
43	t_{HAD1}	PHI Rise to $\overline{HALT}$ Fall Delay	—	15	—	15	ns
44	t_{HAD2}	PHI Rise to $\overline{HALT}$ Rise Delay	—	15	—	15	ns
45	t_{DRQS}	$\overline{DREQ1}$ Set-up Time to PHI Rise	20	—	15	—	ns
46	t_{DRQH}	$\overline{DREQ1}$ Hold Time from PHI Rise	20	—	15	—	ns
47	t_{TED1}	PHI Fall to $\overline{TENDi}$ Fall Delay	—	25	—	15	ns
48	t_{TED2}	PHI Fall to $\overline{TENDi}$ Rise Delay	—	25	—	15	ns
49	t_{ED1}	PHI Rise to E Rise Delay	—	30	—	15	ns
50	t_{ED2}	PHI Fall or Rise to E Fall Delay	—	30	—	15	ns
51	P_{WEH}	E Pulse Width (High)	25	—	20	—	ns
52	P_{WEL}	E Pulse Width (Low)	50	—	40	—	ns
53	t_{Er}	Enable Rise Time	—	10	—	10	ns

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
54	t_{Ef}	Enable Fall Time	—	10	—	10	ns
55	t_{TOD}	PHI Fall to Timer Output Delay	—	75	—	50	ns
56	t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	2	—	2	tcyc
57	t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	7.5 t_{CY} C +75	—	75 t_{CYC} +60	ns
58	t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	tcyc
59	t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	tcyc
60	t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	tcyc
61	t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	tcyc
62	t_{RES}	$\overline{\text{RESET}}$ Set-up Time to PHI Fall	40	—	25	—	ns
63	t_{REH}	$\overline{\text{RESET}}$ Hold Time from PHI Fall	25	—	15	—	ns
64	t_{OSC}	Oscillator Stabilization Time	—	20	—	20	ns
65	t_{EXR}	External Clock Rise Time (EXTAL)	—	5	—	5	ns
66	t_{EXF}	External Clock Fall Time (EXTAL)	—	5	—	5	ns
67	t_{RR}	$\overline{\text{RESET}}$ Rise Time	—	50	—	50	ms
68	t_{RF}	$\overline{\text{RESET}}$ Fall Time	—	50	—	50	ms

STANDARD TEST CONDITIONS

The previous DC Characteristics and Capacitance sections apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows in to the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

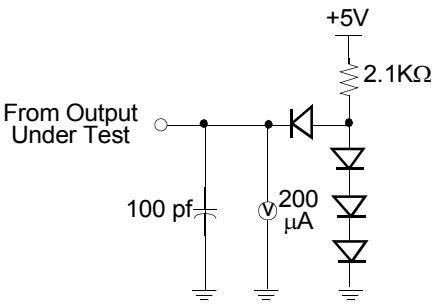


Figure 93. Test Setup

Table 39. Rotate and Shift Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
		11 001 011																
		<d>																
		00 001 110																
	RRD	11 101 101						S/D		2	16		↑	↑	R	P	R	•
		01 100 111										Ar b7 b0						
	SLA g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 100 g																
	SLA (HL)	11 001 011					S/D			2	13	(HL)M b7 b0	↑	↑	R	P	R	↑
		00 100 110																
	SLA (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011										C b7 b0 0						
		<d>																
		00 100 110																
	SLA (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 100 110																
	SRA g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 101 g																
	SRA (HL)	11 001 011					S/D			2	13	b7 b0 C	↑	↑	R	P	R	↑
		00 101 110																
	SRA (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 101 110																
	SRA (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 101 110																
	SRL g	11 001 011				S/D				2	7	0 b7 b0 C	↑	↑	R	P	R	↑
		00 111 g																

Table 41. 8-Bit Load (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7 S	6 Z	4 H	2 P/V	1 N	0 C
Load 8-Bit Data	LD (IX + d),m	11 011 101 00 110 110 <d>	S		D					4	15	$m \rightarrow (IX + d)_M$	•	•	•	•	•	•
	LD (IY + d),m	11 111 101 01 110 g <d> <m>	S		D					4	15	$m \rightarrow (IY + d)_M$	•	•	•	•	•	•
	LD (HL),g	01 110 g				S	D			1	7	$gr \rightarrow (HL)_M$	•	•	•	•	•	•
	LD (IX + d),g	11 011 101 01 110 g <d>			D	S				3	15	$gr \rightarrow (IX+d)_M$	•	•	•	•	•	•
	LD (IY + d),g	11 111 101 01 110 g <d>			D	S				3	15	$gr \rightarrow (IY + d)_M$	•	•	•	•	•	•
(1) In the case of R1 and Z Mask, interrupts are not sampled at the end of LD A, I or LD A,R.																		

Table 42. 16-Bit Load

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7 S	6 Z	4 H	2 P/V	1 N	0 C
Load 16-Bit Data	LD ww,mn	00 ww0 001 <n> <m>	S			D				3	9	$mn \rightarrow ww_R$	•	•	•	•	•	•
	LD IX,mn	11 011 101 00 100 001 <n> <m>	S					D		4	12	$mn \rightarrow IX_R$	•	•	•	•	•	•

Table 43. Block Transfer (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	CPI	11101101					S	S		2	12	Ar-$(HL)_M$	↑	↑	↑	↑	S	•
		10100001										BC_R-1→BC_R						
												HL_R + 1→HL_R		(3)		(2)		
	CPIR	11101101					S	S		2	14	$BC_R \neq 0$ Ar*$(HL)_M$	↑	↑	↑	↑	S	•
		10110001									12	BC_R = 0 or Ar = $(HL)_M$						
												Q: Ar-$(HL)_M$; BC_R-1→BC_R; HL_R + 1→HL_R						
												Repeat Q until						
												Ar = $(HL)_M$ or BC_R = 0				(2)		
	LDD	11 101 101					S/D			2	12	$(HL)_M \rightarrow (DE)_M$	•	•	R	↑	R	•
		10 101 000										BC_R -1→BC_R						
												DE_R-1→DE_R						
												HL_R-1→HL_R						
	LDDR	11 101 101					S/D			2	14($BC_R \neq 0$)	Q: $(HL)_M \rightarrow (DE)_M$; BC_R -1 → BC_R; DE_R -1 → DE_R; HL_R -1 → HL_R	•	•	R	R	R	•
		10 111 000									12(BC_R = 0)	Repeat Q until						
												BC_R = 0				(2)		
	LDI	11 101 101					S/D			2	12	$(HL)_M \rightarrow (DE)_R$	•	•	R	↑	R	•
		10 100 000										BC_R-1→BC_R						
												DE_R + 1→DE_R						
												HL_R + 1→HL_R						
	LDIR	11 101 101					S/D			2	14($BC_R \neq 0$)	Q: $(HL)_M \rightarrow (DE)_M$; BC_R-1→BC_R; DE_R + 1→DE_R; HL_R + 1→HL_R	•	•	R	R	R	•
		10 110 000									12(BC_R = 0)	Repeat Q until						
												BC_R = 0						

(2) P/V = 0: BC_R-1 = 0
P/V = 1: BC_R-1 ≠ 0
(3) Z = 1: Ar = $(HL)_M$
Z = 0 :Ar ≠ $(HL)_M$

Note 1: (HL) replaces g.

Note 2: (HL) replaces s.

Note 3: If DDH is supplemented as first Op Code for the instructions which have HL or (HL) as an operand in Table 48, the instructions are executed replacing HL with IX and (HL) with (IX+d).

```
ex. 22H : LD (mn), HL
```

```
DDH 22H : LD (mn), IX
```

If FDH is supplemented as 1st Op Code for the instructions which have HL or (HL) as an operand in Table 48, the instructions are executed replacing HL with IY and (HL) with (IY+d).

```
ex. 34H : INC (HL)
```

```
FDH 34H : INC (IY+d)
```

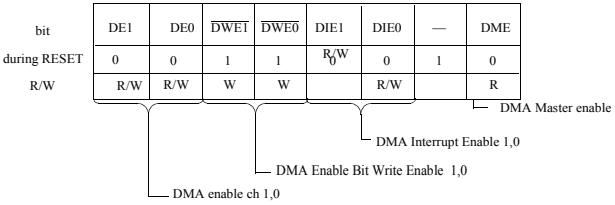
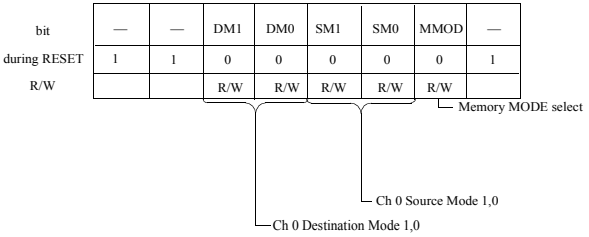
However, JP (HL) and EX DE, HL are exceptions and note the following.

- If DDH is supplemented as 1st Op Code for JP (HL), (IX) replaces (HL) as operand and JP (IX) is executed
- If FDH is supplemented as 1st Op Code for JP (HL), (IY) replaces (HL) as operand and JP (IY) is executed
- Even if DDH or FDH is supplemented as 1st Op Code for EX DE, HL, HL is not replaced and the instruction is regarded as illegal instruction.

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (mn),IX LD (mn),IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	Ti	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	mn	IXL IYL	1	0	0	1	1	1	1
	MC7	T1T2T3	mn+1	IXH IYH	1	0	0	1	1	1	1
LD SP, HL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
LD SP,IX LD SP,IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
LDI LDD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
DMA Memory Address Register Channel 1B:	MAR1B	2	A	Bits 0 - 2 are used for MAR1B
DMA I/O Address Register Channel 1L:	IAR1L	2	B	
DMA I/O Address Register Channel 1H	IAR1H	2	C	
DMA Byte Count Register Channel 1L:	BCR1L	2	E	
DMA Byte Count Register Channel 1H:	BCR1H	2	F	
DMA Status Register:	DSTAT	3	0	
DMA Mode Register:	DMODE	3	1	

DM1,0	Destination	Address
0 0	M	DAR0+1
0 1	M	DAR0-1
1 0	M	DAR0 fixed
1 1	I/O	DAR0 fixed

SM1,0	Source	Address
0 0	M	SAR0+1
0 1	M	SAR0-1
1 0	M	SAR0 fixed
1 1	I/O	SAR0 fixed

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode