Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008peg

Z8018x
Family MPU User Manual

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact

ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

UM005003-0703

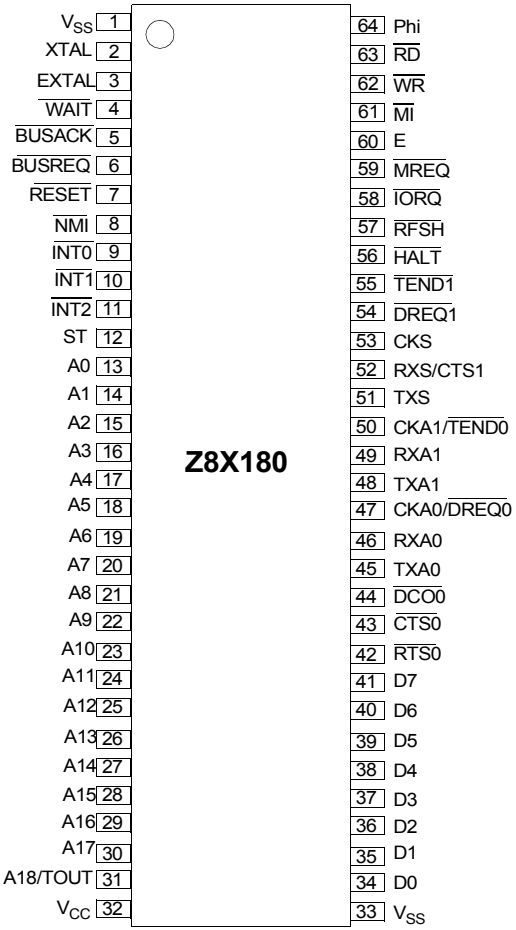


Figure 1. 64-Pin DIP

Low Power Modes (Z8S180/Z8L180 only)

The following section is a detailed description of the enhancements to the Z8S180/L180 from the standard Z80180 in the areas of STANDBY, IDLE and STANDBY QUICK RECOVERY modes.

Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce current consumption. The Z8S180 features two additional power-down modes, STANDBY and IDLE, to reduce current consumption even further. The differences in these power-down modes are summarized in Table 5.

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the $\overline{\text{BUSREQ}}$ does not cause the Z8S180/Z8L180-class processors to exit STANDBY mode.

If STANDBY mode is exited because of a reset or an external interrupt, the Z8S180/Z8L180-class processors remains relinquished from the system bus as long as $\overline{\text{BUSREQ}}$ is active.

STANDBY Mode EXit with External Interrupts

STANDBY mode can be exited by asserting input $\overline{\text{NMI}}$. The STANDBY mode may also exit by asserting $\overline{\text{INT0}}$. $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$, depending on the conditions specified in the following paragraphs.

$\overline{\text{INT0}}$ wake-up requires assertion throughout duration of clock stabilization time (2^{17} clocks).

If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize, before the internal clocking and the system clock output within the Z8S180/Z8L180-class processors resume.

- Exit with Non-Maskable Interrupts

  If $\overline{\text{NMI}}$ is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.

- Exit with External Maskable Interrupts

  If an External Maskable Interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit) and the settings of the corresponding interrupt enable bit in the Interrupt/Trap Control Register (ITC: I/O Address = 34H).

If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input does not cause the Z8S180/Z8L180-class processors to exit STANDBY mode. This condition is true regardless of the state of the Global Interrupt Enable Flag IEF1.

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only)

	Register	Mnemonic	Address		
			Binary	Hex	Page
ASCI	ASCI Control Register A Ch 0	CNTLA0	XX000000	00H	125
	ASCI Control Register A Ch 1	CNTLA1	XX000001	01H	128
	ASCI Control Register B Ch 0	CNTLB0	XX000010	02H	132
	ASCI Control Register B Ch 1	CNTLB1	XX000011	03H	132
	ASCI Status Register Ch 0	STAT0	XX000100	04H	120
	ASCI Status Register Ch 1	STAT1	XX000101	05H	123
	ASCI Transmit Data Register Ch 0	TDR0	XX000110	06H	118
	ASCI Transmit Data Register Ch 1	TDR1	XX000111	07H	118
	ASCI Receive Data Register Ch 0	RDR0	XX001000	08H	119
	ASCI Receive Data Register Ch 1	RDR1	XX001001	09H	119
	ASCI0 Extension Control Register 0	ASEXT0	XX010010	12H	135
	ASCI1 Extension Control Register 1	ASEXT1	XX010011	13H	136
	ASCI0 Time Constant Low	ASTC0L	XX011010	1AH	137
	ASCI0 Time Constant High	ASTC0H	XX001011	1BH	137
	ASCI1 Time Constant Low	ASCT1L	XX001100	1CH	138
	ASCI1 Time Constant High	ASCT1H	XX001101	1DH	138
CSI0	CSI0 Control Register	CNTR	XX001010	0AH	147
	CSI0 Transmit/Receive Data Register	TRD	XX1011	0BH	149

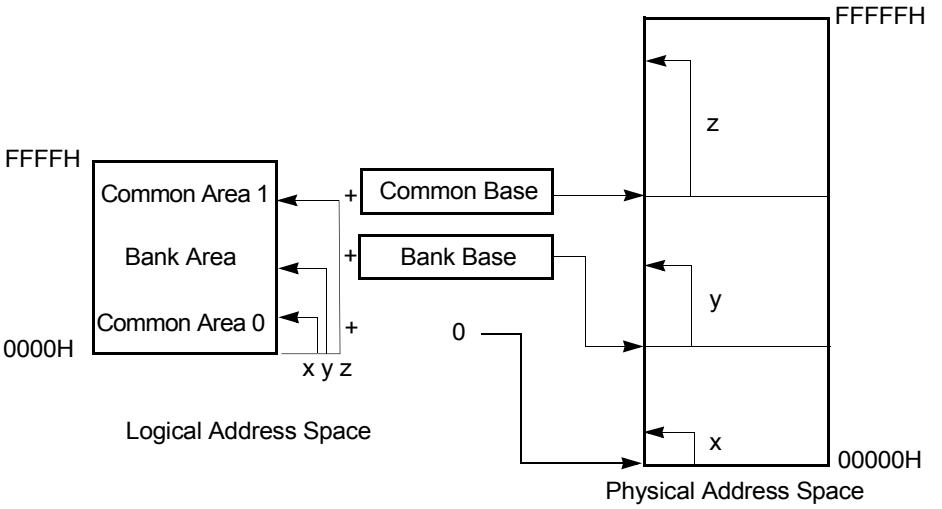


Figure 24. Physical Address Transition

MMU Block Diagram

The MMU block diagram is depicted in Figure 25. The MMU translates internal 16-bit logical addresses to external 20-bit physical addresses.

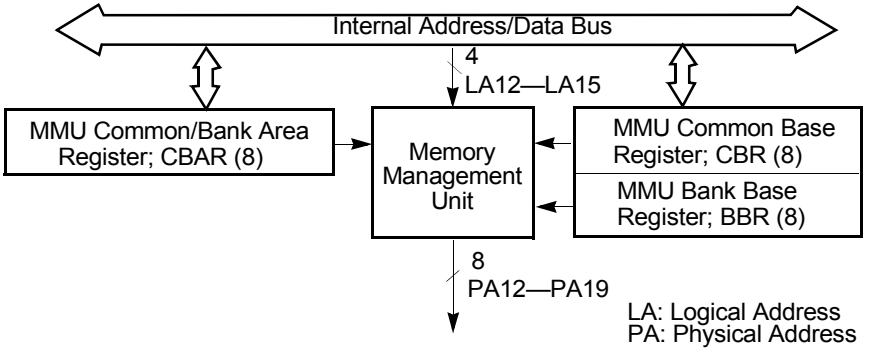


Figure 25. MMU Block Diagram

Table 13. Channel 0 Source

SM1	SM0	Memory/I/O	Address Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	-1
1	0	Memory	fixed
1	1	I/O	fixed

Table 14 describes all DMA TRANSFER mode combinations of DM0 DM1, SM0 SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 14. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Increment/Decrement
0	0	0	0	Memory to Memory	SAR0+1, DAR0+1
0	0	0	1	Memory to Memory	SAR0-1, DAR0+1
0	0	1	0	Memory* to Memory	SAR0 fixed, DAR0+ 1
0	0	1	1	I/O to Memory	SAR0 fixed DAR0+1
0	1	0	0	Memory to Memory	SAR0+1, DAR0-1
0	1	0	1	Memory to Memory	SAR0-1,DAR0-1
0	1	1	0	Memory to Memory	SAR0 fixed, DAR0-1
0	1	1	1	I/O to Memory	SAR0 fixed. DAR0-1
1	0	0	0	Memory to Memory*	SAR0+ 1, DAR0 fixed
1	0	0	1	Memory to Memory*	SAR0-1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	

4. Specify whether $\overline{\text{DREQ1}}$ is level- or edge- sense in the DMS1 bit in DCNTL.
5. Enable or disable DMA termination interrupt with the DIE1 bit in DSTAT.
6. Program DE1 = 1 (with $\overline{\text{DWE1}}$ = 0 in the same access) in DSTAT and the DMA operation with the external I/O device begins using the external $\overline{\text{DREQ1}}$ input and $\overline{\text{TEND1}}$ output.

DMA Bus Timing

When memory (and memory mapped I/O) is specified as a source or destination, $\overline{\text{MREQ}}$ goes Low during the memory access. When I/O is specified as a source or destination, $\overline{\text{IORQ}}$ goes Low during the I/O access.

When I/O (and memory mapped I/O) is specified as a source or destination, the DMA timing is controlled by the external $\overline{\text{DREQ}}$ input and the $\overline{\text{TEND}}$ output indicates DMA termination

Note: External I/O devices may not overlap addresses with internal I/O and control registers, even using DMA.

For I/O accesses, one Wait State is automatically inserted. Additional Wait States can be inserted by programming the on-chip wait state generator or using the external $\overline{\text{WAIT}}$ input.

Note: For memory mapped I/O accesses, this automatic I/O Wait State is not inserted.

For memory to memory transfers (channel 0 only), the external $\overline{\text{DREQ0}}$ input is ignored. Automatic DMA timing is programmed as either BURST or CYCLE STEAL.

When a DMA memory address carry/borrow between bits A15 and A16 of the address bus occurs (crossing 64KB boundaries), the minimum bus

ASCI Control Register A0, 1 (CNTLA0, 1)

Each ASCI channel Control Register A configures the major operating modes such as receiver/transmitter enable and disable, data format, and multiprocessor communication mode.

ASCI Status Register 1 (STAT1: 05H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
R/W	R	R	R	R	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	RDRF	R		**Receive Data Register Full** — RDRF is set to 1 when an incoming data byte is loaded into RDR. Note that if a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into RDR. RDRF is cleared to 0 by reading RDR, when the DCD0 input is High, in IOSTOP mode, and during RESET.
6	OVRN	R		**Overrun Error** — OVRN is set to 1 when RDR is full and RSR becomes full. OVRN is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.
5	PE	R		**Parity Error** — PE is set to 1 when a parity error is detected on an incoming data byte and ASCI parity detection is enabled (the MOD1 bit of CNTLA is set to 1). PE is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.

control register. The PRT input clock for both channels is equal to the system clock divided by 20.

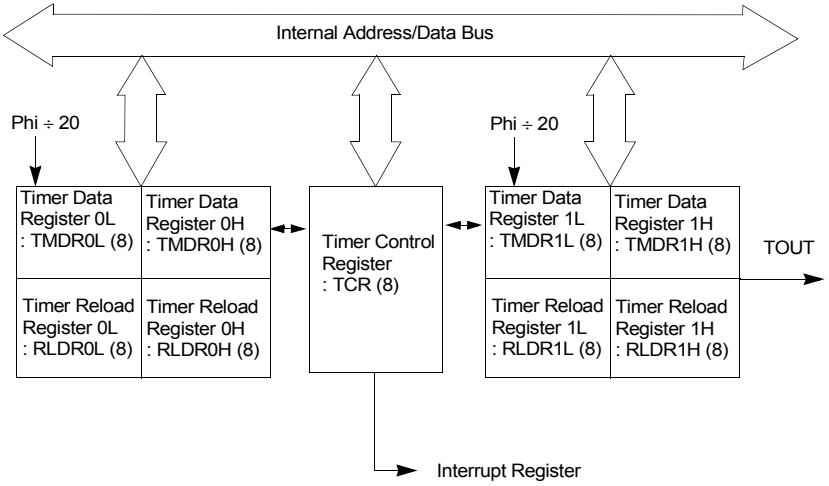


Figure 63. PRT Block Diagram

PRT Register Description

Timer Data Register (TMDR: I/O Address - CH0: 0CH, 0DH; CH1: 15H, 14H). PRT0 and PRT1 each contain 16-bit timer Data Registers (TMDR). TMDR0 and TMDR1 are each accessed as low and high byte registers (TMDR0H, TMDR0L and TMDR1H, TMDR1L). During RESET, TMDR0 and TMDR1 are set to FFFFH.

TMDR is decremented once every twenty clocks. When TMDR counts down to 0, it is automatically reloaded with the value contained in the Reload Register (RLDR).

TMDR is read and written by software using the following procedures. The read procedure uses a PRT internal temporary storage register to

Stack Pointer (SP)

The Stack Pointer (SP) contains the memory address based LIFO stack. SP is cleared to 0000H during reset.

Program Counter (PC)

The Program Counter (PC) contains the address of the instruction to be executed and is automatically updated after each instruction fetch. PC is cleared to 0000H during reset.

Flag Register (F)

The Flag Register stores the logical state reflecting the results of instruction execution. The contents of the Flag Register are used to control program flow and instruction operation.

Flag Register

Bit	7	6	5	4	3	2	1	0
Bit/Field	S	Z	Not Used	H	Not Used	P/V	N	C
R/W	R/W	R/W	?	R/W	?	R/W	R/W	R/W
Reset	0	0	?	0	?	0	0	0

R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	S	R/W	0	**Sign.** S stores the state of the most significant bit (bit 7) of the result. This is useful for operations with signed numbers in which values with bit 7 = 1 are interpreted as negative.

Z80180 DC CHARACTERISTICS

V_{CC} = 5V ± 10%, V_{SS} = OV, Ta = 0° to +70°C, unless otherwise noted.)

Table 28. Z80180 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VIH1	Input High Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		V_{CC} –0.6	–	V_{CC} +0.3	V
VIH2	Input High Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		2.0		V_{CC} +0.3	V
VIL1	Input Low Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.6	V
VIL2	Input Low Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.8 Standard 7 TL_{VIL}	V
VOH	Output High Voltage all outputs	IOH = –200 µA IOH = –20 µA	2.4 V_{CC} –1.2	– –	– –	V V
VOL	Output Low Voltage all outputs	IOL = 2.2 mA	–	–	0.45	V
I_{IL}	Input Leakage Current all inputs except XTAL, EXTAL	V_{IN} = 0.5~ V_{CC} –0.5	–	–	1.0	µA
ITL	Three-State Leakage Current		–	–	1.0	µA
ICC	Power Dissipation* (Normal Operation)	f = 6 MHz f = 8 MHz f = 33 MHz	– – –	15 20 25	40 50 60	mA mA mA

Table 29. Z8S180 DC Characteristics (Continued)

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VOH1	Output High Voltage All outputs	IOH = –200 µA IOH = –20 µA	2.4 V_{CC} –1.2	– –	– –	V V
VOH2	Output High Voltage Output High Phi	IOH = –200 µA	V_{CC} –0.6			
VOL1	Output Low Voltage All outputs	IOL = 2.2 mA	–	–	0.45	V
VOL2	Output Low Voltage Output Low Phi	IOL = 2.2 mA	–	–	0.45	V
IIL	Input Leakage Current all inputs except XTAL, ETAL	VIN = 0.5 ~ VCC –0.5	–	–	1.0	µA
ITL	Three-State Leakage Current	VIN = 0.5 ~ VCC –0.5	–	–	1.0	µA
ICC	Power Dissipation* (Normal Operation)	f = 10 MHz f = 20 MHz f = 33 MHz	–	15 30 60	– 50 100	mA
	Power Dissipation* (SYSTEM STOP Mode)	f = 10 MHz f = 20 MHz f = 33 MHz	–	1.5 3 5	– 6 9	mA
	Power Dissipation* (IDLE Mode)	f = 20 MHz f = 33 MHz	–	4	10	mA
	Power Dissipation* (STANDBY Mode)	External Oscillator, Internal Clock Stops	–	5	10	µA
CP	Pin Capacitance	VIN = 0V, f = 1MHz TA = 25°C	–	–	12	pF

Notes: * VIN min = V_{CC} –1.0V. VIL max = 0.8V (All output terminals are a no load.)
V_{CC} = 5.0V

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
12	t_{MED2}	PHI Fall to $\overline{MREQ}$ Rise Delay	—	25	—	15	ns
13	t_{RDD2}	PHI Fall to $\overline{RD}$ Rise Delay	—	25	—	15	ns
14	t_{M1D2}	PHI Rise to $\overline{M1}$ Rise Delay	—	40	—	15	ns
15	t_{DRS}	Data Read Set-up Time	10	—	5	—	ns
16	t_{DRH}	Data Read Hold Time	0	—	0	—	ns
17	t_{STD1}	PHI Fall to ST Fall Delay	—	30	—	15	ns
18	t_{STD2}	PHI Fall to ST Rise Delay	—	30	—	15	ns
19	t_{WS}	$\overline{WAIT}$ Set-up Time to PHI Fall	15	—	10	—	ns
20	t_{WH}	$\overline{WAIT}$ Hold Time from PHI Fall	10	—	5	—	ns
21	t_{WDZ}	PHI Rise to Data Float Delay	—	35	—	20	ns
22	t_{WRD1}	PHI Rise to $\overline{WR}$ Fall Delay	—	25	—	15	ns
23	t_{WDD}	PHI Fall to Write Data Delay Time	—	25	—	15	ns
24	t_{WDS}	Write Data Set-up Time to $\overline{WR}$ Fall	10	—	10	—	ns
25	t_{WRD2}	PHI Fall to $\overline{WR}$ Rise Delay	—	25	—	15	ns
26	t_{WRP}	$\overline{WR}$ Pulse Width (Memory Write Cycle)	80	—	45	—	ns
26a		$\overline{WR}$ Pulse Width (I/O Write Cycle)	150	—	70	—	ns
27	t_{WDH}	Write Data Hold Time from $\overline{WR}$ Rise	10	—	5	—	ns
28	t_{IOD1}	PHI Fall to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 0	—	25	—	15	
29	t_{IOD2}	PHI Fall to $\overline{IORQ}$ Rise Delay	—	25	—	15	ns
30	t_{IOD3}	$\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay	125	—	80	—	ns

Table 46. I/O Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	OTIMR**	11 101 101 10 010 011					S		D	2	16 (Br ≠ 0) 14 (Br = 0)	$(HL)_M \rightarrow (00C)_I$ $HL_R + 1 \rightarrow HL_R$ Q $Cr + 1 \rightarrow Cr$ $Br-1 \rightarrow Br$ Repeat Q until Br = 0 $Cr \rightarrow A0 \sim A7$ $00 \rightarrow A8 \sim A16$	R	S (5)	R	S	↑ (6)	R
	OUTD	11 101 101 10 101 011						S	D	2	12	$(HL)_M \rightarrow (BC)_1$ $HL_R-1 \rightarrow HL_R$ $Br-1 \rightarrow Br$ $Cr \rightarrow A0 \sim A7$ $Br \rightarrow A8 \sim A16$	X	↑	X	X	↑	X

(5) Z = 1 : Br-1 = 0
Z = 0 : Br-1 ≠ 0
(6) N = 1: MSB of Data = 1
N = 0 : MSB of Data = 0

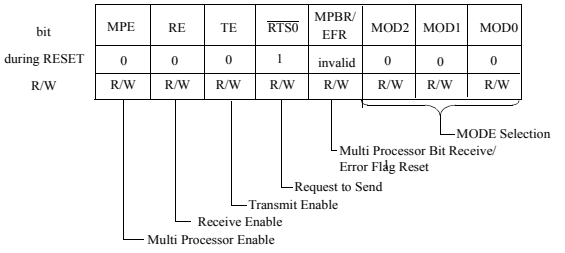
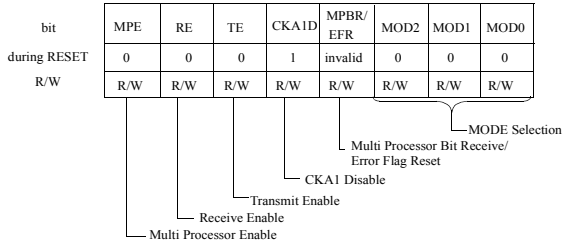
MNEMONICS	Bytes	Machine Cycles	States
	3	3	9 (If f is true)
JP (HL)	1	1	3
JP (IX)	2	2	6
JP (IY)	2	2	6
JP mn	3	3	9
JR j	2	4	8
JR C,j	2	2	6 (If condition is false)
	2	4	8 (If condition is true)
JR NC,j	2	2	6 (if condition is false)
	2	4	8 (If condition is true)
JR Z,j	2	2	6 (If condition is false)
	2	4	8 If condition is true)
JR NZ,j	2	2	6 (If condition is false)
	2	4	8 (If condition is true)
LD A, (BC)	1	2	6
LD A, (DE)	1	2	6
LD A,I	2	2	6
LD A, (mn)	3	4	12
LD A,R	2	2	6
LD (BC),A	1	3	7
LDD	2	4	12

I/O Registers

INTERNAL I/O REGISTERS

By programming IOA7 and IOA6 as the I/O control register, internal I/O register addresses are relocatable within ranges from 0000H to 00FFH in the I/O address space.

Table 57. Internal I/O Registers

Register	Mnemonics	Address		Remarks
ASCI Control Register A Channel 0:	CNTLA0	0	0	
ASCI Control Register A Channel 1:	CNTLA1	0	1	

MOD 2 1 0
0 0 0 Start + 7 bit Data + 1 Stop
0 0 1 Start + 7 bit Data + 2 Stop
0 1 0 Start + 7 bit Data + Parity + 1 Stop
0 1 1 Start + 7 bit Data + Parity + 2 Stop
1 0 0 Start + 8 bit Data + 1 Stop
1 0 1 Start + 8 bit Data + 2 Stop
1 1 0 Start + 8 bit Data + Parity + 1 Stop
1 1 1 Start + 8 bit Data + Parity + 2 Stop

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Status Channel 0:	STAT0	0	4	

bit	RDRF	OVRN	PE	FE	RIE	$\overline{DCD0}$	TDRE	TIE
during RESET	0	0	0	0	invalid	*	**	0
R/W	R	R	R	R	R/W	R	R	R/W

Transmit Interrupt Enable
Transmit Data Register Empty
Data Carrier Detect
Receive Interrupt Enable
Framing Error
Parity Error
Overrun Error
Receive Data Register Full

** $\overline{CTS_0}$ Pin	TDRE
L	1
H	0

* $\overline{DCD_0}$: Depending on the condition of $\overline{DCD_0}$ Pin.

ASCI Status Channel 1:	STAT1	0	5

bit	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
during RESET	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R/W	R	R	R/W

Transmit Interrupt Enable
Transmit Data Register Empty
$\overline{CTS1}$ Enable
Receive Interrupt Enable
Framing Error
Parity Error
Overrun Error
Receive Data Register Full

ORDERING INFORMATION

Codes

- Package
  P = Plastic Dip
  V = Plastic Chip Carrier
  F = Quad Flat Pack
- Temperature
  S = 0°C to +70°C
  E = -40°C to 100°C
- Speed
  06 = 6 MHz
  08 = 8 MHz
  10 = 10 MHz
- Environmental
  C = Plastic Standard
- Example
  Z8018008PSC is an 80180 8 MHz, Plastic DIP, 0°C to 70°C, Plastic Standard Flow.