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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008psc

Table 2. Multiplexed Pin Descriptions

Multiplexed Pins	Descriptions
A18/TOUT	During RESET, this pin is initialized as A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, TOUT function is selected. If TOC1 and TOC0 bits are cleared to 0, A18 function is selected.
CKA0/$\overline{\text{DREQ0}}$	During RESET, this pin is initialized as CKA_0 pin. If either DM1 or SM1 in DMA Mode Register (DMODE) is set to 1, $\overline{\text{DREQ0}}$ function is always selected.
CKA1/$\overline{\text{TEND0}}$	During RESET, this pin is initialized as CKA1 pin. If CKA1D bit in ASCI control register ch 1 (CNTLA1) is set to 1, $\overline{\text{TEND0}}$ function is selected. If CKA1D bit is set to 0, CKA1 function is selected.
RXS/$\overline{\text{CTS1}}$	During RESET, this pin is initialized as RXS pin. If CTS1E bit in ASCI status register ch 1 (STAT1) is set to 1, $\overline{\text{CTS1}}$ function is selected. If CTS1E bit is 0, RXS function is selected.

ARCHITECTURE

The Z8X180 combines a high performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller (including dynamic memory refresh), interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks:

- Direct Memory Access (DMA) Control (2 channels)
- Asynchronous Serial Communications Interface (ASCI, 2 channels),

The external bus is IDLE while the CPU computes the effective address. Finally, the computed memory location is written with the contents of the CPU register (g).

RESET Timing

Figure 15 depicts the Z8X180 hardware RESET timing. If the $\overline{\text{RESET}}$ pin is Low for six or more clock cycles, processing is terminated and the Z8X180 restarts execution from (logical and physical) address `00000H`.

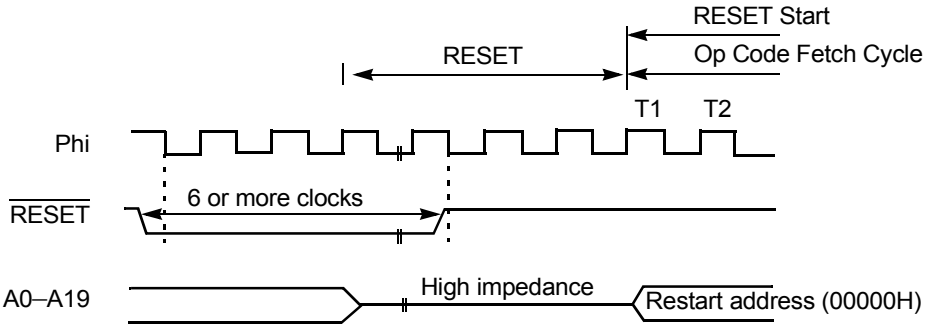

Figure 15. RESET Timing Diagram

$\overline{\text{BUSREQ}}$/$\overline{\text{BUSACK}}$ Bus Exchange Timing

The Z8X180 can coordinate the exchange of control, address and data bus ownership with another bus master. The alternate bus master can request the bus release by asserting the $\overline{\text{BUSREQ}}$ (Bus Request) input Low. After the Z8X180 releases the bus, it relinquishes control to the alternate bus master by asserting the $\overline{\text{BUSACK}}$ (Bus Acknowledge) output Low.

The bus may be released by the Z8X180 at the end of each machine cycle. In this context, a machine cycle consists of a minimum of three clock cycles (more if wait states are inserted) for Op Code fetch, memory read/write, and I/O read/write cycles. Except for these cases, a machine cycle corresponds to one clock cycle.

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only)

	Register	Mnemonic	Address		
			Binary	Hex	Page
ASCI	ASCI Control Register A Ch 0	CNTLA0	XX000000	00H	125
	ASCI Control Register A Ch 1	CNTLA1	XX000001	01H	128
	ASCI Control Register B Ch 0	CNTLB0	XX000010	02H	132
	ASCI Control Register B Ch 1	CNTLB1	XX000011	03H	132
	ASCI Status Register Ch 0	STAT0	XX000100	04H	120
	ASCI Status Register Ch 1	STAT1	XX000101	05H	123
	ASCI Transmit Data Register Ch 0	TDR0	XX000110	06H	118
	ASCI Transmit Data Register Ch 1	TDR1	XX000111	07H	118
	ASCI Receive Data Register Ch 0	RDR0	XX001000	08H	119
	ASCI Receive Data Register Ch 1	RDR1	XX001001	09H	119
	ASCI0 Extension Control Register 0	ASEXT0	XX010010	12H	135
	ASCI1 Extension Control Register 1	ASEXT1	XX010011	13H	136
	ASCI0 Time Constant Low	ASTC0L	XX011010	1AH	137
	ASCI0 Time Constant High	ASTC0H	XX001011	1BH	137
	ASCI1 Time Constant Low	ASCT1L	XX001100	1CH	138
	ASCI1 Time Constant High	ASCT1H	XX001101	1DH	138
CSI0	CSI0 Control Register	CNTR	XX001010	0AH	147
	CSI0 Transmit/Receive Data Register	TRD	XX1011	0BH	149

Clock Multiplier Register (CMR: 1EH) (Z8S180/L180-Class Processors Only)

Bit	7	6						0
Bit/Field	X2	Reserved						
R/W	R/W	?						
Reset	0	1						

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	X2 Clock Multiplier Mode	R/W		X2 Clock Multiplier Mode
			0	Disable
			1	Enable
6–0	Reserved	?	?	Reserved

MMU and RESET

During RESET, all bits of the CA field of CBAR are set to 1 while all bits of the BA field of CBAR, CBR and BBR are reset to 0. The logical 64KB address space corresponds directly with the first 64KB 0000H to FFFFH) of the 1024KB 00000H. to FFFFFH) physical address space. Thus, after RESET, the Z8X180 begins execution at logical and physical address 0.

MMU Register Access Timing

When data is written into CBAR, CBR or BBR, the value is effective from the cycle immediately following the I/O write cycle which updates these registers.

During MMU programming insure that CPU program execution is not disrupted. The next cycle following MMU register programming is normally an Op Code fetch from the newly translated address. One technique is to localize all MMU programming routines in a Common Area that is always enabled.

Function	Name	Access Method
Interrupt Vector High	I	LD A,I and LD I, A instructions
Interrupt Vector Low	IL	I/O instruction (addr = 33H)
Interrupt/Trap Control	ITC	I/O instruction (addr = 34H)
Interrupt Enable Flag 1,2	IEF1, IEF2	El and DI

Interrupt Vector Register (I)

Mode 2 for $\overline{\text{INT0}}$ external interrupt, $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ external interrupts, and all internal interrupts (except TRAP) use a programmable vectored technique to determine the address at which interrupt processing starts. In response to the interrupt a 16-bit address is generated. This address accesses a vector table in memory to obtain the address at which execution restarts.

While the method for generation of the least significant byte of the table address differs, all vectored interrupts use the contents of I as the most significant byte of the table address. By programming the contents of I, vector tables can be relocated on 256 byte boundaries throughout the 64KB logical address space.

Note: I is read/written with the LD A, I and LD I, A instructions rather than I/O (IN, OUT) instructions. I is initialized to `00H` during RESET.

Interrupt Vector Low Register

This register determines the most significant three bits of the low-order byte of the interrupt vector table address for external interrupts $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ and all internal interrupts (except TRAP). The five least significant bits are fixed for each specific interrupt source. By programming IL, the

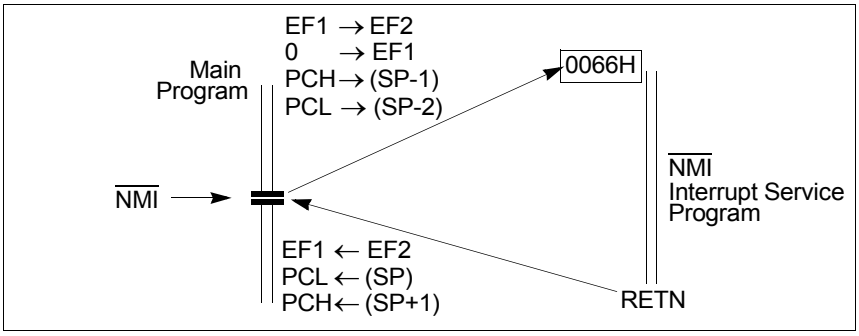

Figure 34. NMI Use

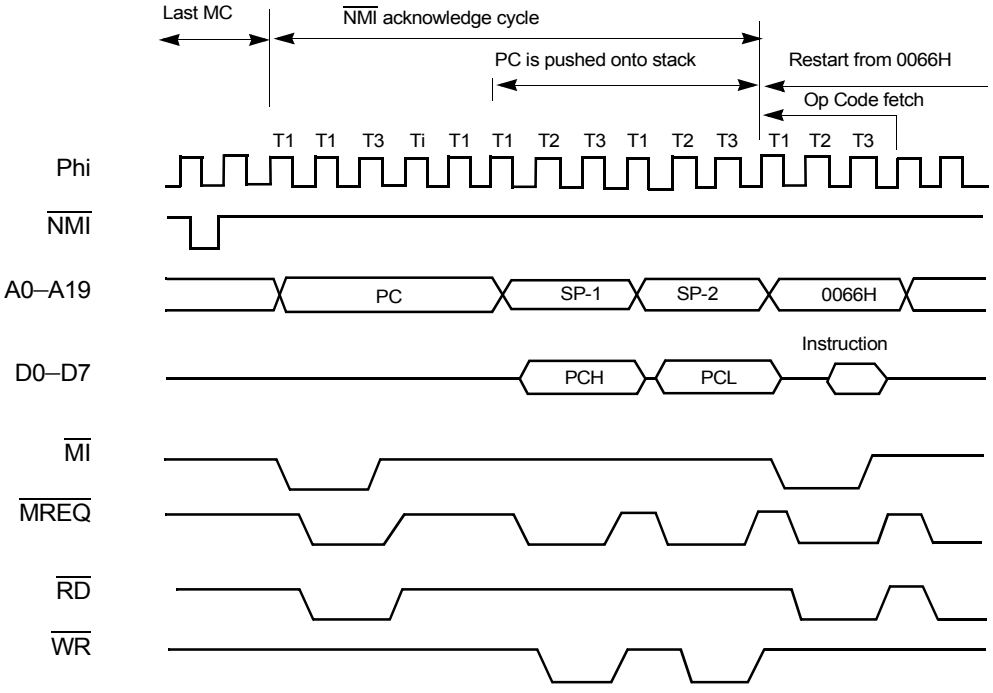

Table 11. DRAM Refresh Intervals

CYC1	CYC0	Insertion Interval	Time Interval				
			10 MHz	8 MHz	6 MHz	4 MHz	2.5 MHz
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.8 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

* Calculated interval

Refresh Control And RESET

After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of ten clock cycles and are three clock cycles in duration.

Dynamic Ram Refresh Operation Notes

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   - During RESET
   - When the bus is released in response to $\overline{\text{BUSREQ}}$
   - During SLEEP mode
   - During Wait States
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. Thus, the time at which the first refresh cycle occurs after the Z8X180 re-acquires the bus depends on the refresh timer and has no timing relationship with the bus exchange.

Table 14. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Increment/Decrement
1	1	0	0	Memory to I/O	SAR0+1, DAR0 fixed
1	1	0	1	Memory to I/O	SAR0-1, DAR0 fixed
1	1	1	0	Reserved	
1	1	1	1	Reserved	
Note: *: includes memory mapped I/O.					

DMA/WAIT Control Register (DCNTL)

DCNTL controls the insertion of Wait States into DMAC (and CPU) accesses of memory or I/O Also, the DMA request mode for each DREQ $\overline{\text{DREQ}}$0 and $\overline{\text{DREQ}}$1) input is defined as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

In addition, the operation of channel 0 DMA with the on-chip ASCI (Asynchronous Serial Communication Interface) as well as Channel 1 DMA are described.

Memory to Memory—Channel 0

For memory to/from memory transfers, the external $\overline{\text{DREQ0}}$ input is not used for DMA transfer timing. Rather, the DMA operation is timed in one of two programmable modes – BURST or CYCLE STEAL. In both modes, the DMA operation automatically proceeds until termination (shown by byte count-BCR0) = 0.

In BURST mode, the DMA operation proceeds until termination. In this case, the CPU cannot perform any program execution until the DMA operation is completed. In CYCLE STEAL mode, the DMA and CPU operation are alternated after each DMA byte transfer until the DMA is completed. The sequence:

- 1 CPU Machine Cycle
- DMA Byte Transfer

is repeated until DMA is completed. Figure 46 describes CYCLE STEAL mode DMA timing.

return accurate data without requiring the timer to be stopped. The write procedure requires the PRT to be stopped.

For reading (without stopping the timer), TMDR is read in the order of lower byte - higher byte (TMDRnL, TMDRnH). The lower byte read (TMDRnL) stores the higher byte value in an internal register. The following higher byte read (TMDRnH) accesses this internal register. This procedure insures timer data validity by eliminating the problem of potential 16-bit timer updating between each 8-bit read. Specifically, reading TMDR in higher byte–lower byte order may result in invalid data. Note the implications of TMDR higher byte internal storage for applications which may read only the lower and/or higher bytes. In normal operation all TMDR read routines must access both the lower and higher bytes, in that order. For writing, the TMDR down counting must be inhibited using the TDE (Timer Down Count Enable) bits in the TCR (Timer Control Register). Then, any or both higher and lower bytes of TMDR can be freely written (and read) in any order.

CSI/O Transmit/Receive Data Register (TRDR: I/O Address = 0BH).

TRDR is used for both CSI/O transmission and reception. Thus, the system design must insure that the constraints of half-duplex operation are met (Transmit and receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, the CSI/O does not work.

TRDR is not buffered. Attempting to perform a CSI/O transmit while the previous transmit data is still being shifted out causes the shift data to be immediately updated, thereby corrupting the transmit operation in progress. Similarly, reading TRDR during a transmit or receive must be avoided.

Addressing Modes

The Z80180 instruction set includes eight addressing modes.

- Implied Register
- Register Direct
- Register Indirect
- Indexed
- Extended
- Immediate
- Relative
- IO

Implied Register (IMP)

Certain Op Codes automatically imply register usage, such as the arithmetic operations that inherently reference the Accumulator, Index Registers, Stack Pointer, and General Purpose Registers.

Register Direct (REG)

Many Op Codes contain bit fields specifying registers used for operation. The exact bit field definitions vary depending on instruction depicted in Figure 75.

Instruction Set

This section explains the symbols in the instruction set.

REGISTER

g, g', ww, xx, yy, and zz specify a register to be used. g and g' specify an 8-bit register. ww, xx, yy, and zz specify a pair of 8-bit registers. Table 32 describes the correspondence between symbols and registers.

Table 32. Register Values

g,g'	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

ww	Reg.
00	BC
01	DE
10	HL
11	SP

xx	Reg.
00	BC
01	DE
10	IX
11	SP

yy	Reg.
00	BC
01	DE
10	IY
11	SP

zz	Reg.
00	BC
01	DE
10	HL
11	AF

Note: Suffixed H and L to ww, xx, yy, zz (ex. wwH, IXL) indicate upper and lower 8-bit of the 16-bit register respectively.

BIT

b specifies a bit to be manipulated in the bit manipulation instruction. Table 33 indicates the correspondence between **b** and bits.

Table 33. Bit Values

b	Bit
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

CONDITION

f specifies the condition in program control instructions. Table 34 describes the correspondence between **f** and conditions.

Table 34. Instruction Values

f	Condition	
000	NZ	Nonzero
001	Z	Zero
010	NC	Non Carry
011	C	Carry
100	PO	Parity Odd
101	PE	Parity Even
110	P	Sign Plus
111	M	Sign Minus

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
PUSH IX PUSH IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3~MC4	TiTi	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP-1	IXH IYH	1	0	0	1	1	1	1
	MC6	T1T2T3	SP-2	IXL IYL	1	0	0	1	1	1	1
RET	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC3	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
RET f (If condition is false)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2~MC3	TiTi	*	Z	1	1	1	1	1	1	1
RET f (If condition is true)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
RETI (R0, R1) RETN	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	SP	DATA	0	1	0	1	1	0	1
	MC4	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
RST v	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2 ~MC3	TiTi	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
SCF	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
SET b,g RES b,g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
SET b. (HL) RES b, (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2ndOp Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	HL	DATA	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
TST g**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
TST m**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
TST (HL)**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	2	0	2	0	2	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T23	HL	Data	0	1	0	1	1	1	1

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
CSI/O Transmit/ Receive Data Register:	TRDR	0	B	
Timer Data Register Channel 0L:	TMDR0L	0	C	
Timer Data Register Channel 0H:	TMDR0H	0	D	
Timer Reload Register Channel 0L:	RLDR0L	0	E	
Timer Reload Register Channel 0H:	RLDR0H	0	F	
Timer Control Register Channel 0L:	TCR	1	0